ME-8987

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298-0253

OPERATION AND MAINTENANCE MANUAL

for

PCM BIT SYNCHRONIZER

MODEL 335

March 1984

AYDIN MONITOR Systems
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Fort Washington, Pa. 19034 USA

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This manual is valid for units having serial numbers 403XXX and above.

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SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains the information necessary to install, operate and maintain the Model 335 PCM Bit Synchronizer, shown in figure 1-1. Sections I through V contain respectively the general description, installation procedures, operation procedures, theory of operation, and maintenance information. Parts lists, assembly drawings and schematic drawings are contained in section VI. Appendix A contains information on the +5 volt, ±15 volt power supply included in the bit synchronizer, and manufactured by acdc electronics, inc. (part number ET602-1).

Various options are available for the bit synchronizer. Information about the options needed to supplement the manual is located in appendices at the rear of the manual. The table below summarizes the options and the pertinent appendices.

	OPTIONS									
	10	11	20	21	22	P0	P1	T0	T1	
Model 335 Part Number	Standard Interface	Model 1126B Interface	No Soft Decision or Data Quality	Soft Decision Output (3 bits)	Data Quality Output (1 bit)	105-125Vac, 47-63 Hz Single-phase power (Standard)	230Vac 47-53 Hz Single-phase power (Option)	Bit Rate Range: 1 bps to 4.999 Mbps (Standard)	Bit Rate Range: 1 bps to 9.999 Mbps (Option)	Applicable Appendix
356-0002-501	X		X			Either Capability Available		Either Capability Available		N.A.
356-0002-502		X	X							B
356-0002-503	X			X						C
356-0002-504		X		X						D
356-0002-505	X				X					E
356-0002-506		X			X					F

1.2 PURPOSE OF EQUIPMENT

The bit synchronizer is used as a data and synchronization link between a receiver and a PCM decommutator. It converts telemetry data to the proper code format and logic levels required for decommutation. To do this, it extracts serial data from both filtered and unfiltered noise-contaminated inputs from telemetry receivers, tape recorders or PCM simulators. The bit synchronizer then conditions the input data, synchronizes the output with input transitions, reconstructs the data, converts the reconstructed data to standard codes, and generates four phases of clock.

3-1199

Figure 1-1. PCM Bit Synchronizer, Model 335

1.3 PHYSICAL DESCRIPTION

The bit synchronizer is a self-contained, solid-state electronic unit consisting of a chassis with mounting slides for installation in a 19-inch EIA equipment cabinet. All input and output cables are connected to the rear of the unit. All operating controls are located on the front panel. The top and bottom views of the bit synchronizer are shown in figures 1-2 and 1-3, respectively.

The bit synchronizer is 19 inches wide, 5-1/4 inches high and 23-1/2 inches deep; it weighs approximately 45 pounds. The chassis contains seven major areas; they are the front and rear panels, four printed circuit (pc) files identified as areas A1 through A4, and one power supply identified as PS1. In this model of the bit synchronizer, area A1 contains 11 pc cards, area A2 contains 4 pc cards, area A3 contains 5 pc cards and area A4 contains 5 pc cards. Thus, the bit synchronizer has a total complement of 25 plug-in pc cards including 21 different card types. Unused spaces in the pc files are not equipped with card connectors. These unused spaces are provided for future expansion of the capabilities within the bit synchronizer. The pc cards and their associated pc connectors are designed with keys to prevent insertion of the pc card into the wrong slot.

The rear panel contains 15 BNC connectors used for input and output signal connections, 2 slide switches, elapse time indicator, a fuse, a fan, an ac input connector, a system ground lug, a chassis ground lug and a multi-pin programming connector. The power supply is mounted on a subchassis which, in turn, is bolted to the main frame of the chassis. All wiring to the power supply is via terminal blocks so that, if necessary, the power supply can conveniently be removed for servicing.

1.4 FUNCTIONAL DESCRIPTION

A simplified block diagram of the bit synchronizer is shown in figure 1-4. The input data can be any of the PCM type codes that are shown and explained in figure 1-5. The input data may be contaminated with high noise level, the bit rate may be from 1.0 bps to 5.0 Mbps, the amplitude may be between 0.5 and 30 volts peak-to-peak, and the baseline may be offset up to 100 percent of the peak-to-peak amplitude. As an example of the latter, if the high and low levels of the input data waveform are 8 and 0 volts respectively, the baseline, midway between the high and low levels, is 4 volts and the peak-to-peak amplitude is 8 volts. Thus, the baseline offset is 4/8 times 100 or 50 percent and well within the 100 percent allowable. If the high and low levels are 8 and 4 volts respectively, the baseline is 6 volts and the peak-to-peak amplitude is 4 volts. Thus, the baseline offset is 6/4 times 100 or 150 percent and not acceptable as an input.

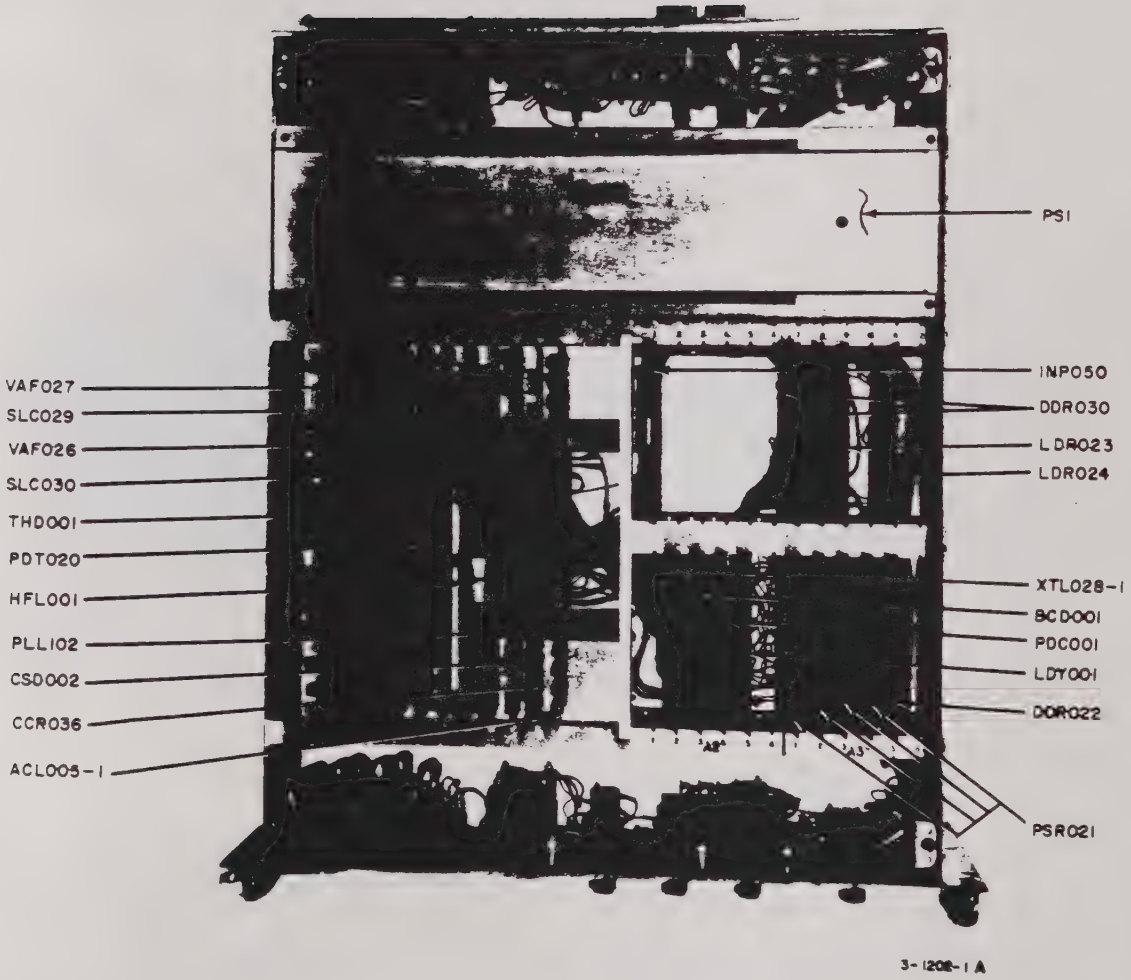


Figure 1-2. Bit Synchronizer, Top View

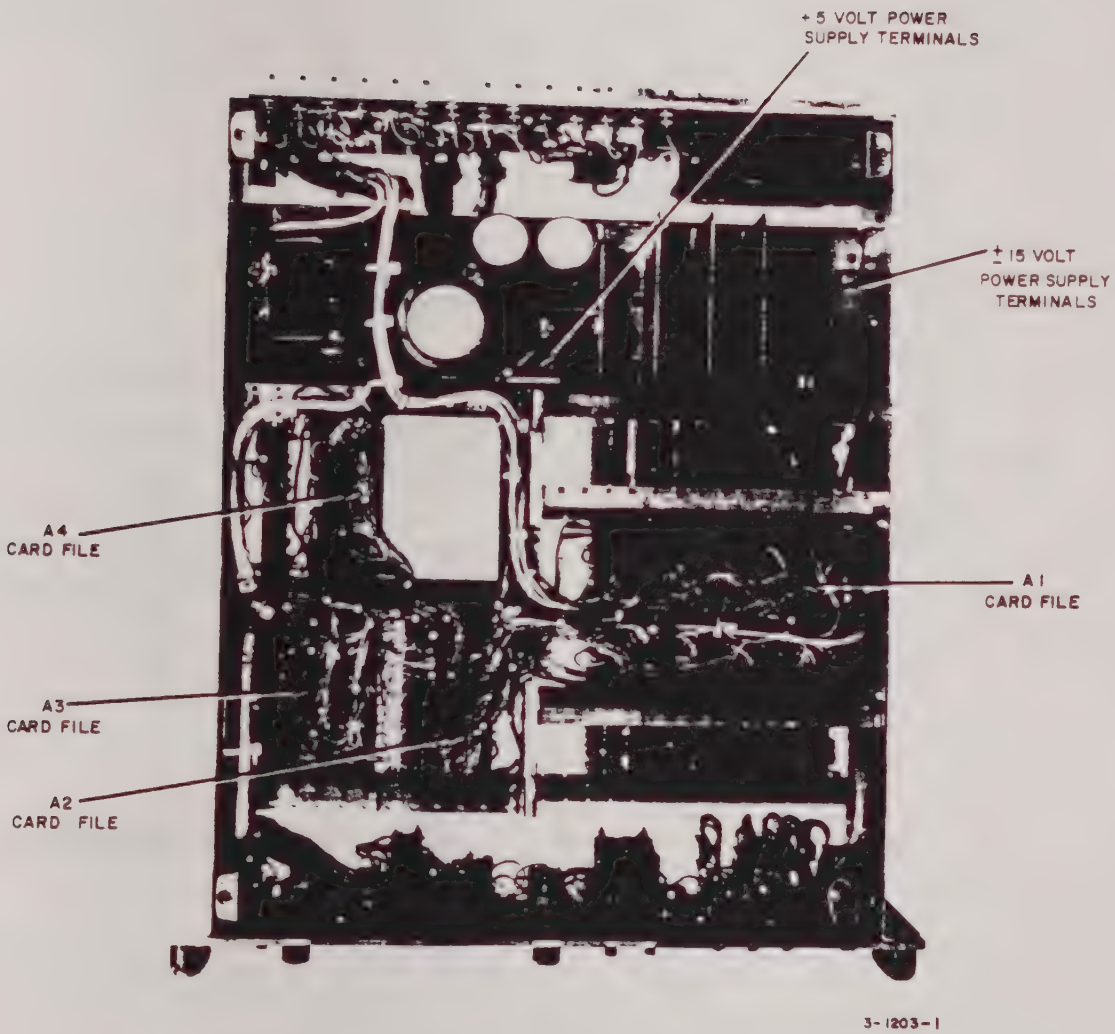


Figure 1-3. Bit Synchronizer, Bottom View

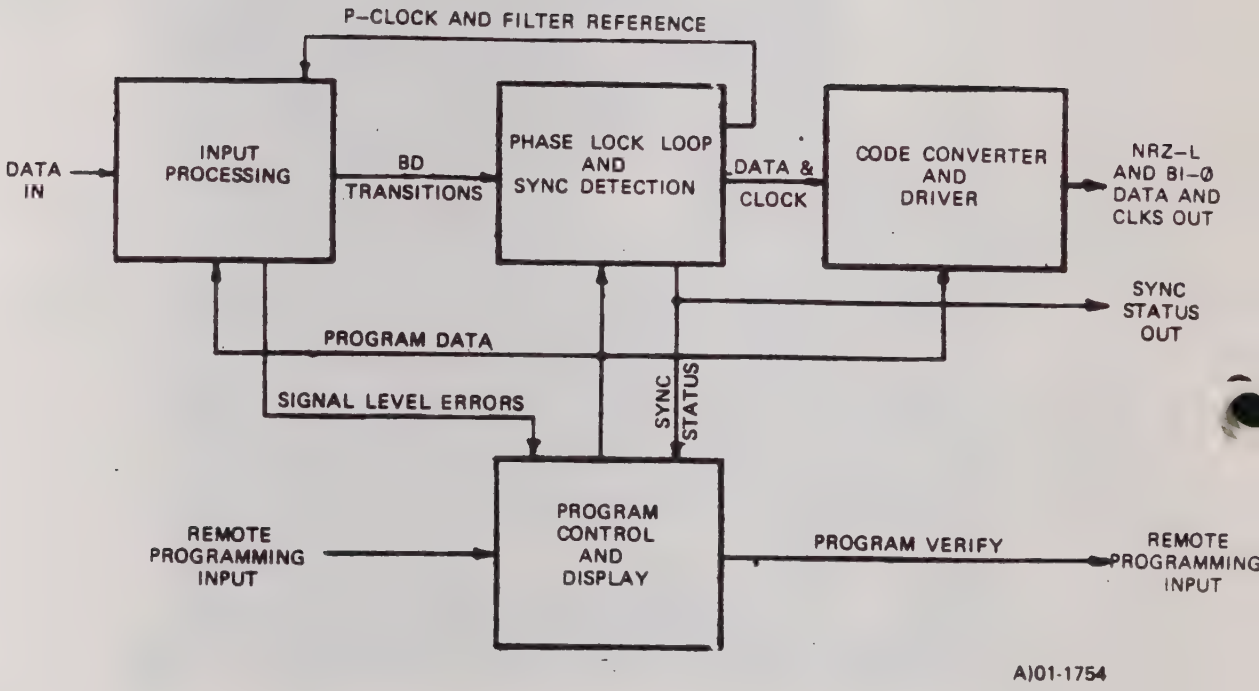


Figure 1-4. Bit Synchronizer, Simplified Block Diagram

Figure 1-5. PCM Codes

The input processing section selects one of the four inputs as specified by the program control and display section and normalizes the selected input to levels of +0.5 and -0.5 volt for processing. The normalized data is filtered and threshold detected to provide control signals that maintain the selected input normalized. The threshold detected signal also is transferred to the phase lock loop and sync detection section.

Four phases of clock are generated within the phase lock loop and sync section. The rate of the clock must be preset, manually or by program, to the approximate bit rate of the incoming signal. The threshold detected signal from the input processing section is then compared in phase with the generated clock. The resultant error signal is used to change the clock bit rate to precisely that of the incoming signal. The threshold detected signal is then level shifted and strobed with the synchronized clock to provide detected data bits in NRZ format.

The synchronized clock and the detected data bits are transferred to the code converter and driver section where they are processed and converted to NRZ-L and BiØ-L formats and then applied through line drivers to the output connectors. The clock, supplied in four phases, also is applied through line drivers to the output connectors.

Front panel programming or remote programming is selected, stored and displayed in the program control and display section. Also displayed are input signal level, sync status and loop phase error.

1.5 CONDENSED DATA

Table 1-1 gives the printed circuit card complement of the bit synchronizer, listing the function and reference designation of each. Table 1-2 lists the technical characteristics of the unit.

1.6 EQUIPMENT SUPPLIED AND REQUIRED

Table 1-3 lists the equipment supplied with the bit synchronizer. Table 1-4 lists the test equipment and tools needed for the installation and maintenance of the unit. Equivalent equipment and tools may be substituted.

Table 1-1. Printed Circuit Card Complement

CARD TYPE	REFERENCE DESIGNATION	FUNCTION	QTY.
VAFC27	A1A1	Low Frequency tracking filter and low frequency threshold detector	1
SLC029	A1A2	Variable gain and offset amplifier; low frequency AGC and offset control	1
VAF026	A1A3	High frequency tracking filter	1
SLC030	A1A4	High frequency AGC and offset control	1
THD001	A1A5	High frequency threshold detectors	1
PDT020	A1A6	Phase detector	1
HLF001	A1A7	High frequency tracking loop filter; equal and loss lamp test buffers	1
PLL102	A1A8	Low frequency tracking loop filter; lamp test and DEC4* buffers; polarity inverter	1
CSD002	A1A9	Countdown and sync detection	1
CCR036	A1A10	Code conversion; spill detection; decade adder	1
ACL009-1	A1A11	Auto-cal; voltage-controlled oscillator; digital/analog conversion; decade range splitter	1
XTL028-1	A2A2	1 kHz reference (derivative of 4 MHz crystal); MSD and NMSD comparator	1
BCD001	A2A3	Bit rate multiplier	1
PDC001	A2A4	Offset and input amplitude detection; program decoding; loop bandwidth adder; source select adder	1
LDY001	A2A5	Transition loss delay; reset	1
PSR021	A3A1-A3A4	Eight-bit program storage registers	4
DDR022	A3A5	Data distributor	1
INP050-1	A4A1	Input select	1
DDR030	A4A7, A4A8	Program verify	2
LDR023	A4A9	Line drivers	1
LDR024-1	A4A11	Bipolar line drivers	1

Table 1-2. Technical Characteristics

CHARACTERISTIC	DESCRIPTION
Bit Rates	1 to 5,000,000 bits/second for NRZ, RZ and BiØ codes and 1 to 2, 499, 999 bps for DM codes. Control may be local or remote.
Acceptable PCM	NRZ-L, NRZ-M, NRZ-S, RZ, BiØ-L, BiØ-M, and BiØ-S, DM-M, DM-S with polarity reversible by front panel switch.
Input	0.5 to 30 volts peak-to-peak, dc-coupled with automatic gain and offset control.
Input Impedance	50 ohms or 10,000 ohms minimum, shunted by 150 pf maximum.
Signal-to-Noise Performance	Within one dB of ideal signal/noise versus error probability curves, with effective synchronization to 0 dB.
Synchronization	Acquires bit synchronization with signal/noise of 0 dB. Maintains bit synchronization in the absence of input transitions for up to 128 bits.
Phase Lock Loop	Four phase lock loop bandwidths (.1, .3, 1.0, 2.0% of selected bit rate) permit optimization of performance.
Jitter Performance	Maintains sync for a wide range of jitter amplitudes and frequencies.
Base Line Shift	No degradation for base line variations of 100% of the peak-to-peak input signal amplitude.
Tracking	Tracks bit rate variations up to ±15%.
Acquisition Range	±5% of bit rate setting.
Acquisition Time	Locks to input waveform with 50% or more transitions within 500 bits and an input bit rate offset of ±2%, and locks within 100 bits average with no bit rate offset.
Outputs	Data: 0 to 3.5v into 50 ohms, simultaneous NRZ-L and BiØ-L. Clock: 0 to 3.5v into 50 ohms, 0°, 90°, 180° and 270° clock provided.

Table 1-2. Technical Characteristics (cont.)

CHARACTERISTIC	DESCRIPTION
Outputs (cont.)	Tape Recorder: Adjustable ±1v to ±3V into 50 ohms, simultaneous NRZ-L and BiØ-L.
Power Requirements	105 to 125 volts ac (210 to 250 volts ac optional) 60 Hz ±5% 1.5 amperes
Dimensions	Width: 19 inches Height: 5.25 inches Depth: 23.5 inches
Weight	Unpacked: 45 pounds Shipping: 55 pounds
Environment	Temperature: 0°C to 60°C Humidity: 0-95% no condensation Altitude: Sea level to 15,000 feet

Table 1-3. Equipment Supplied

NOMENCLATURE	PART NUMBER	QUANTITY
PCM Bit Synchronizer Top Assembly, Model 335	356-0002-[ ]	1
Operation and Maintenance Manual	298-0253	1
Acceptance Test Procedure	297-0477-501	1 (standard)
Acceptance Test Procedure	297-0477-502	1 w/option T1
Acceptance Test Procedure	297-0477-503	1 w/option 21
Acceptance Test Procedure	297-0477-504	1 w/option 11
Acceptance Test Procedure	297-0477-505	1 w/option 11 & 21
Acceptance Test Procedure	297-0477-506	1 w/option 22
Accessory Kit	354-0160-501	

Table 1-4. Equipment Required But Not Supplied

NAME	DESCRIPTION	MFR NAME AND ADDRESS	PART NO.
Oscilloscope	Five-inch, dual beam oscilloscope with sweep magnifier, calibrated sweep delay, dual time base, and automatic display switching.	Tektronix, Inc. Beaverton, Oregon	Model 547
Preamp	Dual-trace preamplifier with dc-to-50 MHz bandwidth and 7 ns rise time.	Tektronix, Inc. Beaverton, Oregon	Model 1A2
Frequency counter	Programmable counter with frequency range of dc to 35 MHz. Minimum display time less than 1 microsecond. Accuracy = 1 count = input time base accuracy.	Hewlett-Packard Palo Alto, Calif.	Model 5245L
Gaussian noise generator	Generates Gaussian white noise within a bandwidth of 5 Hz to 5 MHz.	Elgenco Hurricane, Utah	Model 610A
Multimeter	Volt-ohm-milliameter with voltage ranges covering 2.5 to 1000 vdc full scale.	Simpson Electric Co. Chicago, Illinois	Model 260
AC Voltmeter	RMS-AC Voltmeter with voltage ranges covering .3 millivolts to 300 volts.	Hewlett-Packard Palo Alto, Calif.	Model 3400A
4-pole reference filter	Tuneable filter with adjustment range from 20 Hz to 2 MHz roll-off is 36 db per octave.	Krohn-Hite Cambridge, Mass.	3202R
Function generator	Generates sine, square, triangle, and complex waveforms ranging from 1 MHz down to .0001 Hz.	Exact Electronics Hillsboro, Oregon	Model 505
Bit error monitor & PCM Simulator	Monitors and displays discrepancies between the simulated data and the regenerated data in a PCM test system.	Aydin Monitor Systems Fort Washington, Penna.	Model 852B
Digital multimeter	Volt-ohm-milliameter with digital readout	Fluke Manufacturing Co. Mount Lake Terrace, Wash.	Model 8050A

SECTION II

INSTALLATION

2.1 INTRODUCTION

This section provides the nformation necessary to unpack, install and check out the Model 33' PCM Bit Synchronizer in preparation for normal operation. Informa ion on programming the unit, and on external cabling, is also given.

2.2 UNPACKING

The bit synchronizer is packaged in a molded foam container within a sealed corrugated carton. To unpack the unit cut the tape, open the carton, lift off the top half of the foam container, and remove the equipment from the bottom half of the container. Retain all shipping material for possible repackaging and reshipment. Examine the contents carefully for any broken parts, and compare with packing slip lists for completeness of equipment. Report any damage or discrepancies to cognizant authorities.

2.3 TOOLS AND EQUIPMENT

No special tools or equipment are required for installation of the unit. The basic tools required are a 1/4-inch drill set, a 100-degree countersink, a common 6-inch screwdriver and a #2 Phillips head screwdriver.

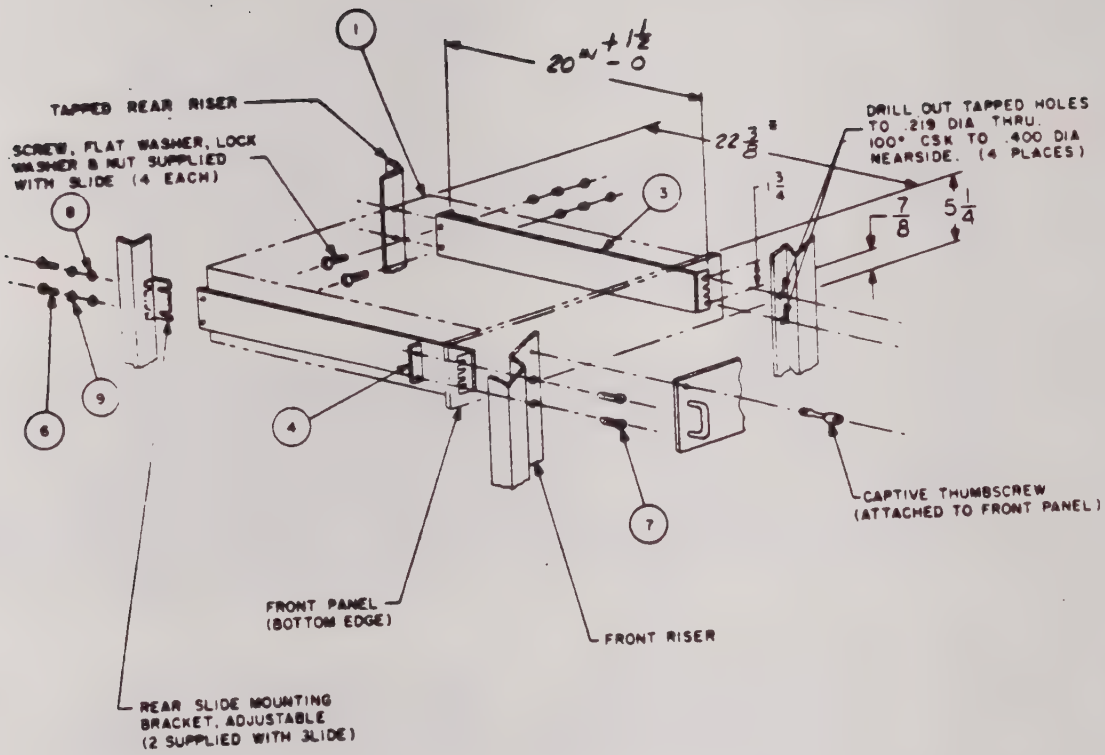
2.4 INSTALLATION PLANNING

The bit synchronizer is designed for mounting in a standard 19-inch EIA type rack. For rack mounting, 5 1/4 inches of vertical cabinet space is required, and sufficient space must be allowed at the rear of the unit for cabling. The depth of the unit, including rear connector cabling, is approximately 25 inches. Non-tilting chassis slides are provided with the unit for rack installation.

2.5 SLIDE INSTALLATION AND RACK MOUNTING PROCEDURE

The following steps outline the procedure for installing the chassis slides and rack-mounting the bit synchronizer. Refer to figure 2-1 for an illustration of the procedure.

a. Locate fixed front mounting brackets of slides on front risers so lowest mounting hole in bracket is 7/8 inch above front panel bottom edge as shown in figure 2-1.



∎ INCLUDES CONNECTORS MOUNTED TO REAR PANEL (NOT MATING CONNECTOR)

QTY	ITEM	FSCM	MONITOR P/N	MFR P/N	DESCRIPTION	NOTES
4	9	96906	128-202-138	MS35338-138	WASHER, LOCK, SPLIT, #10	
4	8	96906	128-200-808	MS15795-808	WASHER, FLAT, #10	
4	7	96906	127-105-272	MS24693-C272	SCREW, 100° FL HD, 10-32 X 1/2	
4	6	96906	127-101-063	MS51958-63	SCREW, PAN HD, 10-32 X 1/2	
	5					
2	4	83508	129-003-001	A300005	NUT BAR, 10-32	
1 PR	3	83508	132-031-005	03330-0107-14 -18-2-14	CHASSIS SLIDE	
	2					
REF	1	20747	356-0002-☐	———	ASSEMBLY	

Figure 2-1. Slide Assembly, Exploded View

b. Drill eight 0.219 inch diameter holes, four holes through rear vertical risers and four holes through front vertical risers.

c. Countersink (100 degrees) holes drilled through front vertical risers to 0.400 inch diameter. Countersink four holes from front vertical risers.

d. Mount rear brackets to slides, using No. 10-32 x 7/16 inch screws and nuts; adjust for correct length of travel.

e. Mount front brackets to front risers back side using No. 10-32 x 5/8 inch flat head screws and nuts as shown.

f. Attach rear brackets to rear riser front using No. 10-32 x 7/16 inch pan head screws, washers, and nuts as shown.

g. Pull out slides, mount chassis and slide back until first catch is engaged.

h. Release first catch and slide back gently until back side of panel seats against front risers.

i. Chassis is now installed and can be secured to rack by installing panel screws through holes located immediately adjacent to handles.

2.6 CABLING

All external connections to the bit synchronizer are made at the rear panel of the unit, as shown in figure 2-2. The function of each BNC connector is given in table 2-1. The pin assignments for J17 and J18 remote programming connectors are given in table 2-2.

2.7 PROGRAMMING INFORMATION

As shown in table 2-3, the remote programming capability is implemented by 16 data lines connected to the specific pins of J17 (or J16).

To accept the programmed data, the MANUAL-PROGRAM switch must be in the PROGRAM position. The programming information is contained in four 16-bit words which are loaded bit parallel, word serially. The four 16-bit words input to the bit synchronizer the same parameters that are, in MANUAL mode, input from the front panel controls. Each of the four words is divided into an instruction, instruction address and unit address. The instruction, bits CB0 through CB7, specifies the parameters to be inputted. Table 2-4 gives the bit assignment for each instruction. These bits are applied through data word buffers to one of the four 8-bit registers in the program storage

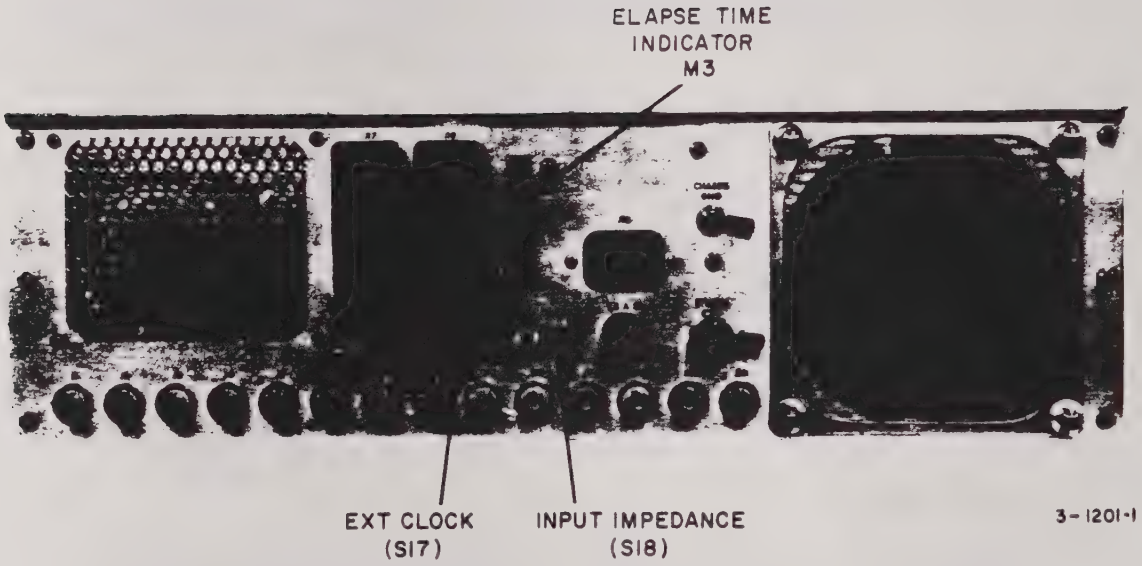


Figure 2-2. Bit Synchronizer, Rear View

section as specified by bits CB8, CB9, and CB10, which comprise the instruction address. Bits CB8, CB9, and CB10 of the instruction address are decoded to provide the four WRITE levels which direct the instruction into the assigned storage register. When TRANSFER STROBE and WRITE ENABLE are received in conjunction with the correct unit address decode, the instruction will be transferred to the specified storage register. The four bits of unit address, CB12, CB13, CB14, and CB15, are received from the computer via J17/J18. The bit synchronizer is pre-assigned a certain unit address; when the proper unit address is received, the unit will then be enabled to either WRITE into the program storage register or READ the output of storage registers through the program verify section.

Table 2-1. BNC Rear Panel Connectors

DESIGNATION	FUNCTION
J1	+3v 0° Clock 2 Output
J2	+3v 90° Clock 2 Output
J3	+3v NRZ 2 Output
J4	+3v 0° Clock 1 Output
J5	+3v 90° Clock 1 Output
J6	+3v 180° Clock Output
J7	+3v 270° Clock Output
J8	+3v NRZ 1 Output
J9	Tape Recorder NRZ Output
J10	Tape Recorder BiØ Output
J11	Data Input 4
J12	Data Input 3
J13	Data Input 2
J14	Data Input 1
J15	External Clock Input

*J1 thru J8 TTL logic compatible outputs
J9 and J10 bipolar outputs

Table 2-2. J17/J18 Remote Programming Connectors

PIN	SIGNAL	REMARKS
A	CB0	Instruction
B	CB1	
C	CB2	
D	CB3	
E	CB4	
F	CB5	
H	CB6	
J	CB7	
K	CB8	Function Address
L	CB9	
M	CB10	
P	CB12	Unit Address
R	CB13	
S	CB14	
T	CB15	

PIN	SIGNAL	REMARKS
AA	VR0	Program Verify
BB	VR1	
CC	VR2	
DD	VR3	
EE	VR4	
FF	VR5	
HH	VR6	
JJ	VR7	
U	TRANSFER STROBE	Remote Program Control
V	INPUT ACKNOWLEDGE	
W	TRANSFER STROBE RETURN	
X	READ REQUEST	
Y	WRITE REQUEST	
Z	D-GND	
LL	LOOP RESET	
KK	SYNC	
MM	D-GND	
NN	D-GND	

Table 2-3. 16-Bit Word Format

	UNIT ADDRESS				FUNCTION ADDRESS				INSTRUCTION							
BIT NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIN NO. J17/J18	T	S	R	P		M	L	K	J	H	F	E	D	C	B	A
WORD 1	0	0	0	1	-	0	1	1	MSD					NMSD		
WORD 2	0	0	0	1	-	0	1	0	NLSD					LSD		
WORD 3	0	0	0	1	-	0	0	1	SOURCE			MULTIPLIER			-	POL
WORD 4	0	0	0	1	-	0	0	0	-	-	CODE				LOOP	

Table 2-4. Instruction Format

SPECIFIED PARAMETER	BIT ASSIGNMENT							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WORD 1								
MSD of bit rate:								
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
NMSD of bit rate:								
0					0	0	0	0
1					0	0	0	1
2					0	0	1	0
3					0	0	1	1
4					0	1	0	0
5					0	1	0	1
6					0	1	1	0
7					0	1	1	1
8					1	0	0	0
9					1	0	0	1
WORD 2								
NLSD of bit rate:								
0	0	0	0	0				
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				

Table 2-4. Instruction Format (cont.)

SPECIFIED PARAMETER	BIT ASSIGNMENT							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WORD 2 (cont.)								
NLSD of bit rate: (cont.)								
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
LSD of bit rate:								
0					0	0	0	0
1					0	0	0	1
2					0	0	1	0
3					0	0	1	1
4					0	1	0	0
5					0	1	0	1
6					0	1	1	0
7					0	1	1	1
8					1	0	0	0
9					1	0	0	1
WORD 3								
Polarity:								
+							N/U	0
-							N/U	1
Multiplier of bit rate:								
0				0	0	0	N/U	
1				0	0	1	N/U	
2				0	1	0	N/U	
3				0	1	1	N/U	
4				1	0	0	N/U	
5				1	0	1	N/U	
6				1	1	0	N/U	
Source:								
1	0	0	0				N/U	
2	0	0	1				N/U	
3	0	1	0				N/U	
4	0	1	1				N/U	

Table 2-4. Instruction Format (cont.)

SPECIFIED PARAMETER	BIT ASSIGNMENT							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WORD 4								
Loop:								
1	N/U	N/U					0	0
2	N/U	N/U					0	1
3	N/U	N/U					1	0
4	N/U	N/U					1	1
Code:								
NRZ-S	N/U	N/U	0	0	0	0		
NRZ-M	N/U	N/U	0	0	0	1		
NRZ-L	N/U	N/U	0	0	1	0		
RZ	N/U	N/U	0	0	1	1		
BiØ-L	N/U	N/U	0	1	0	0		
BiØ-M	N/U	N/U	0	1	0	1		
BiØ-S	N/U	N/U	0	1	1	0		
DM-S	N/U	N/U	0	1	1	1		
DM-M			1	1	1	1		

Note: N/U is bit not used in applicable word.

2.8 PROGRAM VERIFICATION

A unique multiplexed program verify output permits checking of stored instructions on a functional basis. Program verification takes place when the following conditions exist: the write request line is low, the read request line is high, and the remote program setup has the correct unit address.

By varying the function address (refer to table 2-3), each of the four storage registers may be interrogated as to their contents. Since the verified outputs are positive-time logic, the verified format is identical to the program input format (refer to table 2-4).

Should either of the two program verification conditions last mentioned not exist, the verified outputs go to a logic high.

Logic levels of all control and monitor signals are as follows:

a. Program inputs: logic ONE, +2.0 to +5.5 volts.
logic ZERO, 0 to 0.8 volts

b. Verify outputs (DTL/TTL logic compatible): open collector outputs.

c. Strobe pulse is positive-going with minimum width of 500 nanoseconds.

2.9 PREOPERATIONAL CHECKOUT

Perform the following preoperational checkout to ensure that the bit synchronizer is operating properly. If normal indications are not obtained, refer to section IV.

a. Set POWER switch to ON. POWER indicator lights.

b. Depress LAMP TEST pushbutton. All indicators and all segments of displays light.

c. Set MANUAL/PROGRAM switch to MANUAL.

d. Set SCURCE switch to 1. Numeral in source display is 1.

e. Set CCDE switch to NRZ-L. NRZ and L code indicators light.

f. Set POLARITY switch to +. Symbol in POLARITY display is +.

g. Set BIT RATE switches to $2.000 \times 10^{5}_{5}$ for 200 Kbps. Numerals in BIT RATE display read 2.000×10^{5}.

h. Set LOOP BAND switch to 4. Numeral in LOOP display is 4.

i. Connect square wave generator to J14, SOURCE 1 connector. Set generator to obtain a 100 kHz output at 5 volts p-p. Red LOSS indicator goes off and green SYNC indicator lights. Observe INPUT AMPLITUDE meter: indicator needle should be in green area.

j. Set SOURCE switch to 2: SYNC indicator goes off and LOSS indicator lights. Return SOURCE switch to 1. SYNC and LOSS indicators return to original condition.

k. With unit in synchronization, observe that LOOP DEVIATION meter is nulled, or very nearly so.

l. Adjust input signal frequency to approximately 95 kHz. Depress and release RESET pushbutton. SYNC indicator goes off while RESET switch is depressed, and the AUTO-CAL cycle is initiated. After two seconds the SYNC indicator lights, indicating the unit is synchronized, and the AUTO-CAL indicator goes out.

m. Readjust input signal frequency to 100 kHz. Using an oscilloscope, observe the front panel test points marked NRZ-L and 0° clock. Observe that both outputs are square waves varying in amplitude from ground to +5 volts. Also observe that 0° clock is twice the rate of the NRZ-L output, and that the transition edges of the two signals occur in coincidence.

2.10 PREPARATION FOR RESHIPMENT

To prepare the bit synchronizer for reshipment, disconnect all cables from the rear panel and slide the unit out of the equipment rack. Make sure that the cover is secured. Place the unit in the shipping container saved when the unit was unpacked. Place the foam insert over the unit and seal the container. Clearly mark the outside as to its contents.

SECTION III

OPERATION

3.1 GENERAL

This section contains complete instructions for operating the bit synchronizer under normal and emergency conditions. Also included is a tabulation of the operating controls, indicators and front panel test points.

3.2 CONTROLS, INDICATORS AND TEST POINTS

Controls, indicators and test points are shown in figure 3-1 and explained in table 3-1.

3.3 NORMAL OPERATING PROCEDURES

Normal operating instructions include the turn-on procedure, manual and program operating modes, and the shutdown procedure.

3.3.1 Turn-On Procedure

The proper procedure to turn on the bit sync is as follows:

a. Set POWER switch to the ON position. POWER indicator lights.

b. Depress LAMP TEST pushbutton. All indicators light, BIT RATE, SOURCE and LOOP displays provide numeral 8 and POLARITY display provides symbol +.

c. Allow about a two minute warmup period before proceeding to allow the circuits to stabilize, particularly if the bit rate is in the low frequency range (10^3 bps or lower).

3.3.2 Manual Mode of Operation

To operate the bit synchronizer in the manual mode, proceed as follows:

a. Set MANUAL/PROGRAM switch to MANUAL position.

b. Set CLOCK switch to EXT position if an external clock is connected to J15 or to INT position if an external clock is not provided. If EXT position is selected EXTERNAL CLOCK indicator lights.

c. Set TERMINATION switch to HIGH or LOW position to agree with the impedance characteristics of the input PCM signal cable.

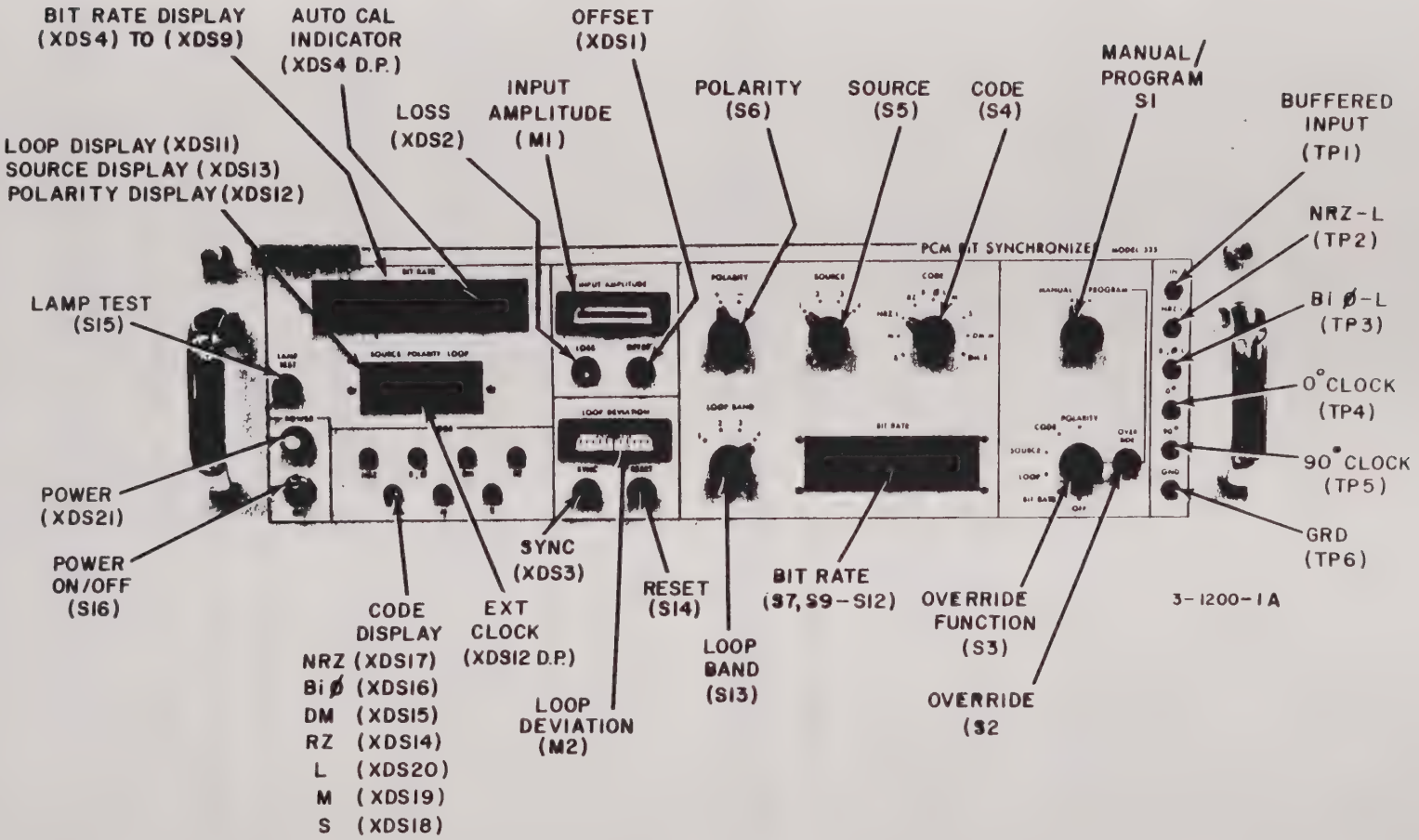


Figure 3-1. Bit Synchronizer, Operating Controls, Indicators and Test Points

Table 3-1. Operating Controls, Indicators and Test Points

NAME	FUNCTION
MANUAL/PROGRAM switch, S1	MANUAL position provides for manual operation using front panel controls. PROGRAM position provides for operation with parameters input by program rather than front panel controls.
OVERRIDE pushbutton, S2	Used during program mode only. When depressed, transfers data from switch selected by override function switch S3 to program storage registers.
OVERRIDE function switch, S3	Used with OVERRIDE pushbutton S2 during program mode only. Selects type of parameter to be transferred.
CODE switch, S4	Selects one of nine PCM codes that corresponds to the selected input PCM code. Selectable input codes are NRZ-L, NRZ-M, NRZ-S, RZ, BiØ-L, BiØ-M, BiØ-S, DM-M and DM-S.
SOURCE switch, S5	Selects one of four (1, 2, 3, or 4) input PCM data sources.
POLARITY switch, S6	In + position, phase of output PCM is same as phase of input PCM. In - position, phase of output PCM is the inverse (by 180°) of phase of input PCM.
BIT RATE thumbwheels, S7, S9 through S12	Sets bit rate of bit synchronizer to agree with bit rate of input PCM between 1.000×10^{0} (1 bps) and 5.000×10^{6} (5 megabits). Bit rates above 5 megabits exceed specifications of bit synchronizer. S7 is the multiplier and S12 is the most significant digit.
LOOP BAND switch, S13	Selects one of four phase lock loop filter bandwidths.
RESET pushbutton, S14	When depressed, initiates an AUTO-CAL cycle.
LAMP TEST pushbutton, S15	When depressed, lights all indicators and display segments.
POWER switch, S16	In ON position, applies power to bit synchronizer, and in OFF position, removes power from bit synchronizer.
CLOCK switch, S17 (located on rear panel)	In INT position, bit rate clock is synchronized from PCM data, and in EXT position, when an external clock is applied to J15, bit rate clock is synchronized from external clock.
TERMINATION switch, S18 (located on rear panel)	In HIGH position, terminates selected input data line into 10,000 ohms, and in LOW position, terminates selected input data line into 50 ohms.

Table 3-1. Operating Controls, Indicators and Test Points (cont.)

NAME	FUNCTION
INPUT AMPLITUDE meter, M1	Indicates relative amplitude of input PCM.
LOOP DEVIATION meter, M2	Indicates direction and magnitude of phase lock loop error voltage.
OFFSET indicator, XDS1	Indicates, when lit, that input signal is exceeding ±100 percent offset.
LOSS indicator, XDS2	Indicates, when lit, that data transitions are not being detected, usually due to excessively low input PCM.
SYNC indicator, XDS3	Indicates, when lit, that input PCM is synchronized with generated clock, thus indicating normal operation.
BIT RATE display, XDS4 thrugh XDS9	Displays numerical readout of selected bit rate.
AUTO-CAL indicator, decimal point portion of XDS4	Indicates, when lit, that AUTO-CAL cycle is in progress.
EXTERNAL CLOCK indicator, decimal point portion of XDS12	Indicates, when lit, that CLOCK switch, S17, is in EXT position.
LOOP display, XDS11	Displays numerical readout of selected loop bandwidth.
POLARITY display, XDS12	Displays (+ or -) readout of selected polarity.
SOURCE display, XDS13	Displays numerical readout of selected source.
CODE indicators: RZ, XDS14 DM, XDS15 BiØ, XDS16 NRZ, XDS17 S, XDS18 M, XDS19 L, XDS20	Indicates, when lit, selected PCM code.
POWER indicator, XDS21	Indicates, when lit, that power is on.
IN test point, TP1	For monitoring PCM input at 1/3 amplitude.

Table 3-1. Operating Controls, Indicators and Test Points (cont.)

NAME	FUNCTION
NRZ-L test point, TP2	For monitoring NRZ-L PCM output,
BiØ-L test point, TP3	For monitoring BiØ-L PCM output.
0° test point, TP4	For monitoring 0° clock output.
90° test point, TP5	For monitoring 90° clock output.
GND test point, TP6	For convenient connection of oscilloscope ground return lead.

d. Set CODE switch to a position corresponding to the type of PCM that is to be processed. CODE indicators corresponding to the selected code light.

e. Set SOURCE switch to position 1, 2, 3 or 4, depending on whether the desired input PCM signal is connected to J14, J13, J12 or J11, respectively. SOURCE display provides a numeral corresponding to the selected source.

f. Normally, POLARITY switch is set to + which causes the phase of the output PCM to be the same as the input PCM. However, if it is desired to change the output PCM phase by 180 degrees, set POLARITY switch to -. POLARITY display provides symbol + or - corresponding to selected polarity.

g. Set BIT RATE thumbwheels to the bit rate of the incoming PCM. BIT RATE display provides the selected bit rate.

h. Set LOOP BAND switch to optimize the characteristics of the bit synchronizer to accept jitter and high noise levels on the incoming PCM signal. If the incoming signal has a high signal-to-noise ratio and possibly some jitter, set LOOP BAND switch to position 4 (widest bandwidth). If the incoming signal has no jitter but has a low signal-to-noise ratio, set LOOP BAND switch to position 1 (narrowest bandwidth). Positions 2 and 3 of LOOP BAND switch are selected for intermediate values of jitter (which require a narrower bandwidth as the signal-to-noise ratio decreases).

i. Observe that INPUT AMPLITUDE meter indicates in green area; otherwise level of input PCM must be adjusted to within specifications of the bit synchronizer.

j. Depress RESET pushbutton to clear any residual error voltage or false lock and to initiate an AUTO-CAL cycle. The duration of an AUTO-CAL cycle is approximately 2 seconds. AUTO-CAL indicator remains lit for the duration of AUTO-CAL cycle (approximately two seconds).

k. During operation, monitor LOSS, OFFSET and SYNC indicators and LOOP DEVIATION meter. LOSS and OFFSET indicators should not be lit. SYNC indicator must remain lit. LOOP DEVIATION meter must indicate center scale at 0. If these indicators or meter provide an abnormal indication, depress RESET pushbutton. After AUTO-CAL cycle is completed (when AUTO-CAL indicator goes out), indicators and meter should provide normal indications; otherwise, troubleshooting is required (refer to section V).

3.3.3 Program Mode of Operation

To operate the bit synchronizer in the program mode, proceed as follows:

a. Set MANUAL/PROGRAM switch to the PROGRAM position.

b. To set the UNIT ADDRESS, select the jumper option on DDR022 (A3A5) to the desired 4-bit code.

c. Strobe the four data words into the bit synchronizer. (See section II for programming information.) Criteria used to select programmed information is the same as that given for the corresponding switches described in the preceding paragraph. If, after the program is stored, the bit synchronizer is momentarily turned off, the program must again be strobed into the bit synchronizer. The BIT RATE, SOURCE, POLARITY and LOOP displays provide information as input by the program, and the displayed information will not necessarily agree with the corresponding front panel control.

d. Set CLOCK and TERMINATION switches as instructed in steps b, c and d of the preceding paragraph.

e. Follow instructions given in steps i, j and k of the preceding paragraph. Operation of RESET pushbutton does not affect the stored program.

3.3.4 Manually Updating Programmed Parameters

Any of the programmed parameters (bit rate, polarity, source, code and loop band) may be changed by using the front panel controls. Once changed, the new data remains in the storage registers until a new program is input, the MANUAL/PROGRAM switch is placed in MANUAL position, or the bit synchronizer is turned off. To change any of the programmed parameters, proceed as follows:

a. Set override function switch to the type of parameter to be changed. As an example, if the bit rate is to be changed, set override switch to BIT RATE position.

b. Set the parameter switch (POLARITY, SOURCE, CODE or LOOP BAND) or BIT RATE thumbwheels to the position corresponding to the updated information. As a continuation of the previous example, suppose the bit rate is to be changed from the programmed value to 2 Kbps, set BIT RATE thumbwheels to 2.000×10^3.

c. Depress OVERRIDE pushbutton. BIT RATE displays provide the updated bit rate.

d. Return override function switch to OFF position as a safeguard in case the OVERRIDE pushbutton is accidently depressed.

3.4 SHUTDOWN PROCEDURE

Set POWER switch to OFF position. If the bit synchronizer was operating in the program mode, see paragraph 3.3.3.

3.5 EMERGENCY OPERATING PROCEDURES

Some portions of the bit synchronizer circuits, if disabled, can be bypassed to keep the equipment in operation until repairs can be effected. Some of the possibilities are as follows:

a. If a malfunction occurs in the source input circuit (INPUT AMPLITUDE meter probably will go into red area), change PCM input cable to an unused input jack, and accordingly change the position of SOURCE switch.

b. If a malfunction occurs in the phase lock loop circuit (LOOP DEVIATION meter deviates from 0 and cannot be corrected by depressing RESET pushbutton), change position of LOOP BAND switch.

c. If a malfunction occurs in the output circuit (PCM or clock not available at output connectors), change the output cable to a connector. This provides a duplicate of the malfunctioning signal, if available.

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section contains the theory of operation for the Model 335 PCM Bit Synchronizer. The information is presented in four levels. The first level is an overall description referenced to a simplified block diagram which identifies the five functional areas of the unit. This description explains the purpose of each functional area and the relationships among the areas. The second level includes breakdowns of the five functional areas into their major sections. This level includes for each of the functional areas a block diagram which identifies each section within it. The third level is the explanation of a series of detailed functional block diagrams representing each section, each of which shows all the circuits within its section. The fourth, and most detailed level, contains the printed circuit card descriptions. On the pc card schematic diagrams (see section VI), parts of all circuits are enclosed by dashed lines and identified by name, which references back to the third level functional descriptions in this section.

4.2 OVERALL FUNCTIONAL DESCRIPTION

The overall functional block diagram of the bit synchronizer is shown in figure 4-1. The number in parenthesis in each block is the figure number of the more detailed functional diagram. Following is a description of the block diagram.

The input processing functional area selects PCM data from one of four input sources. This input data is amplitude and offset normalized, filtered and then threshold detected to produce clean data transitions from the noisy PCM data input. Amplitude and offset information obtained during the processing of the input signal is sent to the program and operational status displays functional area where this information is displayed on the front panel of the equipment. A signal, X LOSS, generated when data transitions are not present, is sent to the phase lock loop (PLL) functional area to optimize the PLL circuits; and via P clock pulses, to optimize the input processing functional area in an effort to recapture the input signal as rapidly as possible. The data transitions are fed to the PLL.

The prime function of the PLL is to provide clock pulses that are synchronized with the incoming PCM data. The bit rate of these clock pulses is determined primarily by front panel controls or is received from an external source. Thus, the bit rate originates within the equipment in the program control functional area. However, the PLL deviates this bit rate to provide clock pulses at precisely the bit rate of the input data. PLL provides VDl which is an analog voltage containing bit rate information, and is used in

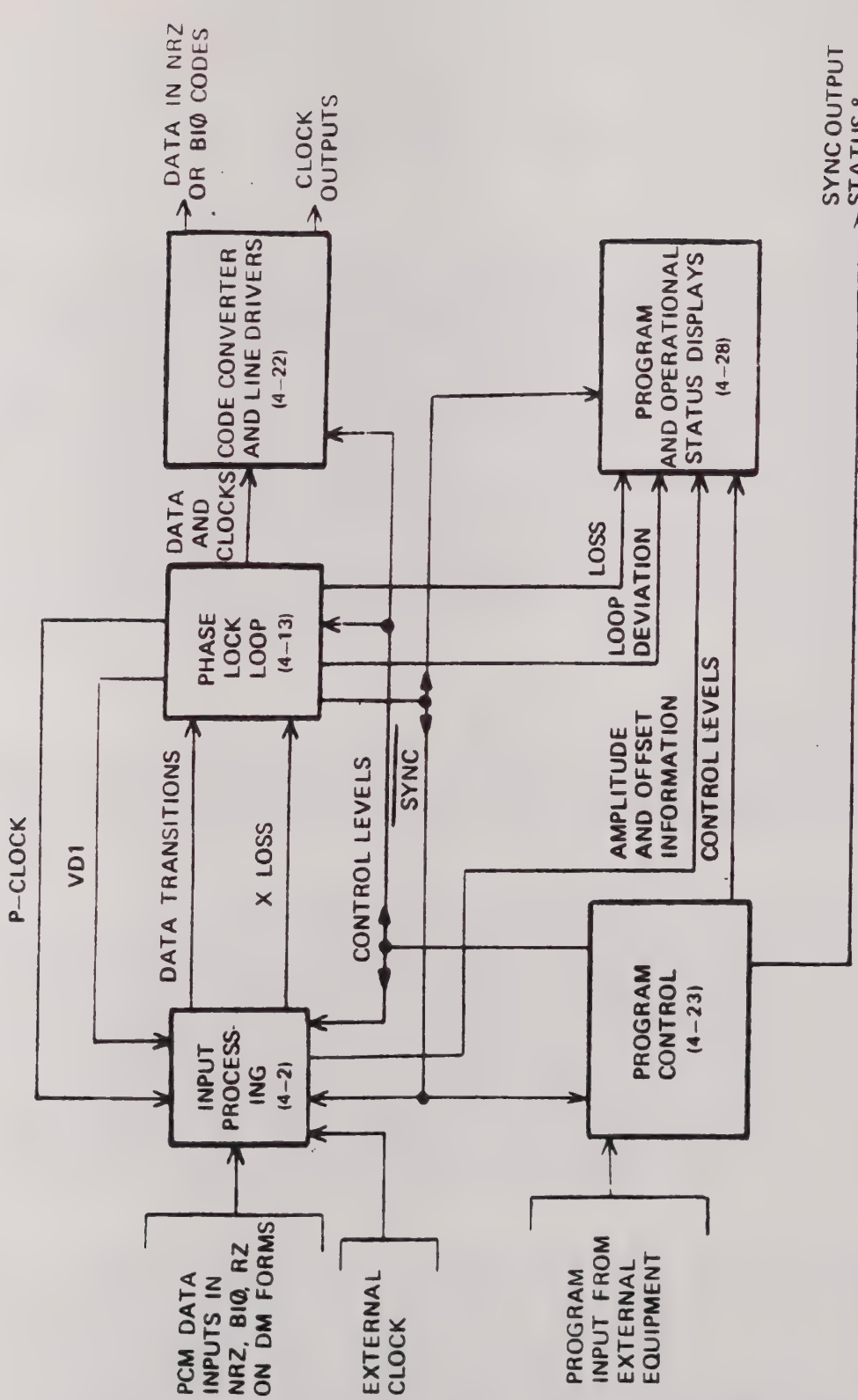


Figure 4-1. Model 335 PCM Bit Synchronizer, Overall Functional Block Diagram

the input processing functional area to provide linear tracking currents during the normalization of the data input. If the data and clock cannot be synchronized, a signal, SYNC, is generated and is routed to input processing and program and operational displays functional areas. In input processing, SYNC reinitiates the normalization process in an effort to reestablish synchronization in the PLL. Also, SYNC, applied to the program and operational status displays, alerts the operator via a front panel indicator that the bit synchronizer has lost synchronization. The sync loss signal is also provided for the operator of external equipment but would be used only when the bit synchronizer is operated under external program control. Three additional clocks, one for each quadrant (90°, 180° and 270°, are generated from the synchronized clock. These clocks, the synchronized 0° clock and the data transitions, are fed to code converter and line drivers functional area.

The code converter and line drivers functional area uses data and four phases of clock to convert the data to NRZ-L and BiØ-L code correctly phased with the four clock outputs. The converted codes and clocks are then available at output connectors. Circuits are provided for these signals to drive 50 ohm terminated lines with levels of 0 to +3 volts. An additional circuit is provided for the BiØ-L signal to drive tape recorders.

The program control functional area receives remote programming information or local programming information, depending on whether the bit synchronizer is operated in the program or local mode of operation. The programming information is stored in registers, decoded and fed to the other functional areas as required. Manual programming information is inserted through the use of front panel controls. When operating in program mode of operation, provisions are made to locally program any or all of the programmed parameters. The programmed parameters that may be locally programmed include bit rate, loop, source, code and polarity. The bit rate, any value between 1.000×10^0 to 4.999×10^6 bps (or, optionally, to 9.999×10^6 bps), sets the bit rate about which the clock pulses are tracked; it is set to the bit rate of the input data. Loop selects one of four available bandwidths in the clock tracking circuit. Source selects one of four input PCM sources as available at the four input connectors. Code selects the one of nine type codes and must agree with the code of the selected input. Code also selects the code output at the tape recorder and data out connectors. Polarity selects either + or - to provide the output signals in their true or complement forms.

The program and operational status displays functional area includes all front panel indicators and meters. These indicators display the contents of the storage registers in the program control functional area and give indications when sync or input signal is lost, and when offset exceeds the maximum limit acceptable to the bit synchronizer (100 percent). In addition, one green lamp is provided that indicates, when lit, that the synchronizer is synchronized with the incoming data and is operating normally. The two meters provide an indication of the incoming signal amplitude and the amount of deviation between the programmed bit rate and the synchronized bit rate. A lamp test circuit is incorporated.

4.3 INPUT PROCESSING FUNCTIONAL AREA

The sections of input processing functional area are shown in figure 4-2 and explained in the following paragraphs. After the description of this functional area, each section of this functional area is explained in more detail. For ease of reference, each block in figure 4-2 contains the figure number of its detailed block diagram.

The input select section, under the command of the program control, selects PCM data from one of four inputs. The input signal may be terminated into 50 ohms or 10,000 ohms by means of a HIGH-LOW TERMINATION switch located on the rear panel. The signal selected is fed to the variable gain and offset amplifier section. The selected input signal can be monitored at one-third amplitude at the IN test point located on the front panel.

The variable gain and offset amplifier section is controlled by the HF/AGC and offset control section when the bit rate of the incoming PCM is 1×10^4 bps or greater and is controlled by the LF AGC and offset control section when the bit rate of the incoming PCM is less than 1×10^4 bps. The output of the variable gain and offset amplifier section is a reproduction of the input PCM signal that has been gain and offset normalized. This output signal, depending on the bit rate, is routed to either the HF or LF tracking filter.

The HF and LF matched filters are similar to each other in function; they differ only in method of implementation due to frequency differences. In each matched filter section the input signal is subjected to a four part filter from which selected outputs are obtained and summed to provide signals identified as HF (or LF) - NRZ - MF and HF (or LF) - SØ - MF. Essentially, the NRZ signal provides a means of locating the center of the bit period and the SØ signal provides a means of determining and controlling the amplitude of the PCM data.

The HF and LF threshold detectors also are similar to each other in function; they differ only in method of implementation due to frequency differences. In each threshold detector, the two filter outputs are selectively combined to provide data transitions and correction signals. The data transitions are transferred to the phase lock loop functional area for further processing. The correction signals, HF (or LF) 3/4T and HF (or LF) 1/2T, are returned to their appropriate AGC and offset control section where they are used to normalize the output signal. The data transitions from the low frequency threshold detector section are processed through the high frequency threshold detector section before being sent to the phase lock loop.

Spill detector and transition loss delay generator section provides SPILL if data transitions are not detected within 128 clock periods when SYNC is not present, or when SYNC is present and data transitions

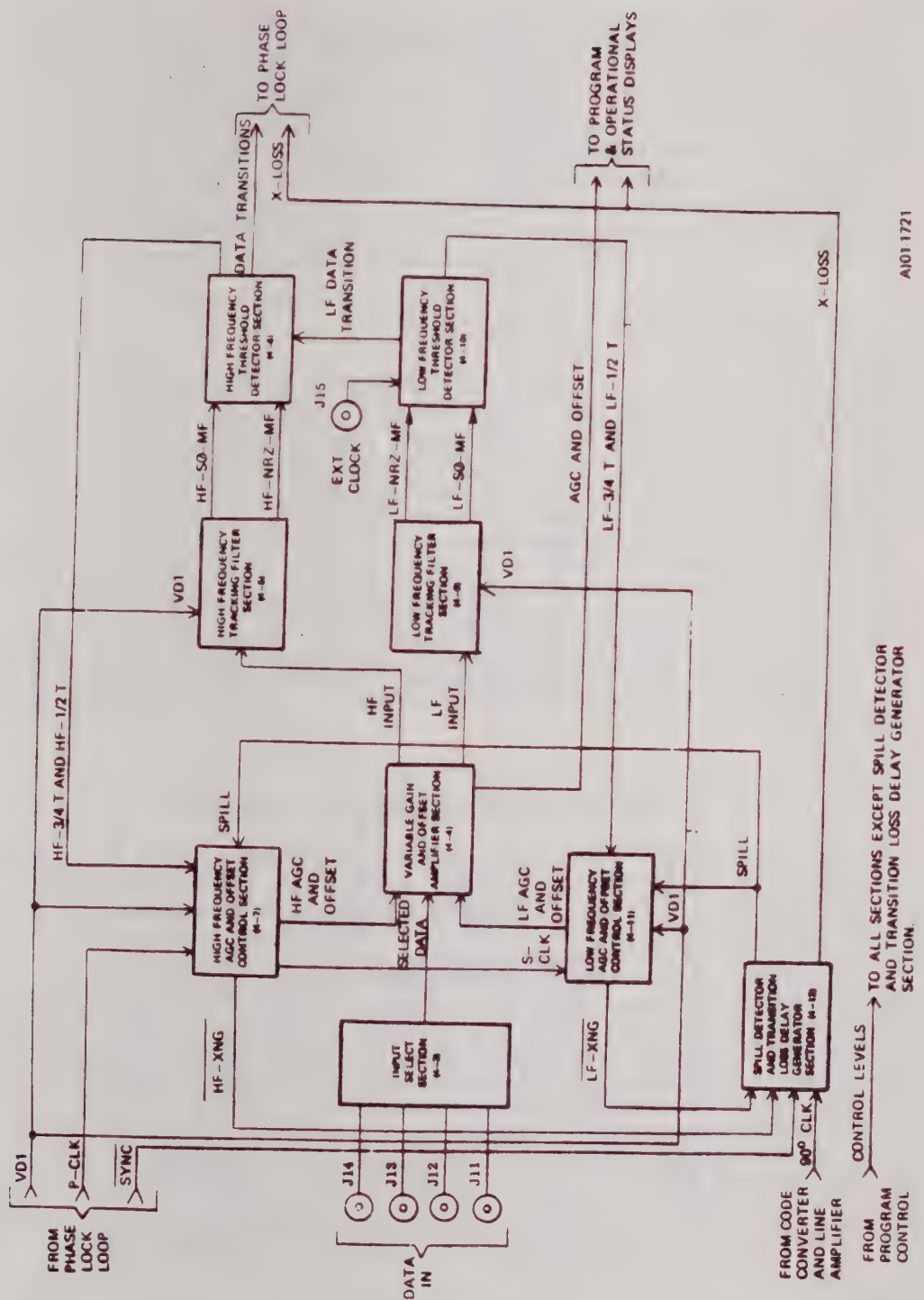


Figure 4-2. Input Processing, Functional Block Diagram

are not detected within 2048 clock periods. Data transitions are monitored via the HF-XNG and LF-XNG signals. Condition of the synchronization process is monitored via SYNC. The 90 degree clock pulses are used to provide the clock periods. SPILL, a 50-nanosecond positive-going pulse, is transferred to the high and low frequency AGC and offset control sections where it reinitiates the normalizing process. SPILL also causes X-LOSS to be generated which remains high for at least eight clock periods and then continues to remain high until data transitions are detected. X-LOSS is transferred to the phase lock loop and also to the program and operational status displays.

4.3.1 Input Select Section

The input select section (see figure 4-3) includes input signal select, termination select and ac/dc select circuits. The input signal select circuit chooses one of four input signals which are connected to BNC jacks J11-J14 on the rear panel. The desired input signal is selected by inputs IB1 and IB2 from program control functional area. The selected signal is applied through the termination select circuit where the signal line is terminated in 50 or 10,000 ohms depending on whether TERMINATION switch S18 is in LOW or HIGH position respectively. The selected signal is then applied through the ac/dc coupling select circuit. When the data code is BiØ at a bit rate greater than 1×10^4, the coupling select circuit ac couples the signal to the variable gain and offset amplifier. For all other combinations of bit rate and code the signal is dc coupled to the variable gain and offset amplifier.

4.3.2 Variable Gain and Offset Amplifier Section

The Variable Gain and Offset Amplifier (see figure 4-4) compensates for variations in amplitude and offset of the input signal. The incoming signal, SIG IN, from the input select section is fed to the test point driver and the variable gain amplifier. The output of the test point driver is fed to the IN test point (TP1) on the front panel. The variable gain amplifier changes gain in response to the applied AGC feedback voltage from the LF/HF AGC select circuit to maintain the amplifier output signal at a constant amplitude. Inputs to LF/HF AGC select circuit are the LF AGC/V and HF AGC/V signals from the low frequency and the high frequency AGC and offset control sections, respectively. The output of the LF/HF AGC select circuit is controlled by the DEC 4 input from the program control section. The gain-normalized output signal is fed through a polarity I (current) switch to the offset I correction circuit. The switch circuit, controlled by POL +/- input from the program control section, allows changing the polarity of the output signal, polarity I (current).

Offset feedback voltage from the LF/HF offset select circuit is applied to the offset I (current) correction circuit to maintain the offset of the output signal at zero, despite variations in the offset of the input signal. The offset feedback voltage is derived from LF OFST/V and HF OFST/V signals produced in the low and the high frequency AGC and offset control sections, respectively.

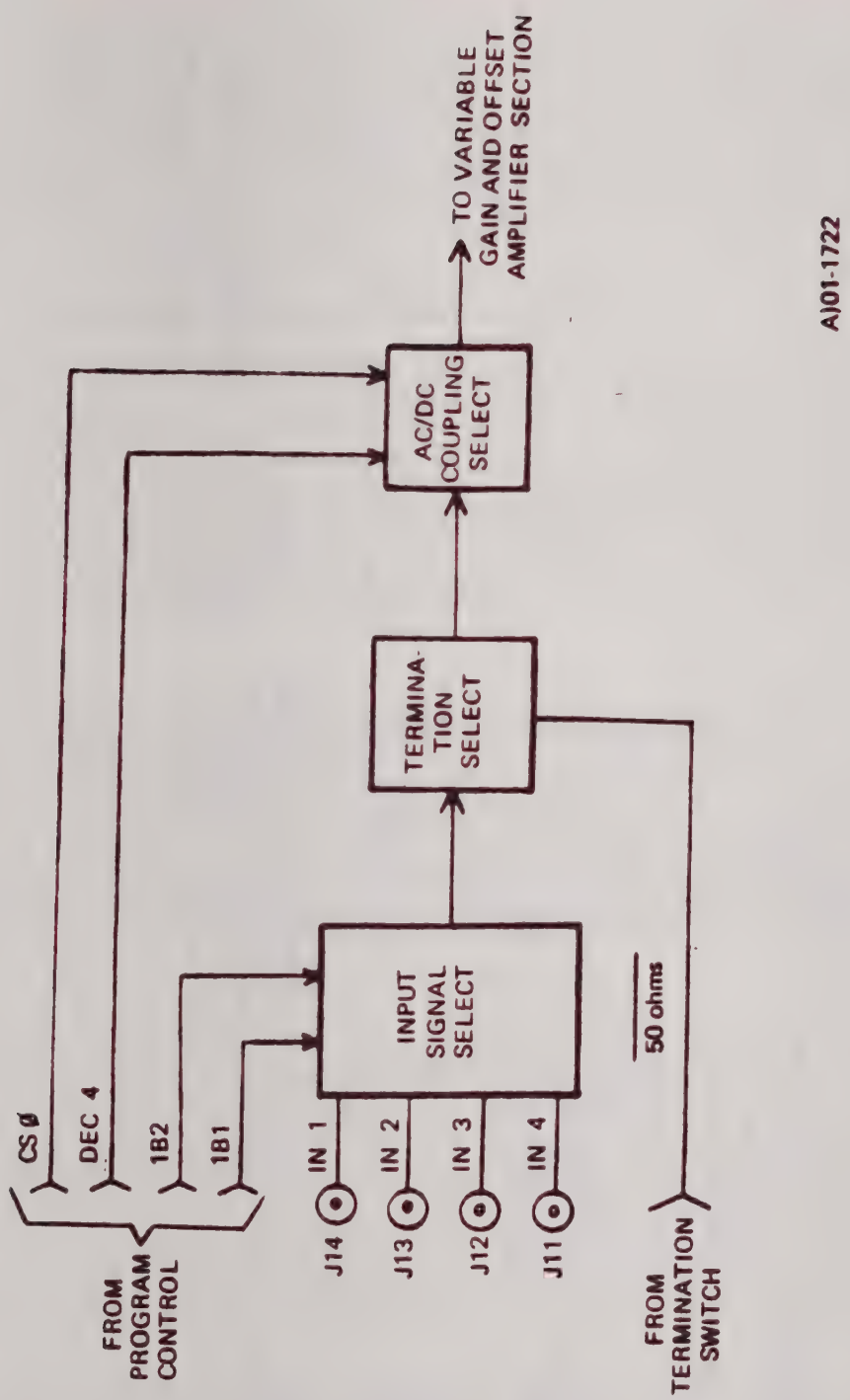


Figure 4-3. Input Select Section, Detailed Functional Block Diagram

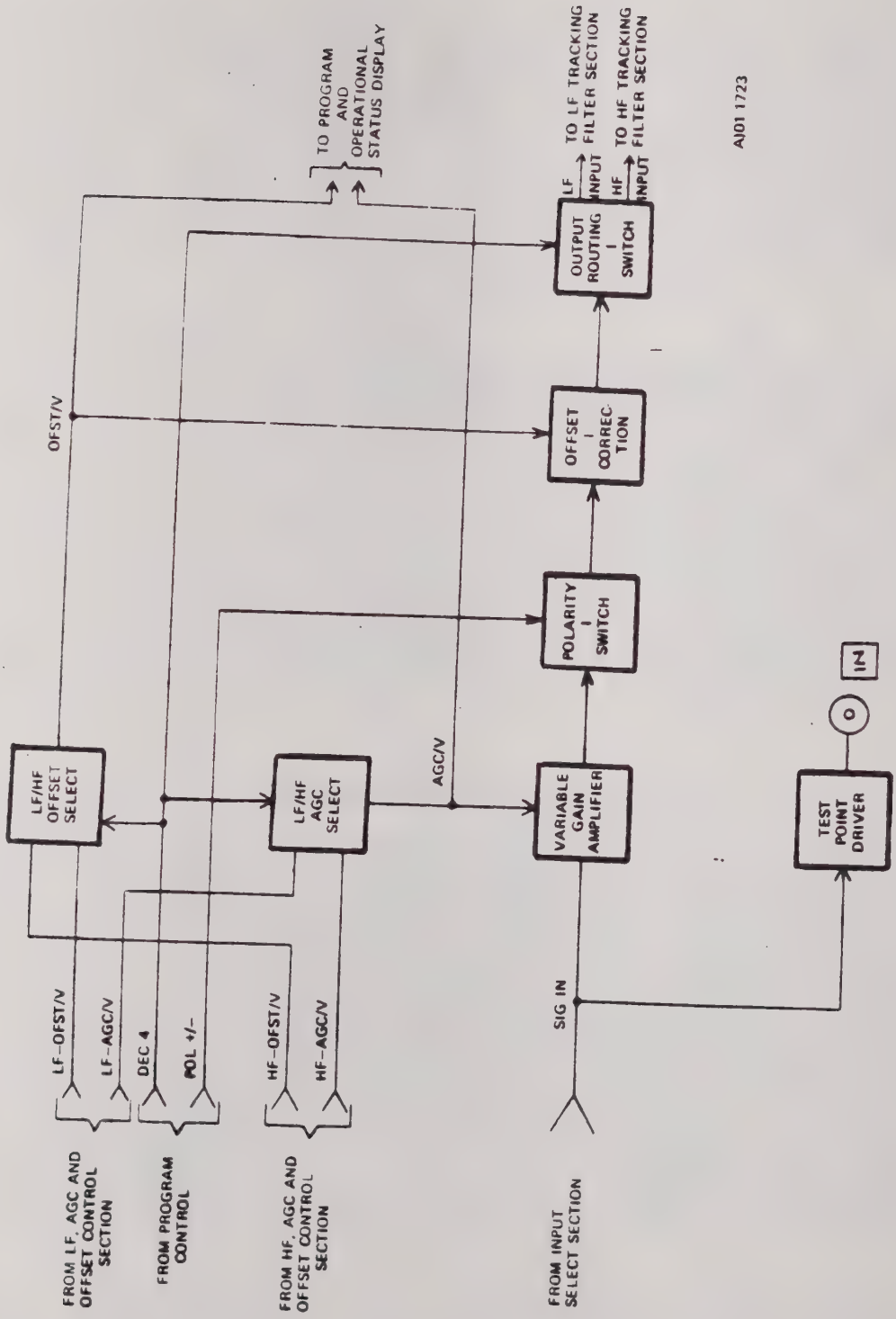


Figure 4-4. Variable Gain and Offset Amplifier Section, Detailed Functional Block Diagram

The gain and offset stabilized signal is fed to the output routing I (current) switch, which is controlled by the DEC 4 signal. If the output signal has bit rates of 1×10^4 bps or more (high frequency), the output routing I (current) switch directs HF INPUT to the high frequency tracking filter section; if the output signal has bit rates less than 1×10^4 bps (low frequency), the output routing I (current) switch directs LF INPUT to the low frequency tracking filter section. Signals AGC/V and OFST/V also are fed to the program and operational status displays functional area.

4.3.3 High Frequency Tracking Filter Section

Basically, the section contains a series of filters identified as Q, R, S, and T (see figure 4-5). Each filter is a frequency compensated amplifier which has its compensating parts automatically changed as the bit rate is changed; the values of other frequency-compensating parts are automatically varied in accordance with the bit rate within a decade range. The outputs of the filters are individually summed to produce HF-SØ-MF and HF-NRZ-MF. The line receiver receives the HF INPUT signal from the variable gain and offset amplifier section and provides, through the buffer, the driving current necessary for the Q filter.

Levels DEC 1 and DEC 2 select from programming control, via relays, the R-to-Q feedback capacitors and the T-to-S feedback capacitors. In addition, DEC 1 and DEC 2 also select the proper bypass capacitors for the input circuits of the Q and S filters. Thus, these signals change the bandpass characteristics of the filters to provide the desired output for each decade range. Because the high frequency tracking filter section processes bit rates of 1×10^4 bps and higher, it is not necessary to decode DEC 4 in the capacitor decode control to select bit ranges of 10^4, 10^5 and 10^6.

Raysistor control circuit and the individual raysistor drivers control the value of a resistive element in the input circuit of each filter. This resistive element changes the bandwidth of each filter in accordance with the bit rate within each decade of the PCM signal being processed. The bit rate information is contained in VD1 from the phase lock loop. VD1 is an analog voltage proportional to the bit rate within the decade. To improve tracking, MSD 8 and MSD 4 from program control are decoded to send the VD1 signal as VD1 ($\leq 3.999 \times 10^4$) or as VD1 ($\geq 4.000 \times 10^4$) to its respective input of each Raysistor driver. The level of the -6.2 volt reference level from the phase lock loop is changed to a +2 volt level and applied to each Raysistor driver.

Selected outputs from the filters are summed in the HF-SØ-MF and HF-NRZ-MF summing amplifiers which transfer their respective output signals to the high frequency threshold detector section. For a normalized HF INPUT signal, HF-SØ-MF output provides the following output. For a positive-going input transition, the output is a positive-going ramp that starts at zero volts, peaks at +1 volt at the center of the

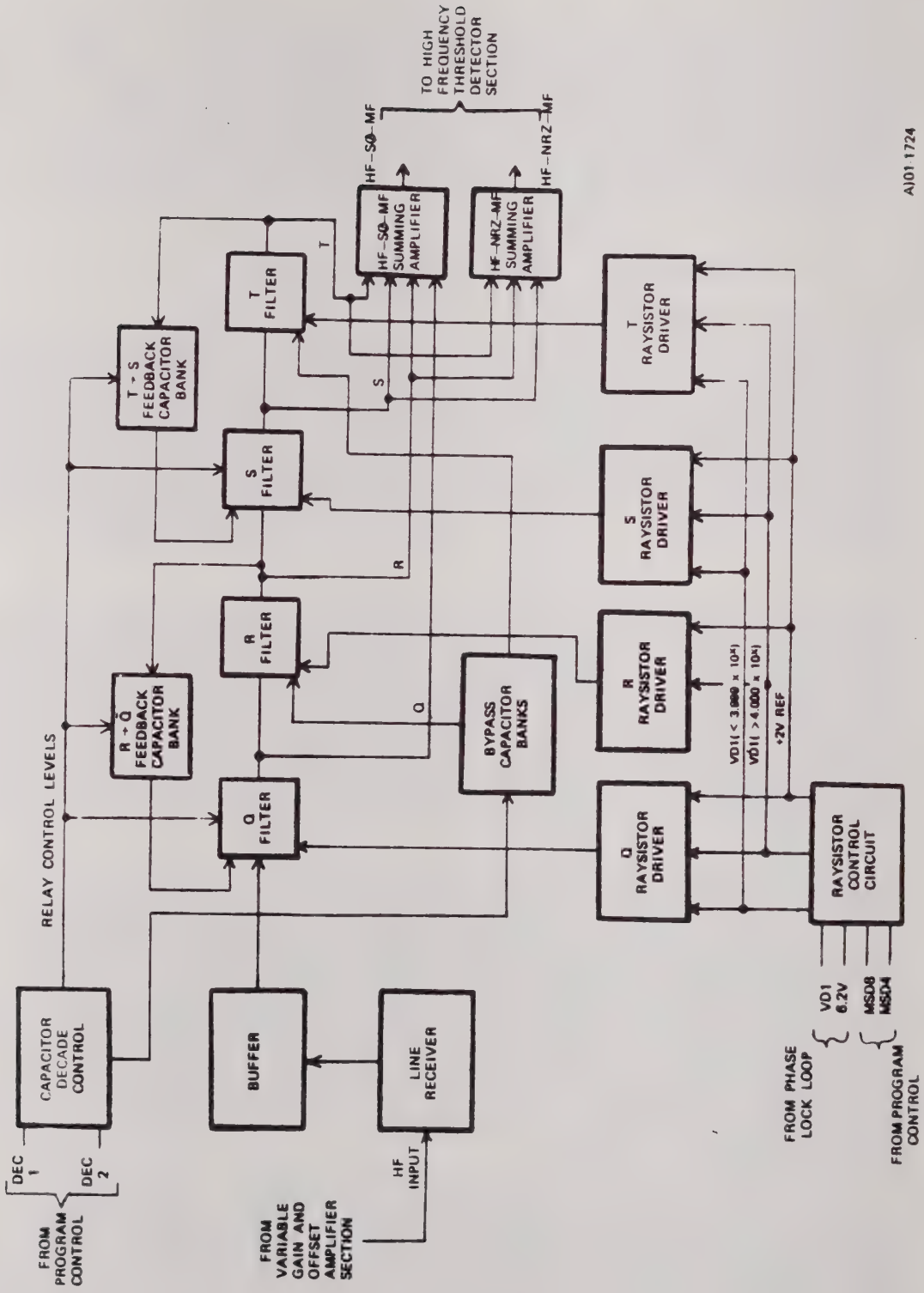


Figure 4-5. High Frequency Tracking Filter Section, Detailed Functional Block Diagram

bit time and then returns with a negative-going range to zero volts at the end of a bit period. An input negative-going transition causes the output waveform to duplicate that for a positive-going transition, but the initial range is negative-going to -1 volt. This waveshape and the HF-NRZ-MF are shown (figure 4-8) and explained in the high frequency AGC and offset control section (paragraph 4.3.5). For a normalized HF INPUT signal, HF-NRZ-MF output provides the following output. For a positive-going input transition, the output is a positive-going ramp that starts at -1 volt, and goes to +1 volt at the end of the bit period. A negative-going input transition causes a negative-going ramp that starts at +1 volt and goes to a -1 volt at the end of one bit period. For either output, if there is no transition after the end of the bit period described above, the output waveshape remains at the voltage level obtained at the end of the bit period. Thus, HF-NRZ-MF is +1 or -1 volt, depending on whether the previous transition was positive-going or negative-going, respectively; the HF-SØ-MF is at zero volts.

The significant properties of the HF-SØ-MF and HF-NRZ-MF waveshapes are as follows. For an AGC normalized input signal, HF-SØ-MF peaks at +1 volt or -1 volt at the center of the bit period which started with a positive-going or negative-going transition, respectively. If the input signal is below its normalized amplitude, the positive and negative peaks occur in the center of the bit period but at a lower absolute voltage value. Conversely, if the input signal is above its normalized amplitude, the positive and negative peaks occur in the center of the bit period but at a higher absolute voltage value. It is the value of these peaks for which the AGC correction voltage is developed.

For an offset normalized input signal, HF-NRZ-MF has a zero crossing at the center of any bit period which started with a positive-going or negative-going transition. If the input signal has a positive offset, the zero crossing for a positive-going ramp occurs sooner than the center of the bit period and, conversely, if the input signal has a negative offset, the zero crossing for a positive-going ramp occurs after the center of the bit period. Negative input transitions cause the opposite effect, that is, a positive offset causes the zero crossing to occur later and a negative offset causes the zero crossing to occur sooner than the center of the bit period. It is the time in which these zero crossings occur from which the offset correction voltage is developed.

4.3.4 High Frequency Threshold Detector Section

The high frequency threshold detector section (see figure 4-6) contains comparators, mixers, and drivers, along with receiver amplifiers, a control signal gating circuit, a voltage reference generator and a U select circuit. The U pulse is the data transitions; its origin within the high frequency threshold detector depends on the type of PCM data being processed. These U pulses and, under specified conditions the Z and BD pulses, are transferred to the phase lock loop

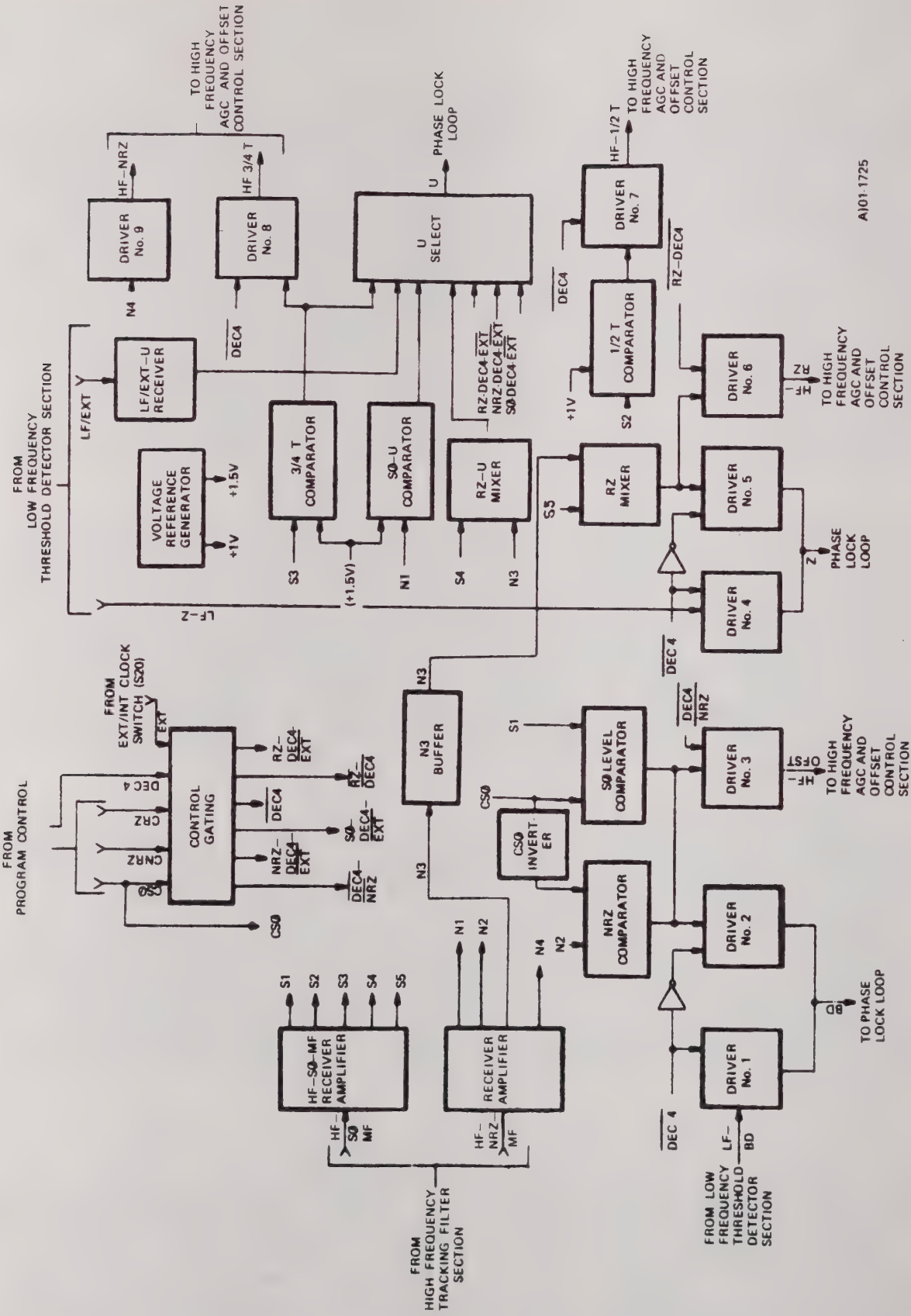


Figure 4-6. High Frequency Threshold Detector Section, Detailed Functional Block Diagram

functional area. The other output signals shown in figure 4-6 are transferred to the high frequency AGC and offset control section where they are used during the signal normalization process.

The HF-SØ-MF and HF-NRZ-MF inputs from the high frequency tracking filter are applied to their respective receiver amplifiers which generate outputs of 2 volts peak-to-peak when the data is normalized. The output of the HF-SØ-MF receivers is split into five isolated signal paths, S1 through S5, that are transferred to the appropriate comparator or mixer. The HF-NRZ-MF generated output is fed to four isolated branches, N1 through N4. These signals are likewise fed to appropriate comparators or mixers, except N4 which goes directly to a driver.

The control gating circuit combines CSØ, CNRZ, CRZ and DEC 4 levels from the program control functional area and the EXT level originating at the INT/EXT clock switch. The CSØ level is also fed directly to a comparator. The combined levels control the operation of comparators and the selection gates, depending on the frequency and type of codes being processed.

The voltage reference generator produces two voltages, a +1 volt reference, which is supplied to the 1/2T comparator, and a +1.5 volt reference, which is supplied to the 3/4T and SØ-U comparators.

For bit rates less than 1×10^4 bps or when in external clock mode, two of the three inputs from the low frequency threshold detector section, LF-BD and LF-Z, are routed through driver No. 1 and driver No. 4, respectively, to outputs BD and Z. The third input, LF/EXT-U, is fed through a receiver to the U select circuit where it is gated to the output by the absence of the three control levels. These three output signals, U, Z, and BD, are fed to the phase lock loop functional area. All other circuits are disabled at this time.

When processing high frequency NRZ or DM type PCM signals, the NRZ· DEC 4· $\overline{\text{EXT}}$ control level gates only the output of the 3/4T comparator through the U select to provide the U pulse. The 3/4T comparator provides pulses whose width is proportional to the amplitude of the S3 signal. The 3/4T also is applied through driver No. 8 to the high frequency AGC and offset control section. In addition, the N2 signal is applied to the NRZ comparator which provides a signal that has a transition for each zero crossing of the N2 signal. The output of the NRZ comparator is applied to drivers No. 2 and No. 3 which, respectively, provide the BD to the phase lock loop and HF-OFST to the high frequency AGC and offset control section. The 1/2T comparator, similar to the 3/4T comparator, also provides pulses through driver No. 7; the width of these pulses is proportional to the amplitude of its input signal. The N4 signal is applied through driver No. 9 to the high frequency AGC and offset control section.

When processing high frequency BiØ type PCM signals, the SØ·DEC 4·$\overline{\text{EXT}}$ control level gates only the output of the SØ-U comparator through the U select to provide the U pulse. In addition, the S1 signal is applied through the SØ comparator and driver No. 2 to provide the BD pulse. Drivers No. 7, No. 8 and No. 9 are enabled to provide their respective signals. When processing high frequency RZ type PCM signals, the RZ·DEC 4·$\overline{\text{EXT}}$ control level gates only the output of the RZ-U mixer through the U select to provide the U pulse. In addition, the S5 and N3 signals are combined in the RZ mixer and then applied through driver No. 6 to provide the HF-RZ signal. Both the RZ mixer and RZ-U mixer combine their input signals to provide a one-half bit period pulse for each positive data transition.

4.3.5 High Frequency AGC and Offset Control Section

The HF AGC and OFST control section (see figure 4-7) generates the AGC and the offset correction voltages, HF AGC/V and HF OFST/V, for the high frequency section of the variable gain and offset amplifier section. It also produces two control signals that are used in this section as well as other sections. One is $\overline{\text{HF-XNG}}$ which indicates the HF threshold detector section is processing PCM signal; it is routed to the spill detector section and transition loss delay section; the other is S-CLK, a buffered P-CLK, used in the low frequency AGC and offset control section.

The HF AGC and OFST control section is enabled only when PCM signals with bit rates of 1×10^4 bps and up, are being processed. The DEC 4 input from program control applied to the dump and overload detectors enables the section. VD1 from the digital-to-analog converter section in the phase lock loop is fed to voltage-to-current converter and is converted to tracking currents +IDA, -2IDA, +2IDO, -2IDO, and -IDO. Because VD1 is a voltage proportional to the bit rate between 0.000 and 9.999 bps within each decade (power of ten), the tracking currents increase in value as the bit rate increases. The HF AGC generator uses +IDA and -2IDA; the HF offset generator uses +2IDO and -2IDO; and SØ correction circuit uses -IDO. Two signals, a HF-1/2T pulse and a HF-3/4T pulse, which contain the PCM amplitude information, are received from the high frequency threshold detector section and are coupled through their respective line receivers to drive the 1/2T and 3/4T inputs for the HF AGC generator. The acquisition switch uses both of these pulses; the RZ offset safety circuit uses only the 1/2T pulses. The HF-3/4T pulse also produces the $\overline{\text{HF-XNG}}$ signal which is applied to the spill detector and the transition loss delay generator section and the acquisition switch within this section.

In the HF AGC generator, 1/2T gates the +IDA current on and off, and 3/4T input gates the -2IDA current on and off. The two gated currents are summed and thus generate HF AGC/V. The DEC 1 and DEC 2 inputs from the program control section aid the VD1 signal in providing tracking currents that are linear with the bit rate; however, unlike

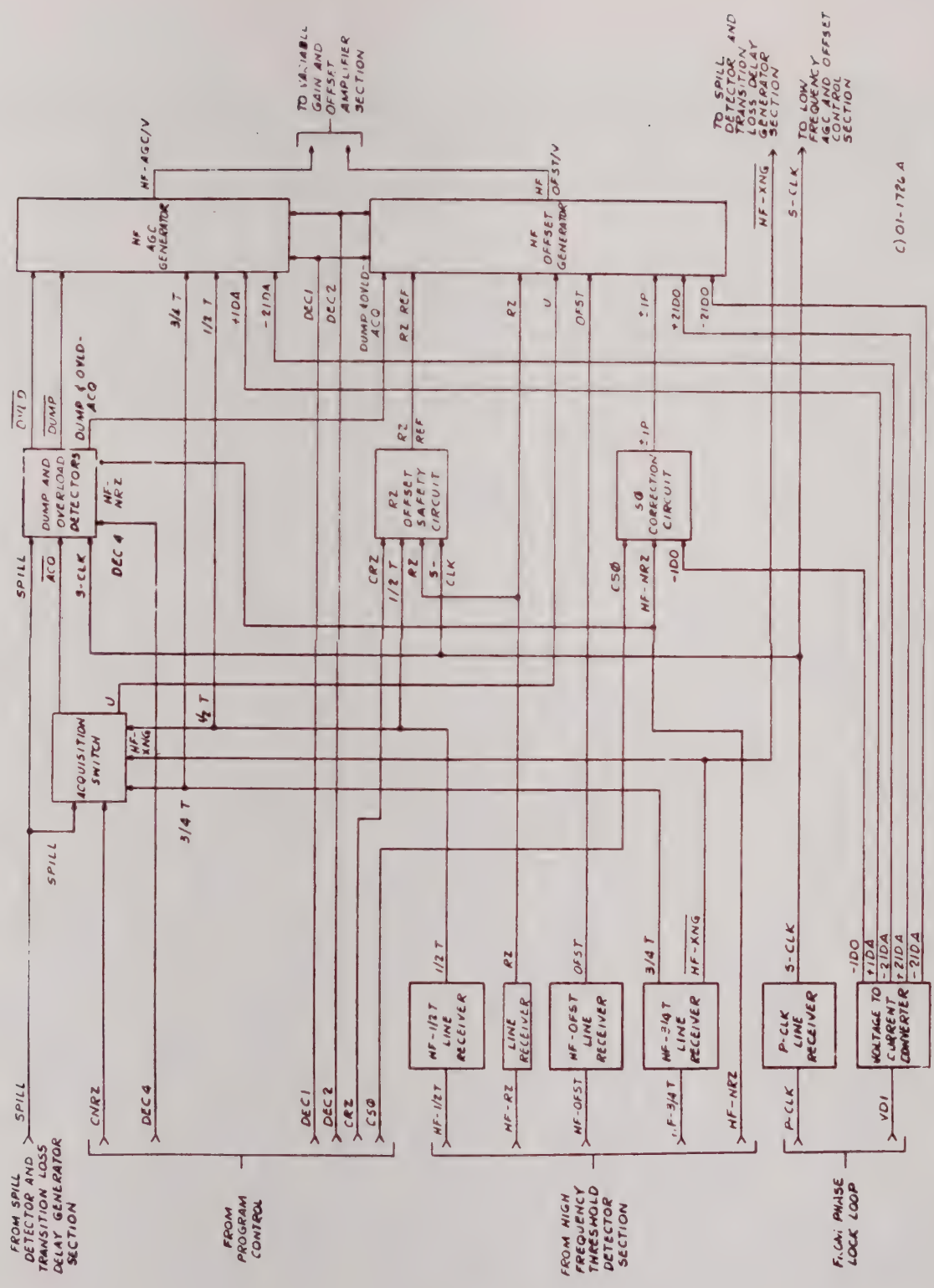


Figure 4-7. High Frequency AGC and Offset Control Section, Detailed Functional Block Diagram

VD1, DEC 1 and DEC 2 provide a course adjustment in the three decade ranges of 10^4, 10^5 and 10^6. Should the data from the variable gain and offset (VG and OFST) amplifier section increase in amplitude, the 3/4T pulse increases in width faster than that of the 1/2T pulse. This results in the development of a more negative AGC voltage, HF-AGC/V, which is fed back to the VG and OFST amplifier section to reduce its gain until the 3/4T pulse is one-half the width of the 1/2T pulse. When this occurs, the amplitude of the data output of the VG and OFST amplifier is normalized. If the data input decreases in amplitude, the width of the 3/4T pulse is reduced faster than that of the 1/2T pulse. Under these conditions, a more positive HF-AGC/V feedback voltage is developed, thus increasing the gain of the VG and OFST amplifier until the 3/4T pulse width is one-half the width of the 1/2T pulse. At this point the amplitude of the VG and OFST amplifier output is again normalized.

Operation of the HF offset generator depends on whether NRZ (or DM), SØ or RZ type PCM signals are being processed. The DM type signals are processed in the same manner as the NRZ signals except the clock pulse rate is doubled for the DM type signals. When processing NRZ (or DM) type PCM signals, the CNRZ signal from program control section enables the acquisition switch, which is also controlled by SPILL from the spill detector and transition loss delay generator section and HF-XNG generated in the 3/4T line receiver. This circuit specifies whether or not the bit synchronizer is in acquisition mode. The HF-XNG signal generates ACQ level which is combined with the 3/4T pulses to provide relatively narrow µH pulses which are commonly referred to as narrow windows. If a SPILL level is received, ACQ level is generated and combined with the 1/2T pulses to provide relatively wide µH pulses which are commonly referred to as wide windows. The relatively wide µH pulses continue until zero crossings are again detected, at which time HF XNG generates the ACQ level. These µH pulses are applied to the HF offset generator. The HF OFST signal, which is generated in the high frequency threshold detector section from PCM data signal zero crossings, also is fed to the HF offset generator through its line receiver. Within the HF offset generator, HF OFST is ANDed with µH and gates the +2IDO current on and off, and HF OFST is ANDed with µH and gates the -2IDO current on and off. The two gated currents are summed and thus generate the output signal HF OFST/V. The DEC 1 and DEC 2 signals applied to HF offset generator affect HF OFST/V in the same manner as they affect HF AGC/V of the HF AGC generator described in the preceding paragraph. If the offset of the data output from the VG and OFST amplifier section goes positive, the transition edges of the HF OFST signal occur sooner than those of a normalized signal. This causes the +2IDO pulses to become wider and the -2IDO pulses to become narrower. As a result, the HF OFST/V signal to the VG and OFST amplifier section goes increasingly positive to correct the offset condition until the +2IDO and -2IDO pulses are again equal in width. When this occurs, the output of the VG and OFST amplifier section is offset normalized. When the offset is negative, the transition edges of the HF OFST signal occur later than those of a normalized signal. This causes

the -2IDO pulses to become wider and the +2IDO pulses to become narrower. As a result, the HF OFST/V signal to the VG and OFST amplifier section goes increasingly negative to correct the offset condition until the +2IDO and -2IDO pulses are again equal in width and the output of the VG and OFST amplifier section is offset normalized.

When processing SØ type PCM signals, the +2IDO and -2IDO tracking current circuits are disabled, and the SØ correction circuit is enabled by the CSØ input from the program control section. The HF-NRZ input from the high frequency threshold detector section is fed to the SØ correction circuit. In this circuit the dc offset of the HF-NRZ is averaged and a bipolar current, +I and -I, for positive and negative offset, is generated. The +I and -I currents are fed to the HF offset generator where they are summed and thus generate HF OFST/V. The DEC 1 and DEC 2 inputs from program control section also offset the amplitude of HF OFST/V. HF OFST/V is fed back to the VG and OFST amplifier which provides the correction necessary to provide offset normalized output signal.

When processing RZ type PCM signals, the H signal from the acquisition switch and the ±I signal from the SØ correction circuit are not present. Instead, the HF RZ signal from the HF threshold detector is applied through the HF RZ line receiver to the RZ offset safety circuit where RZ, 1/2T, and S CLK generate the RZ REF pulse which is always 1/2-bit wide. The CRZ level from program control enables the RZ offset safety circuit. Within the HF offset generator, the HF RZ signal controls the length of time that +2IDO current is present. The RZ REF pulse, which is always one-half bit-time wide and occurs coincidentally with the positive-going edge of the HF RZ signal, controls the length of time that -2IDO current is present. When no offset condition exists, the HF RZ signal, for each ONE of data, has a positive-going pulse that is one-half bit-time wide. Because the HF RZ pulse has the same width and is coincident with the RZ REF signal, the summed circuits (+2IDO and -2IDO) equal zero. If the HF RZ signal has a positive offset, the positive-going pulses are wider than the one-half bit-time width. Thus, when the two currents are summed, the +2IDO is predominant and causes the HF OFST/V signal to go less negative to correct the offset condition within the VG and OFST amplifier. If the HF RZ signal has a negative offset, the positive-going pulses are narrower than the one-half bit-time width. Thus, when the two currents are summed, the -2IDO is predominant and causes the HF OFST/V signal to go more negative to correct the offset condition within the VG and OFST amplifier. If a large negative offset occurs, such that the HF RZ signal is not present at the line receiver and this condition exists for three bit periods, the RZ offset safety circuit generates the RZ REF pulse which causes, via -2IDO current, the HF OFST/V signal to go more negative in an effort to restore the proper offset and recapture the HF RZ signal.

The dump and overload detectors provide $\overline{OVLD}$, $\overline{DUMP}$ and DUMP+OVLD·ACQ. OVLD is generated in response to excessive amplitude of HF NRZ and applied to the HF AGC generator causing the HF AGC/V output to go negative which, in turn, reduces the gain of the VG and OFFSET amplifier section in an effort to eliminate overload condition. The complement of the signal, $\overline{OVLD}$, is used rather than the true signal to facilitate electronic requirements.

DUMP is generated three clock pulses after SPILL is received from the spill detector and transition loss delay generator section. The DUMP pulse, which is the same width as the S CLK, is applied to the HF AGC generator where it cancels the effects of the AGC tracking currents and thereby causes the output of the HF AGC generator to go to approximately zero volts. This output returns the gain of the VG and OFST amplifier section to the middle of its operating range in an effort to recapture zero crossings in the HF threshold detector section. To facilitate electronic requirements, the complement of the signal, $\overline{DUMP}$, is used rather than the true signal.

DUMP+OVLD·ACQ is applied to the HF offset generator where it cancels the effects of the offset tracking currents and thereby causes the output of the HF offset generator to go to approximately zero volts. This output returns the VG and OFST amplifier section to the middle of its offset correction range in an effort to recapture zero crossings in the HF threshold detector section. The OVLD·ACQ portion of DUMP+OVLD·ACQ is generated during overload condition, and when ACQ is received from acquisition switch, ACQ is ANDed with OVLD so the offset correction range is not changed while the acquisition switch is using the wide window to recapture the zero crossings.

Figure 4-8 is a timing diagram showing, in waveform A, data with normalized amplitude and offset correction typical of NRZ PCM data. Waveform B represents the output from the NRZ filter in the HF tracking filter section and waveform C represents the output of the SØ filter in the HF tracking filter section. It should be noted that these filters provide outputs similar to that shown in the diagram when processing any type of PCM data. Waveforms D and E, 3/4T and 1/2T, are obtained from HF threshold detector by detecting waveform C at 3/4 volt level and the 1/2 volt level, respectively. Thus, as the amplitude of waveform C increases, the width of the 3/4T pulse widens more than the 1/2T pulse and, conversely, as the amplitude of waveform C decreases, the width of the 3/4T pulse narrows more than the 1/2T pulse. In other words, when the amplitude of waveform C is increasing, the 3/4T pulse width increases faster than the 1/2T pulse width and when the amplitude of waveform C is decreasing, the 3/4T pulse width decreases faster than the 1/2T pulse width. Waveform F, HF OFST, is derived in the threshold detector section from waveform B by providing a positive transition when waveform B goes through zero volts in a positive direction and a negative transition when waveform B goes through zero volts in a negative direction. When zero crossing of waveform B occurs in the middle of the bit period as shown, the transition of waveform F is as shown.

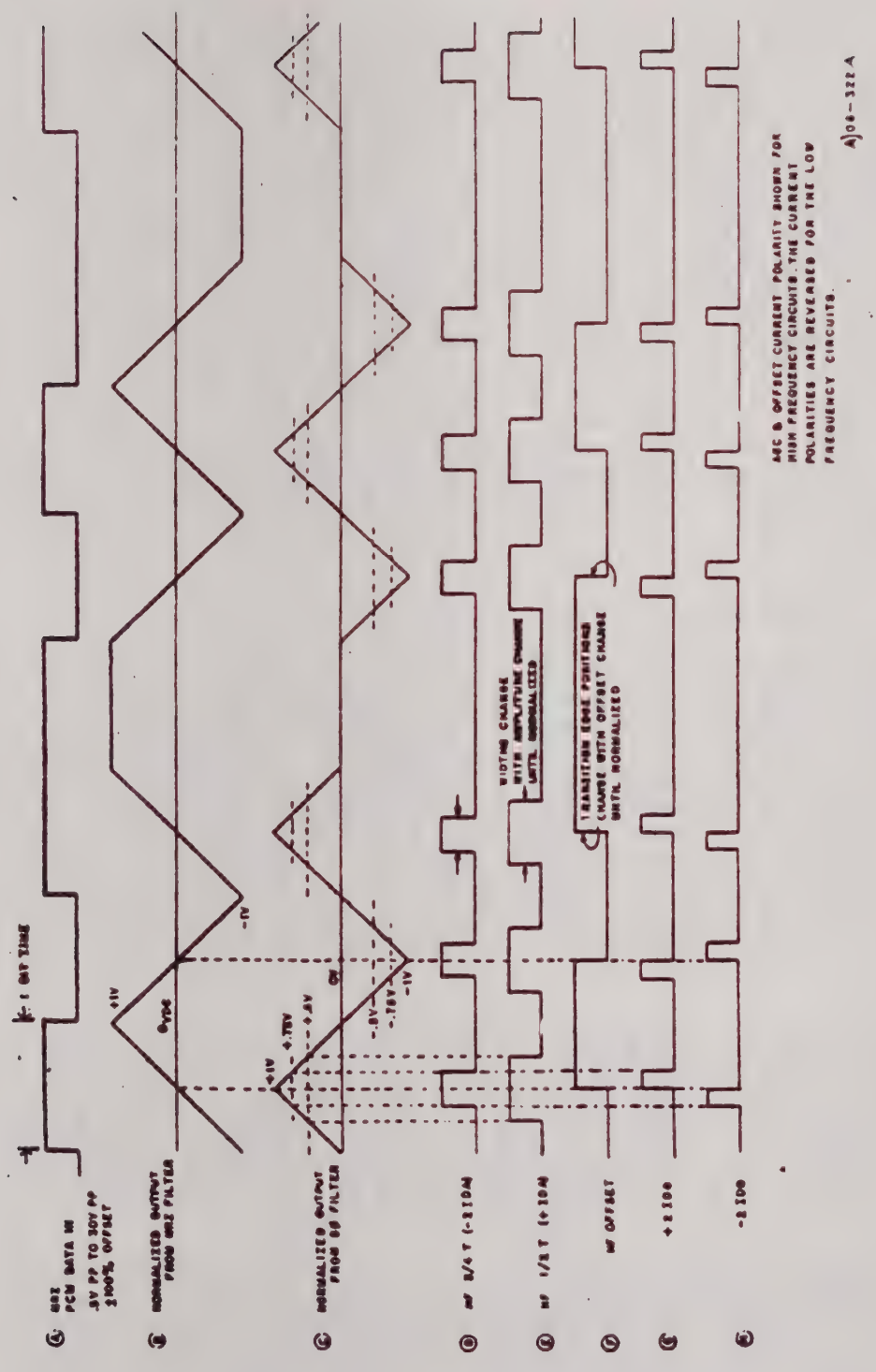


Figure 4-8. Typical Waveforms Produced by Amplitude-and Offset-Normalized NRZ Type PCM Data

If the output of the NRZ filter, waveform B, has a positive offset, the positive and negative transitions of waveform F occur sooner than shown and if the output of the NRZ filter has a negative offset, the positive and negative transitions of waveform F occur later than shown. During normal operation, the 3/4T pulse, waveform D, is gated with OFST, waveform F, to produce +2IDO, waveform G; and $\overline{OFST}$, the complement of waveform F, is gated with the 3/4T pulse to produce -2IDO, waveform H. Thus, when zero volt crossings occur in the middle of the bit period, the +2IDO and -2IDO pulse widths are equal. When a positive offset occurs, the zero crossing occurs sooner than shown in waveform B and causes +2IDO to be wider than shown in waveform G and causes -2IDO to be narrower than shown in waveform H. When a negative offset occurs, the zero crossing occurs later than shown in waveform B and causes +2IDO to be narrower than shown in waveform $\overline{G}$ and causes -2IDO to be wider than shown in waveform F. During $\overline{ACQ}$ time, the +2IDO and -2IDO pulses are obtained in the same manner as just described except the 1/2T pulse is used instead of the 3/4T pulse resulting in wider, but proportional, +2IDO and -2IDO pulses.

4.3.6 Low Frequency Tracking Filter Section

The overall function of the low frequency tracking filter section (see figure 4-9) is identical to that of the high frequency tracking filter section described in paragraph 4.3.3. The description of the two output signals, LF-SØ-MF and LF-NRZ-MF, are the same as that given in paragraph 4.3.3 for the comparable high frequency signals. However, because of lower bit rate frequencies in the low frequency section, the circuits are implemented differently than those in the high frequency section. Rather than rising capacitive feedback circuits as in the high frequency section, this section uses resistive circuits to provide the feedback which changes the bandwidth of the filters in accordance with the bit rate of the signal being processed.

The LF INPUT signal from the variable gain and offset amplifier section is applied through the line receiver to the Q filter. From the Q filter, the signal is fed, in turn, to R, S, and T filters. The outputs of the filters are selectively summed in the LF-SØ-MF and LF-NRZ-MF amplifiers which provide the LF-SØ-MF and LF-NRZ-MF signals for the low frequency threshold detector section.

DEC 1 and DEC 2 signals are decoded in decade control. The resultant control signals change the resistive feedback circuits and other resistive circuits within the filters to provide the proper filter bandwidths for each decade of bit frequencies. Decoding of DEC 1 and DEC 2 provides decade increments of 10^0, 10^1, 10^2 and 10^3.

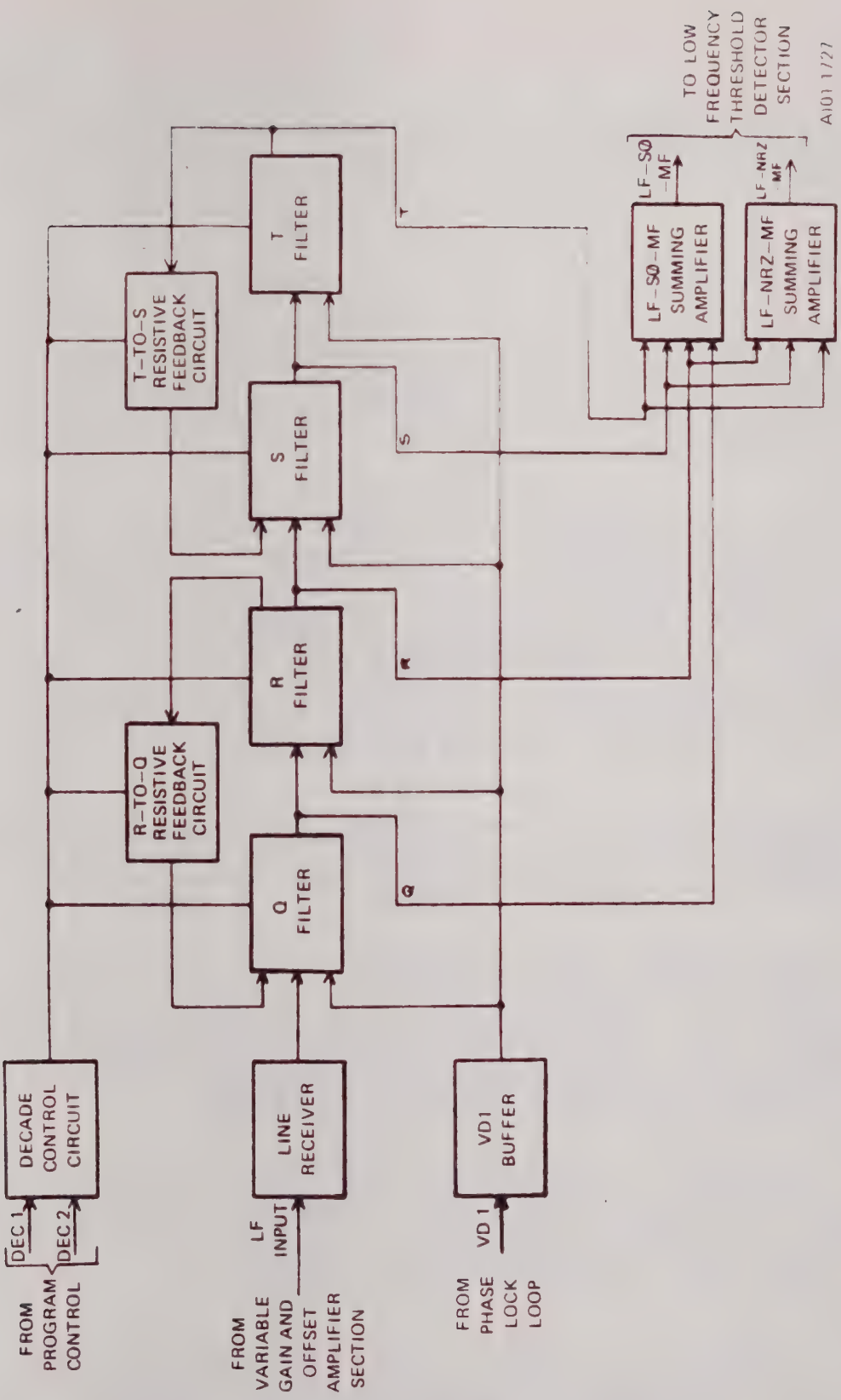


Figure 4-9. Low Frequency Tracking Filter Section, Detailed Functional Block Diagram

VD1 from the phase lock loop is applied through its buffer to each filter and causes relatively minor changes in filter bandwidth to effect complete tracking from the lowest to the highest bit rate processed in the low frequency tracking filter section.

4.3.7 Low Frequency Threshold Detector Section

The low frequency threshold detector section (see figure 4-10) contains a series of comparators and drivers, along with internal/external clock signal selection, a control gating circuit, a voltage reference generator and a level converter. This section is enabled only when PCM signals with bit rates of 9.999×10^3 bps and below are being processed.

The LF-NRZ-MF and LF-SØ-MF inputs, from the low frequency tracking filter section, are applied to their respective receiver amplifiers which generate a 2 volt peak-to-peak output when the data is normalized. The NRZ output is dc coupled, and both are distributed to the offset comparator and the RZ mixer. In addition, the NRZ signal goes to the SØ comparator and the SØ signal goes to the 3/4T and the 1/2T comparators. The voltage reference generator produces +0.5 volts and +0.75 volt used to set the thresholds of the comparators. The +0.75 volt is applied to the 3/4T and SØ comparators; the +0.5 volt is applied to the 1/2T comparator and the RZ comparator.

The control gating circuit combines CNRZ, CSØ, CRZ and DEC 4 levels from the program control functional area. The combined levels control the operation of comparator and select gates according to the frequency of and type of code being processed.

The 3/4T comparator, enabled when $\overline{\text{DEC 4}}$ is high, uses the +0.75 volt and SØ inputs to produce a pulse (3/4T-L) one-quarter of a bit period wide for each data transition when the input signal is normalized. The (3/4T-L) pulse is fed to the 3-way UL select circuit and to driver No. 2. The latter generates the LF-3/4T pulse that is fed to the low frequency AGC and offset control section.

The 1/2T comparator, also enabled when $\overline{\text{DEC 4}}$ is high, generates a pulse (1/2T-L) one-half of a bit period wide for each data transition when the input signal is normalized. The (1/2T-L) pulse is fed to driver No. 1 where the LF-1/2T pulse is generated and then fed to the low frequency AGC and offset control section.

The offset comparator detects the zero crossings of the NRZ or SØ pulses, depending on the code selected, to derive BD-L information which is fed to driver No. 3 and driver No. 4. Driver No. 3 produces LF-BD which is fed to the high frequency threshold detector section. Driver No. 4, which is enabled by SØ2, produces LF-OFST.

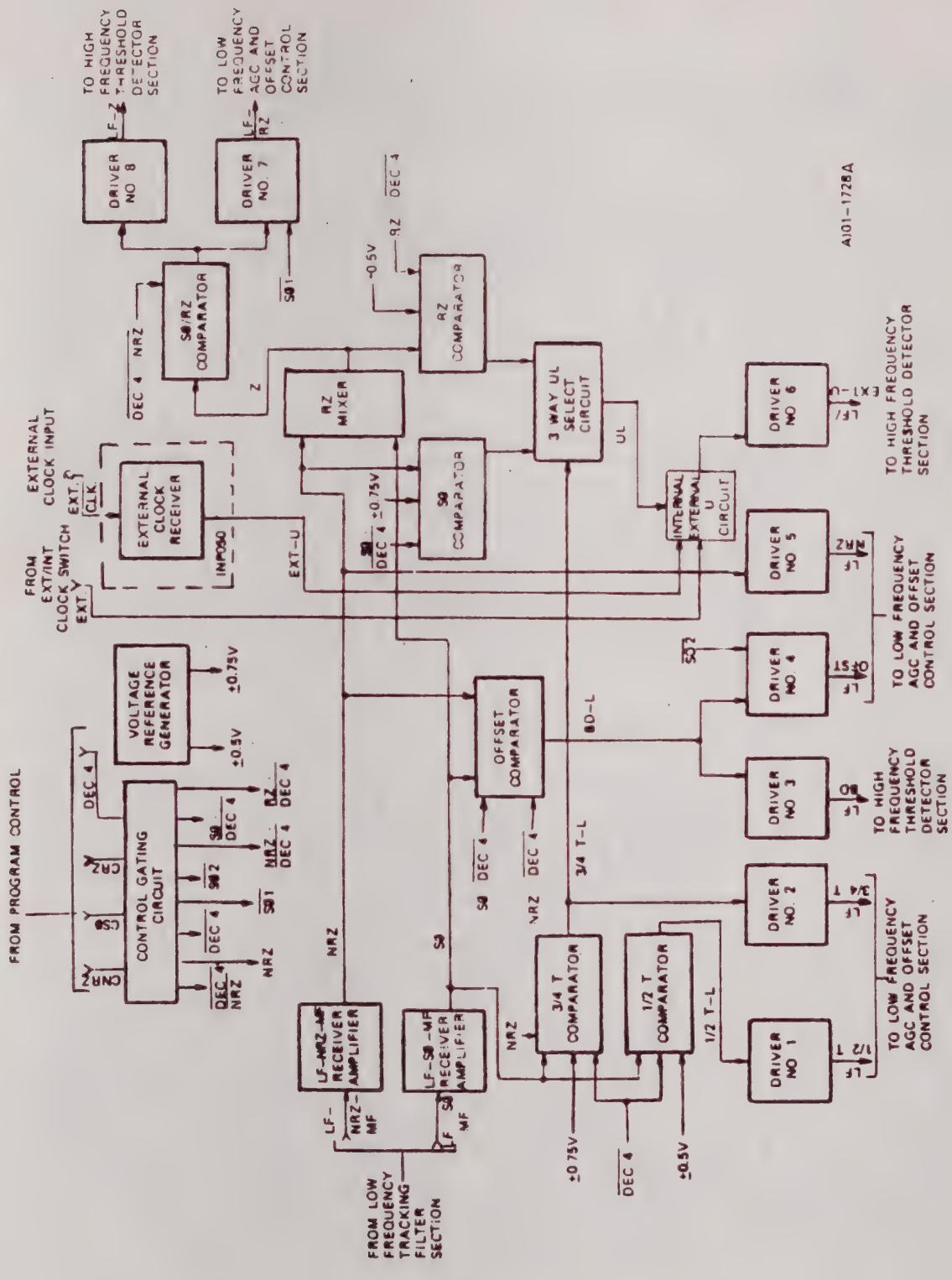


Figure 4-10. Low Frequency Threshold Detector Section, Detailed Functional Block Diagram

The NRZ pulse is also fed to driver No. 5. Both the LF-OFST and LF-NRZ outputs are fed to the low frequency AGC and offset control section.

The RZ mixer combines the NRZ and SØ signals to derive Z which is fed to two comparators, the RZ and the SØ/RZ comparators, enabled when $\overline{\text{DEC 4}}\cdot\text{NRZ}$ is high, detects zero crossings of Z and feeds this signal to driver No. 8 and driver No. 7. The latter, enabled by $\overline{\text{SØ1}}$, produces LF-RZ which is fed to the low frequency AGC and offset control section. Driver No. 8 generates LF-Z which is applied to the high frequency threshold detector section.

The 3-way UL select circuit selects its input from the signals produced by the 3/4T, the SØ or the RZ comparators. The RZ comparator is enabled by $\overline{\text{RZ}\cdot\text{DEC 4}}$ and utilizes the +0.5 volt threshold to derive an output pulse one-half bit period wide for each positive transition. The SØ comparator is enabled by $\overline{\text{SØ}\cdot\text{DEC 4}}$ and uses the ±0.75 volt and NRZ inputs to derive a pulse one-quarter of a bit period wide for each data transition. The 3-way UL select picks the input from the 3/4T comparator when NRZ is high. When NRZ is low, the input from either the SØ or RZ comparator, whichever is enabled, produces the output. The UL signal is applied to driver No. 6.

4.3.8 Low Frequency AGC and Offset Control Section

The LF AGC and OFST control section (see figure 4-11) generates the AGC and the offset correction voltages, LF AGC/V and LF OFST/V, for the low frequency section of the variable gain and offset amplifier section. It also generates the $\overline{\text{LF-XNG}}$ signal for the spill detector and transition loss delay generator section. The LF AGC and OFST control section is enabled only when PCM signals with bit rates less than 1×10^4 bps are being processed. The DEC 4 input from program control enables the section. VD1 from DAC in phase lock loop is applied to the DAC inverter which produces -VD and +VD. These two signals track the VD1 input directly or at one-tenth when the bit rate is set at decade zero by means of the DEC 1 and DEC 2 inputs from program control. -VD and +VD are fed to the LF AGC generator and the LF offset generator; -VD is also fed to the SØ correction circuit. The LF-1/2T and LF-3/4T signals, from the low frequency threshold detector section, are fed through line receivers to derive a 1/2T pulse and a 3/4T pulse. These two pulses are fed to the LF AGC generator and the acquisition switch. The 1/2T pulse, in addition, goes to the RZ offset safety circuit. The 3/4T pulse is also used to derive $\overline{\text{LF-XNG}}$ which is fed to the acquisition switch and to the spill detector and transition loss delay generator section.

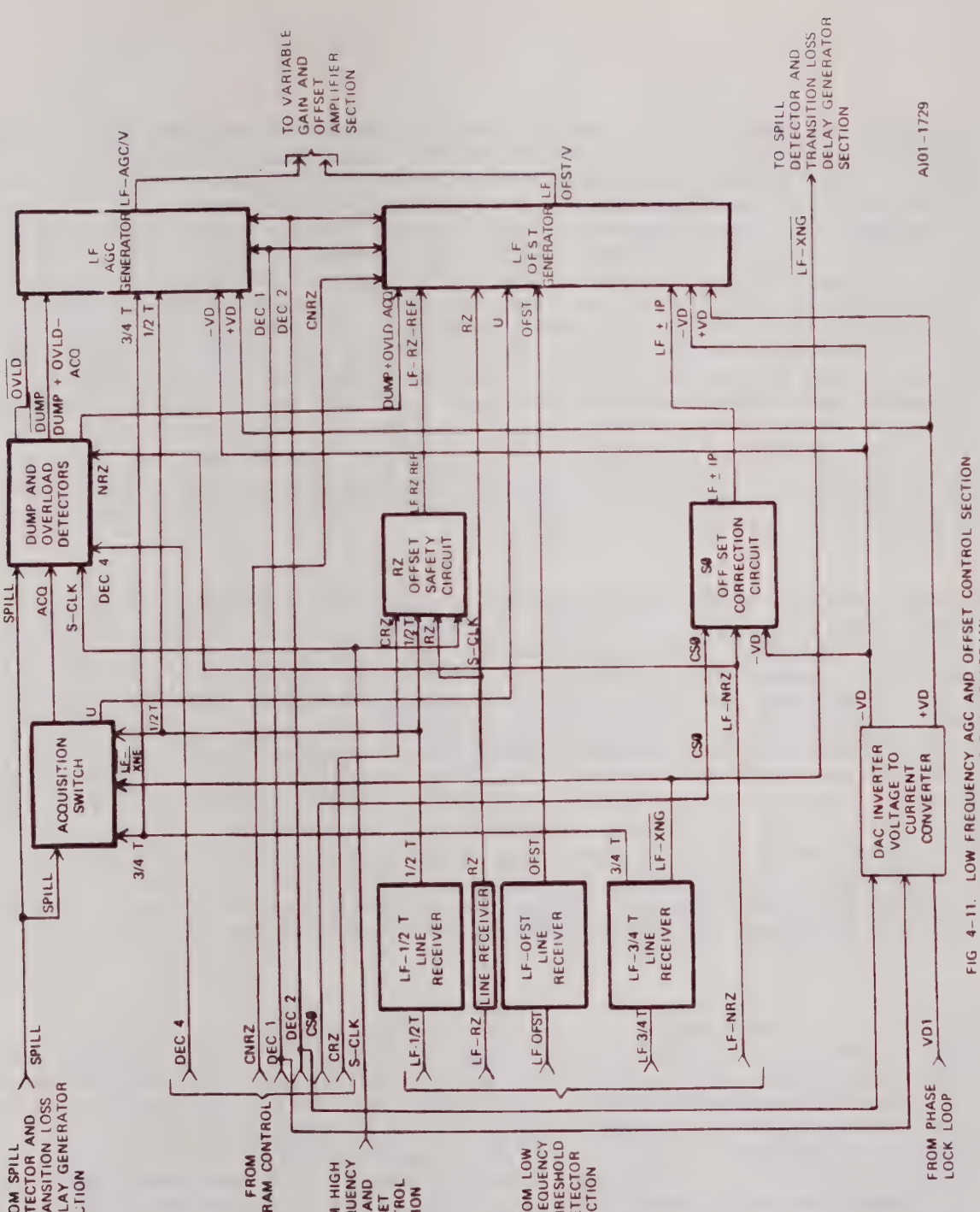


FIG 4-11. LOW FREQUENCY AGC AND OFFSET CONTROL SECTION DETAILED FUNCTIONAL DIAGRAM

Figure 4-11. Low Frequency AGC and Offset Control Section, Detailed Functional Block Diagram

In the LF AGC generator, the 1/2T pulse gates -VD and the 3/4T pulse gates +VD to derive -I and +I currents, respectively. These two currents are summed and thus generate LF-AGC/V. The DEC 1 and DEC 2 inputs aid in linearizing tracking currents used to generate LF-AGC/V. If the PCM data from the VG and OFST amplifier section increases in amplitude, the width of the 3/4T pulse increases faster than the width of the 1/2T pulse. As a result, the LF-AGC/V voltage being fed back to VG and OFST amplifier section goes negative to reduce the gain of the amplifier until the width of the 3/4T pulse is half the width of the 1/2T pulse. When this point is reached, the output of the amplifier is normalized. If the amplitude of the PCM data from the amplifier decreases, the width of the 3/4T pulse decreases faster than that of the 1/2T pulse, and a more positive LF-AGC/V feedback voltage is developed. This positive voltage increases the gain of the amplifier until the width of the 3/4T pulse is half that of the 1/2T pulse, once again normalizing the PCM data output of the VG and OFST amplifier section.

When processing NRZ or DM type PCM signals, SØ correction and RZ offset safety circuits are inhibited. The LF-OFST signal, which is generated from the zero crossings of the PCM data output of the low frequency threshold detector section, is fed through a line receiver to the LF offset generator and is gated with the μL pulse to derive CHARGE + and CHARGE -, which gate -VD and +VD, respectively. The gated -VD and +VD are summed to produce LF-OFST/V which is fed back to the VG and OFST amplifier section to normalize the offset. If the offset of the PCM data is positive, the transitions of LF-OFST occur sooner than normal, causing LF-OFST/V to go positive. This positive-going feedback voltage reduces the offset in the PCM data from the VG and OFST amplifier until the offset in the data is normalized. If the data has a negative offset, just the opposite occurs. The LF-OFST/V feedback goes negative to offset-normalize the PCM signal.

When processing SØ type PCM signals, OFST and RZ REF signals are inhibited. Offset averaging is provided by the SØ correction circuit which is enabled by CSØ. The LF-NRZ input from the low frequency threshold detector section is fed to the SØ correction circuit where it gates -VD to provide a bipolar current ±I that is proportional to the average offset of LF-NRZ. This bipolar current is fed to the LF offset generator. If the PCM data has a positive offset, the ±I causes the LF-OFST/V being fed back to the VG and OFST amplifier to go positive until the offset is normalized. If the data input has a negative offset, the reverse of the process just described occurs to normalize offset.

When processing RZ type PCM signals, OFST and ±I signals are inhibited. The LF-RZ is applied through its line receiver to the RZ offset safety circuit which is enabled by CRZ. Other inputs to the RZ offset safety circuit include 1/2T and S-CLK. These signals produce an RZ-REF pulse which is 1/2-bit period wide. This pulse gates +VD on and off.

The -VD is gated on and off by the RZ applied to LF offset generator. If the offset in the RZ data is positive, the LF-RZ pulse becomes wider than the output of the RZ offset safety circuit, thus keeping the -VD generator on longer than the +VD generator. As a result, a positive voltage appears at the LF-OFST/V output, and this is fed back to the VG and OFST amplifier to reduce the offset until the LF-RZ pulse is equal in width to that of the RZ REF pulse. When both pulses are equal, the offset of the input data is normalized. For negative offsets in the data input the LF-RZ pulse is narrower in width than the width of the RZ REF pulse. Consequently, this produces a negative LF-OFST/V voltage which is fed back to the VG and OFST amplifier to correct the offset in the data input until the LF-RZ pulse and RZ REF pulse are again equal in width.

The dump and overload detectors operate in the same manner as their counterpart detectors in the high frequency circuits. See paragraph 4.3.5.

4.3.9 Spill Detector and Transition Loss Delay Generator Section

Refer to figure 4-12. SPILL is generated using the transition detector, clock counter and delay select circuit. The clock counter, if not reset by the transition detector, advances 1 count for each 90° clock. Decoded counts of 128 and 2048 are applied to the delay select circuit. If $\overline{\text{SYNC}}$ is high (clock pulses in phase lock loop are not synchronized with incoming data), SPILL is produced at a count of 128. If $\overline{\text{SYNC}}$ is low, SPILL is produced at a count of 2048.

Each time RESET from transition detector is applied to the clock counter, the counter is reset to zero and thus restarts the counting of 90° clocks. Usually, RESET is received before the clock reaches 128. RESET is produced each time $\overline{\text{HF-XNG}}$ or $\overline{\text{LF-XNG}}$ goes low, thus indicating that high or low frequency data crossings are being received.

When SPILL is applied to the counter control circuit, CLEAR is generated and applied to loss storage and control circuit where the X-LOSS level is generated. X-LOSS remains high until eight data transitions are received from the high or low frequency AGC and offset control section. Each data transition from either $\overline{\text{HF-XNG}}$ or $\overline{\text{LF-XNG}}$ produces an XNG pulse which is applied to the counter control circuit. Each XNG pulse causes GATED CLK to advance the divide-by-eight counter by 1. When eight pulses are counted, DEL 8 is generated and transferred to the loss storage and control circuit where it causes X-LOSS level to go low. DEL 8 also inhibits GATED CLK until SPILL is again received to generate the next X-LOSS level. X-LOSS level is applied to phase lock loop and program and operational status displays.

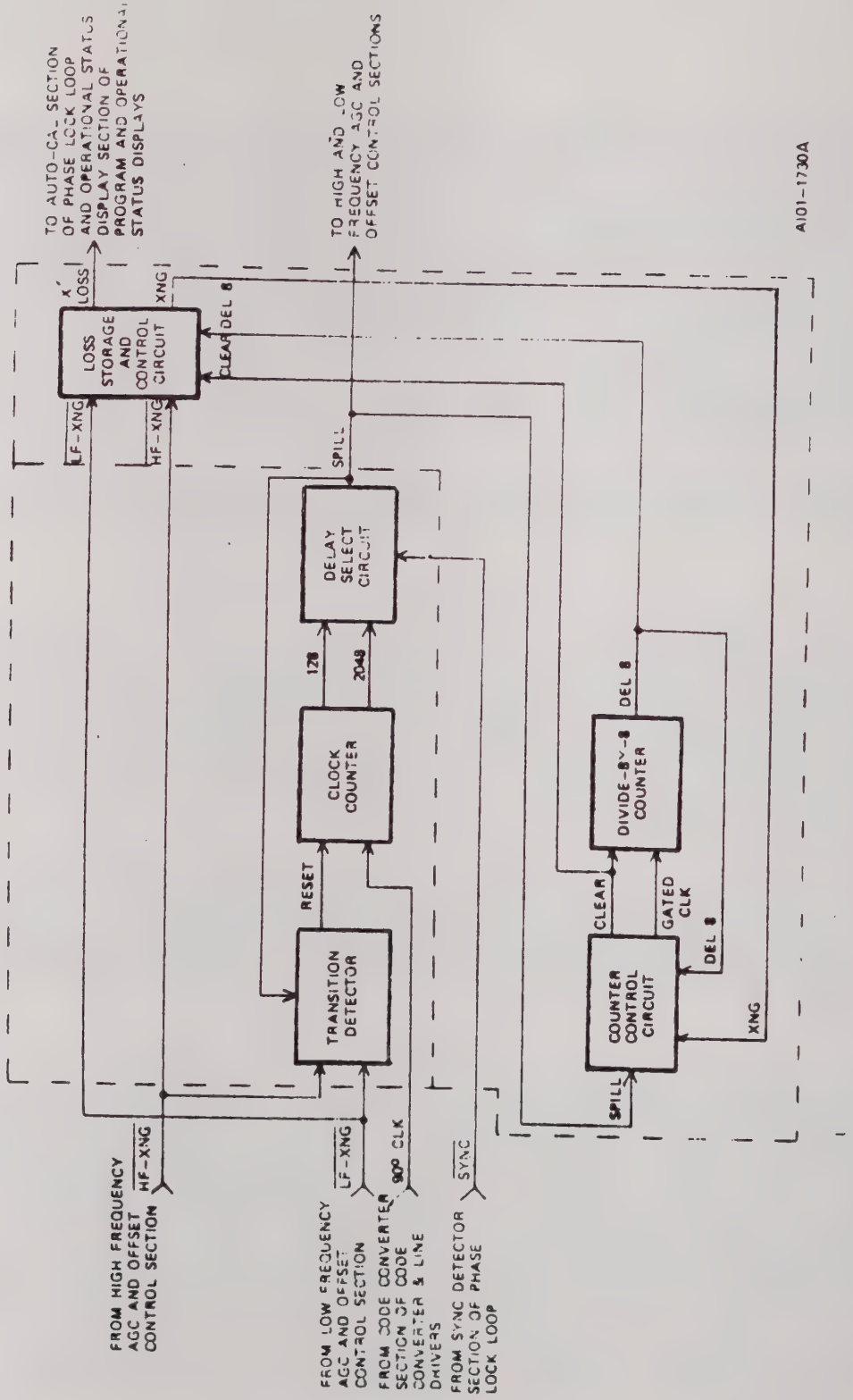


Figure 4-12. Spill Detector and Transition Loss Delay Generator Section, Detailed Functional Block Diagram

4.4 PHASE LOCK LOOP FUNCTIONAL AREA

The sections of phase lock loop functional area are shown in figure 4-13 and explained in the following paragraphs. After the description of this functional area, each section of this functional area is explained in more detail. For ease of reference, each block in figure 4-13 contains the figure number of its detailed functional block diagram.

The phase detector section accepts the U, Z and BD signals from input processing functional area and clocks from the countdown section. Either the Z or BD pulse is detected, depending on whether the PCM is RZ or not RZ, respectively. The result of this detection is the BD-NRZ signal which is the PCM information in NRZ code. It is transferred to the code converter portion of the code converter and line amplifiers functional area. The SD-BD signal is a buffered copy of the BD-NRZ signal and is tranferred to the sync detector. The ZR, UR, SD-CLK signals are buffered copies of Z, U and Øq clock. They are also transferred to the sync detector section where the phase of the signals are compared to the phase of SD-CLK to determine whether or not the signals are in phase with the generated clock. If not, $\overline{\text{SYNC}}$ is generated and transferred to the spill detector and transition loss delay generator section (figure 4-12) in the input processing functional area. As explained in paragraph 4.3.9, $\overline{\text{SYNC}}$ can cause SPILL and the X-LOSS to be generated. Also as explained earlier, SPILL initiates a normalization process in the input processing functional area in an effort to reestablish synchronization. If this process continues until X-LOSS is generated, $\overline{\text{SYNC}}$, together with X-LOSS, both applied to the automatic-calibration section, start an AUTO-CAL cycle which recalibrates the voltage controlled oscillator section via the VA signal. This process shifts the VCO clock frequency to achieve synchronization. Another signal from the sync detector section, SYNC LT, is transferred to the SYNC lamp which indicates, when lit, that the bit synchronizer is in sync. The SYNC lamp is part of the program and operational status displays functional area.

The phase detector section also compares the phases of the U pulse and clock and, in addition, when processing SØ PCM signals, compares the phases of the Z pulse and clock to derive a correction signal. This correction signal is HF-IØ when processing high frequency (10^4 bps or greater) PCM signals, or LF-IØ when processing low frequency PCM signals. The applicable signal is transferred to its associated tracking loop filter section where it is modified to account for the bit rate of the PCM and for the bandwidth of the tracking loop filter. The correction signal, LFΔI, from the low frequency tracking loop filter section, is routed into the high frequency tracking loop filter section where, depending on the PCM bit rate, the high frequency or low frequency correction signal is selected and transferred as VCOΔI, to the voltage controlled oscillator section.

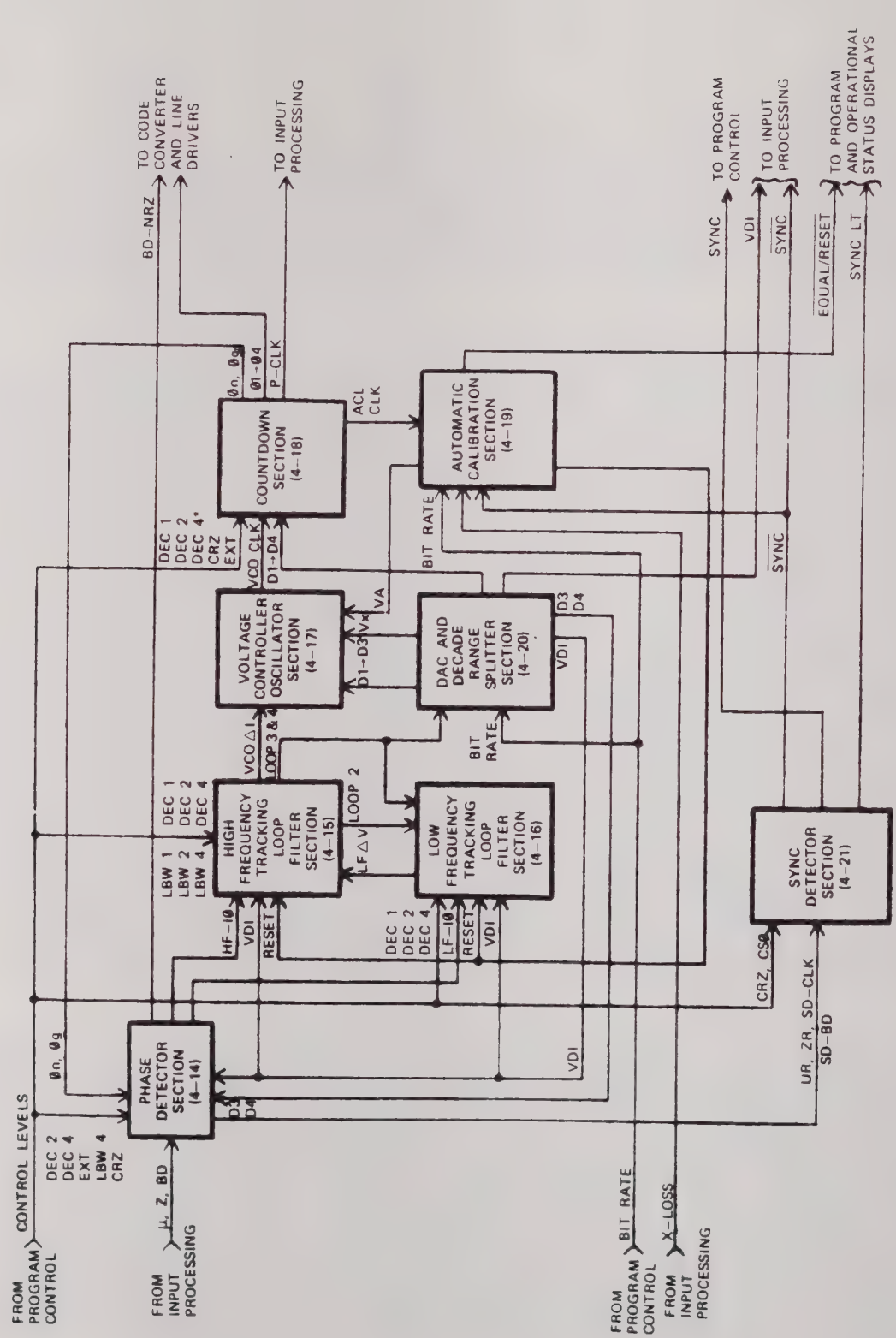


Figure 4-13. Phase Lock Loop, Functional Block Diagram

The voltage controlled oscillator (VCO) section is the basic clock generator from which all phases of clock are derived. It is a free-running oscillator whose frequency is periodically calibrated by a crystal controlled oscillator in the automatic calibration section. The VCO frequency is primarily determined by the setting of the BIT RATE thumbwheels on the front panels. In addition to the VA signal which is periodically updated by the automatic-calibration section, the frequency is affected by Vx, $\overline{D1}$, $\overline{D2}$ and $\overline{D3}$ from the DAC and decade range splitter section and VCOΔI from the high frequency tracking loop filter section. The prime function of Vx, modified by $\overline{D1}$, $\overline{D2}$ and $\overline{D3}$, is to provide a linear relationship between the dialed bit rate, regardless of the setting of the multiplier thumbwheel, and the VCO output frequency. The VCOΔI signal compensates for any frequency deviation between the VCO output frequency and the frequency and phase of the incoming PCM.

The VCO output frequency, called VCO clock, is routed to the countdown section where it is divided to provide a frequency substantially equal to that of the dialed bit rate (or the bit rate as received from an external source when the bit synchronizer is operated in the program mode). Three additional quadrature phases of clock at bit rate frequency are generated within the countdown section. The phases identified as Øn, $\overline{Øn}$, Øq, and $\overline{Øq}$, are transferred to the phase detector section where they are compared with the incoming signals. The phases identified as Ø1, Ø2, Ø3 and Ø4 are transferred to the code converter portion of the code converter and line drivers functional area. The P-CLK, also at the bit rate frequency, is transferred to the input processing functional area. The ACL-CLK which is applied to the automatic-calibration section, is within a frequency range of 0.2 to 2 MHz.

The automatic-calibration section provides a full AUTO-CAL cycle when the RESET pushbutton is pressed or when either of the two most significant digits of the bit rate is changed. During this cycle, RESET nullifies the effects of HF-IØ and LF-IØ which, in turn, normalizes the VCOΔI signal. Meanwhile, VA, after being set to a mid-range value, is updated every 10 milliseconds for at least 2 seconds. VA is the result of the comparison between ACL-CLK and control levels derived from the crystal controlled oscillator. Thus, the frequency of the VCO section is calibrated to crystal accuracy. After full AUTO-CAL cycle, the last value for VA remains constant and VCOΔI again affects the VCO frequency. If both $\overline{SYNC}$ and X-LOSS occur, the automatic-calibration section initiates a partial AUTO-CAL cycle which is similar to the full AUTO-CAL cycle except (1) the cycle terminates when either $\overline{SYNC}$ or X-LOSS is absent, and (2) instead of presetting the VA signal to a midscale before updating, the VA signal is updated from its previous value.

4.4.1 Phase Detector Section

The phase detector section (see figure 4-14) provides three types of signals that are utilized in other sections of the bit synchronizer. These signals are: BD-NRZ which is transferred to the code converter and line amplifier functional area; the ZR, UR, SD-BD and SD-CLK which are transferred to the sync detector section; and the HF-IØ and LF-IØ which are transferred to the high and low frequency tracking loop filter sections. All of these signals are derived from one or more of the following: three input signals (BD, Z and U), two phases of clock (Øn and Øq), various control levels (CRZ, EXT, LBW 4, DEC 4*, DEC 2, D3 and D4) and the VD1 signal which is an analog voltage proportional to the decade bit rate. Each of the input signals and the two phases of clock are received in differential form, applied through an individual line receiver and then made available in their true and, if necessary, their complement forms.

The bit detector uses EXT to select the proper phase of clock during the bit detection process. CRZ causes the Z pulse to be detected when RZ type PCM data is being processed and causes the BD pulse to be detected when the PCM data being processed is other than RZ. The output signal, BD-NRZ, is PCM data in NRZ code. The same signal is applied through a line driver for transfer as SD-BD to the sync detector.

The primary phase detector compares the transitions of Øn clock with the U pulse to determine whether or not Øn clock transitions are occurring in the middle of the U pulse, which indicates the bit rate of the clock and U pulse are the same. Under this condition, the primary phase detector provides X and Y pulses whose widths are identical and each equivalent to one-half the U pulse; otherwise, one output pulse is wider than half a U pulse and the other output pulse is narrower than half a U pulse.

The Δ current generator accepts the X and Y signals and, if they have equal widths, equal and opposite currents are generated; however, when the two input signals differ in width, a predominant current in one direction is generated. These currents flow through the routing switch into and out of the appropriate tracking loop filter section. Thus, unequal bidirectional currents subsequently change the frequency of the generated clock until the X and Y pulses are equal in width.

Because the X and Y pulses become relatively narrower as the bit rate is increased, the amount of current for the correction signal must be increased proportionally to the bit rate. This tracking capability is provided by the loop bandwidth tracking control circuit. In addition, tracking also is enhanced by using one of three current range select circuits within the Δ current generator. The frequency range decoder provides three levels corresponding to frequency ranges

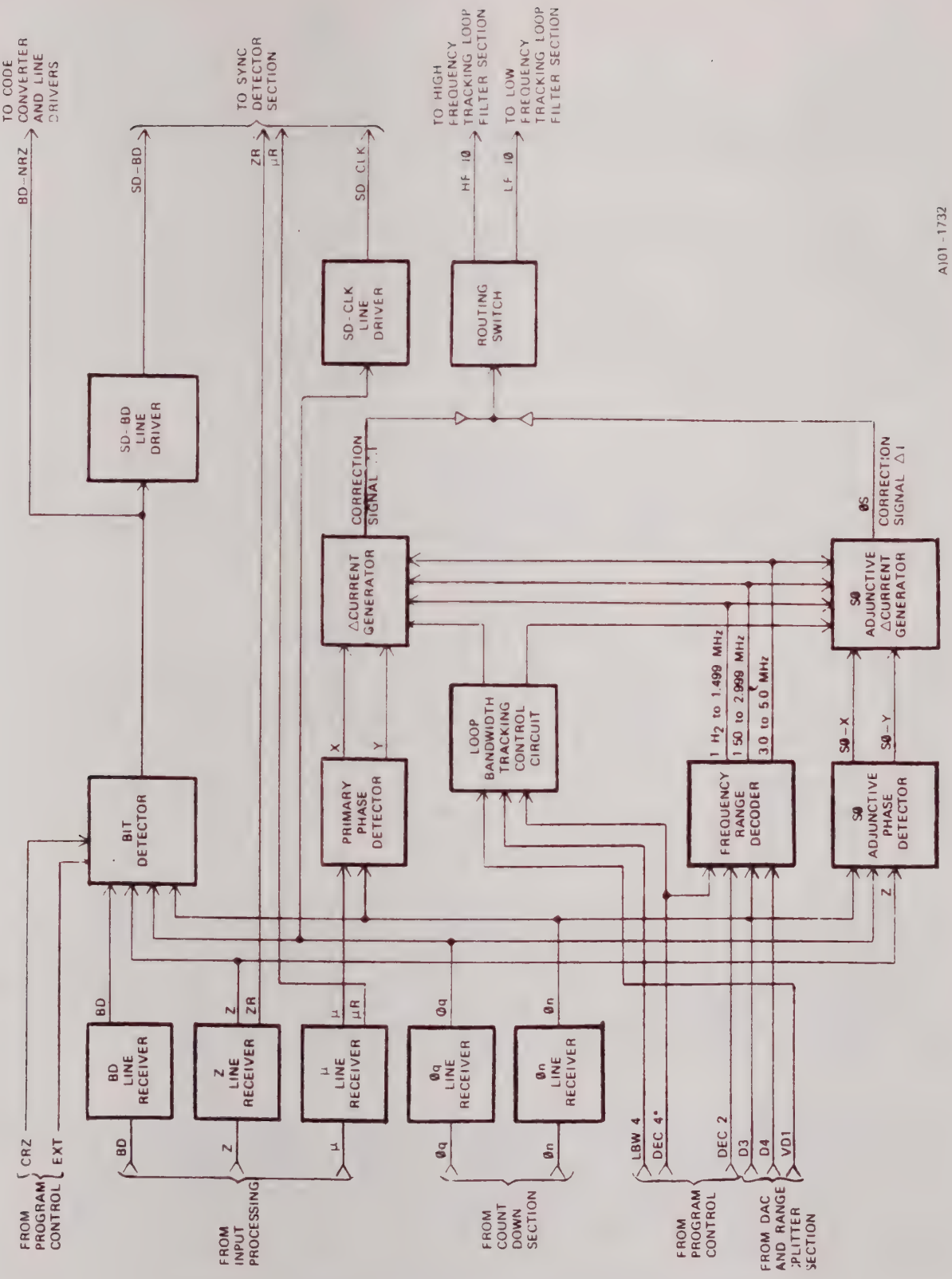


Figure 4-14. Phase Detector Section, Detailed Functional Block Diagram

of 1 Hz to 1.499 MHz, 1.50 to 2.999 MHz and 3.0 to 5.0 MHz. One of these levels, depending on the operating frequency, is active and selects the appropriate current range select circuit.

When processing SØ type PCM signals, the SØ adjunctive phase detector and the SØ adjunctive Δ current generator are used to ensure that correction signals will be generated as necessary when a long series of ONEs or ZEROs is contained in the PCM data. These two circuits operate in the same manner as the primary phase detector and the Δ current generator described previously, only the input signals differ. The output, SØ correction signal, is added to the output of the primary phase detector.

Signals Øq and BD-NRZ are applied through individual line drivers to the sync detector section; the output signals are identified as SD-CLK and SD-BD, respectively. Signals ZR and UR are obtained from the Z line receiver and U line receiver, respectively. These signals also are transferred to the sync detector section.

4.4.2 High Frequency Tracking Loop Filter Section

The high frequency tracking loop filter section (see figure 4-15) smoothes the pulse-width-modulated bipolar current, HF-IØ, from the phase detector, to produce a filtered phase error current, VCOΔI, whose amplitude is adjusted for the bit rate and bandwidth. The VCOΔI is fed to the VCO to adjust its frequency and null the phase error between the VCO and the incoming PCM data at zero. The high frequency tracking loop filter section operates at bit rates 1.000×10^4 bps and higher.

The loop filter is a network composed of selectable capacitors and a circuit to provide a variable resistance in shunt with some of the capacitors. The overall function of the loop filter is to provide a filter whose characteristics are determined by the bit rate and the selected loop bandwidth. The desired capacitors are selected by a combination of DEC 4, DEC 2, DEC 1, LOOP 2, and LOOP 3 & 4. The desired shunt resistance is selected by the value of VD1.

The filtered HF-IØ signal is applied through a buffer whose output is applied to the HF/LF select circuit and also to the feedback network. The feedback network has its amplification controlled by VD1 and provides an output signal that maintains the input to the buffer at a dc level of 5.5 volts. The feedback network is effective primarily during the absence of PCM to maintain the proper dc level at the input to the buffer.

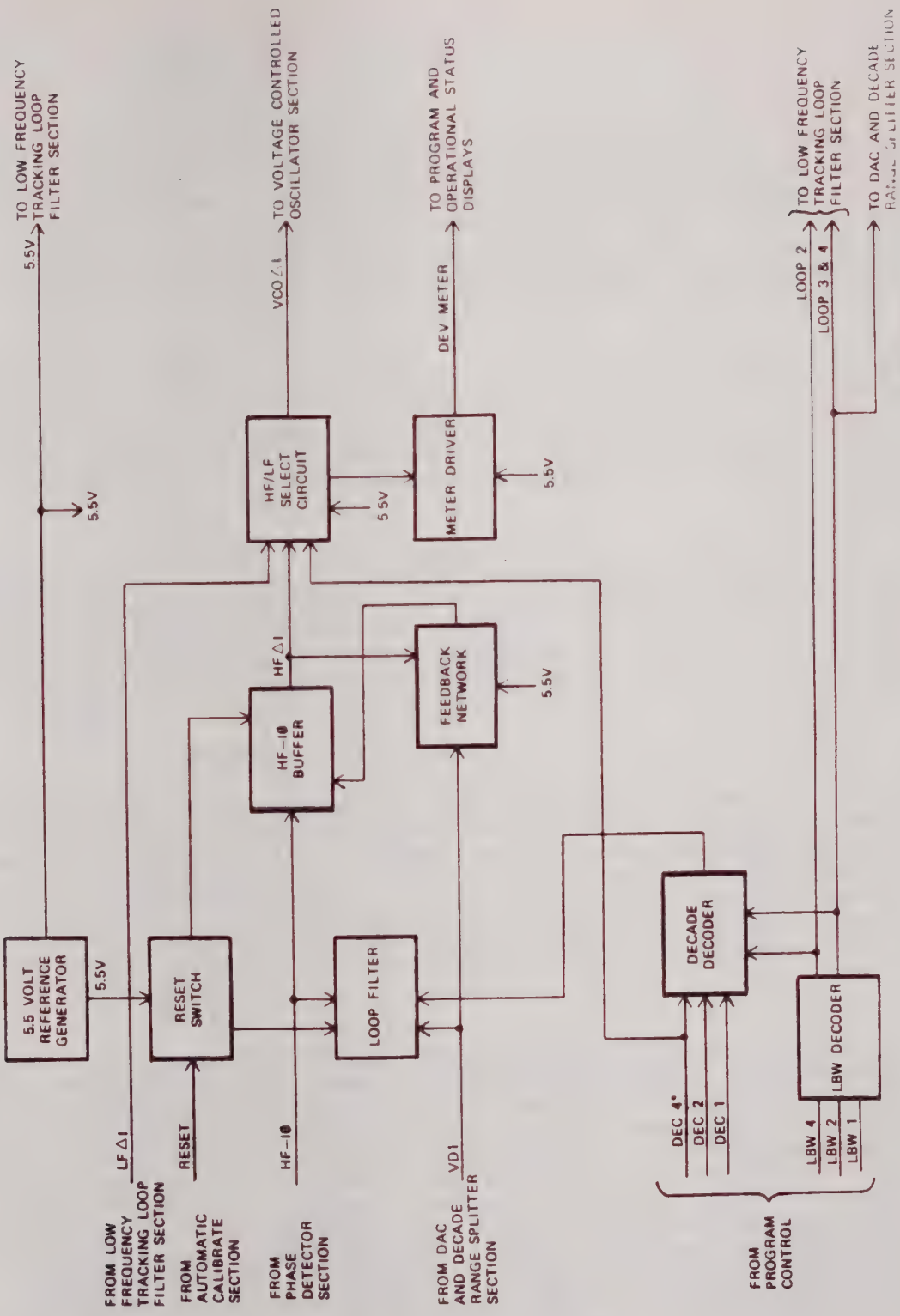


Figure 4-15. High Frequency Tracking Loop Filter Section, Detailed Functional Block Diagram

The HF/LF select circuit consists of select relays and a line driver. DEC 4* controls the operation of the relays which direct LFΔI or HFΔI through the line driver to become VCOΔI. When the bit rate is lower than 10^4 bps, LFΔI is selected and when the bit rate is 10^4 bps or higher, HFΔI is selected. The selected signal, LFΔI or HFΔI, also is applied through the meter driver to the LOOP DEVIATION meter which is part of the program and operational status displays.

The reset switch, upon receipt of RESET signal from the AUTO-CAL section, normalizes the input to the buffer and loop filter to 5.5 volts. The 5.5 volt reference generator provides a regulated source of 5.5 volts for the reset switch, the feedback network, the HF/LF select circuit, low frequency tracking loop filter, and the meter driver.

The LBW decoder accepts inputs of LBW 4, LBW 2 and LBW 1 and decodes control levels of LOOP 2 and LOOP 3 & 4. The decade decoder adds the binary value of DEC 4*, DEC 2 and DEC 1 to the binary value of LOOP 2 and LOOP 3 & 4. The resultant binary sum is converted to a decimal value which selects the proper capacitors in the loop filter.

4.4.3 Low Frequency Tracking Loop Filter Section

This filter section (see figure 4-16) accepts LF-IØ which, when PCM is synchronized, is positive and negative current pulses of equal duration and amplitude; the net result at the output of this section is a zero volt dc change of 5.5 volt bias. For phase difference between the PCM signal and clock, the width relationship of LF-IØ changes, causing the 5.5 volt reference to increase or decrease which, in turn, changes the VCO frequency in a direction to provide synchronization.

To provide linearity from input to output, the loop filter is frequency compensated by a pair of selectable capacitors whose capacitance effect is changed by the gain of two operational amplifiers. The desired pair of capacitors is selected by the output levels from the decade decode circuit. Relatively large values are selected for bit rates of 10^0 and 10^1, and relatively small values are selected for bit rates of 10^2 and 10^3. Further, the gain of the operational amplifiers is changed in response to DEC 1 which is applied through the DEC 1 driver and the resistive element of two Raysistors which are controlled by the Raysistor control circuit in response to VD1 and DEC 1. Thus, the RC time constant of the loop filter is linearly decreased as the bit rate is increased to provide the linear change between the width difference of the input signal and the amplitude of the output signal for all bit rates between 1.000×10^0 to 9.999×10^6 bps. In addition, the RC time constant of the loop filter is affected by the LOOP 2 and LOOP 3 & 4 control levels which select smaller value resistors to increase the bandwidth of the loop filter as the LOOP BAND switch is rotated towards the higher numbers.

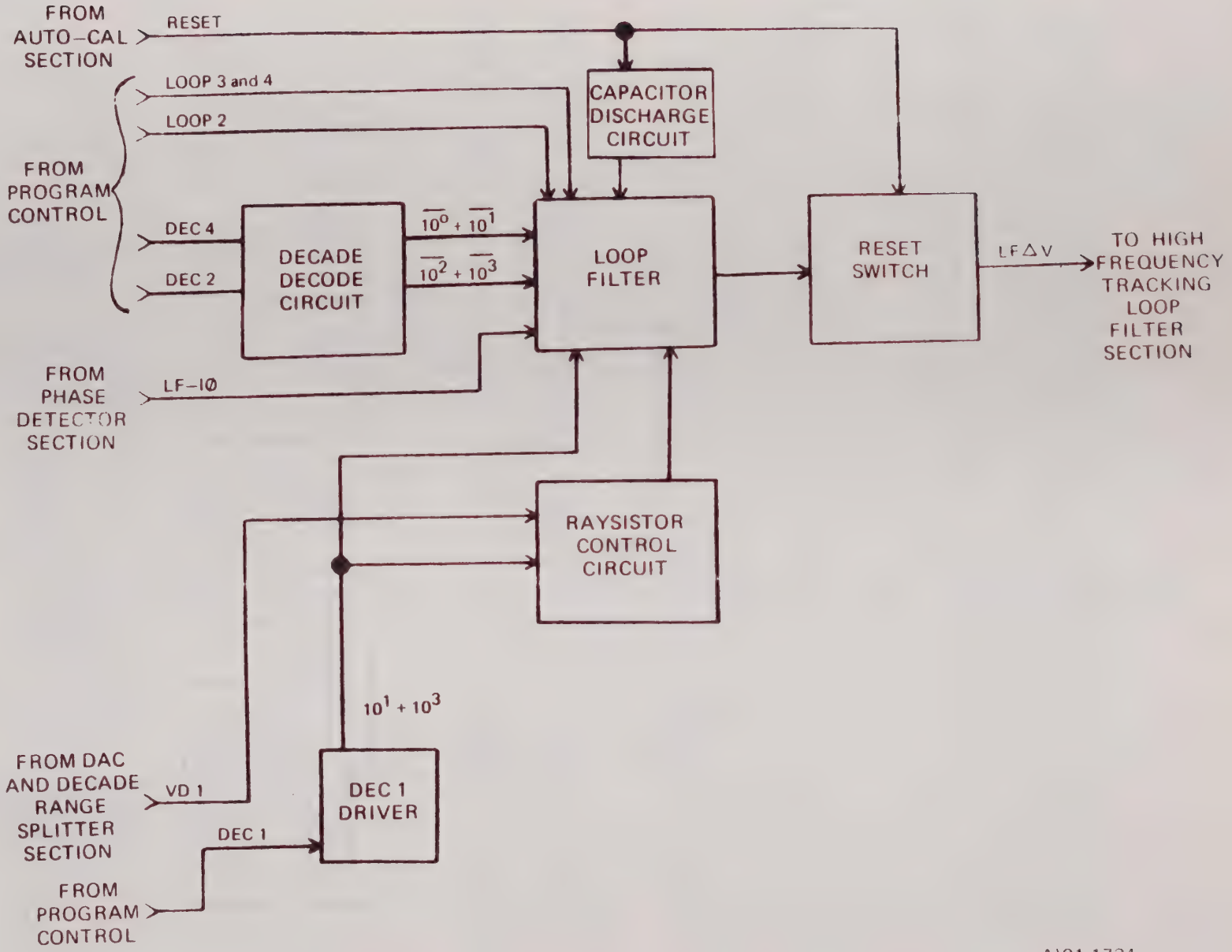


Figure 4-16. Low Frequency Tracking Loop Filter Section, Detailed Functional Block Diagram

When RESET is not present, the output signal from the loop filter is passed through the reset switch to the high frequency tracking loop filter section. When RESET is present, the reset switch clamps the output, LFΔV, at 5.5 volts. RESET is generated during AUTO-CAL cycle to hold LFΔV at the center of its range while the VCO is being calibrated. The RESET level, applied through the capacitor discharge circuit, discharges the selected pair of capacitors in the loop filter to avoid abrupt changes in LFΔV when RESET is terminated.

4.4.4 Voltage Controlled Oscillator Section

Refer to figure 4-17. The emitter controlled oscillator (ECO) generates the basic frequency from which the clocks are derived. Essentially, the ECO is a multivibrator whose output frequency is determined primarily by the amount of current provided through the current source from the current multiplier. The current multiplier is controlled primarily by the tuning voltage obtained from the gain selectable amplifier whose output increases from 5 to 10 volts as the bit rate increases from 1.000 to 9.999 in each decade range.

The gain selectable amplifier uses $\overline{D1}$, $\overline{D2}$ and $\overline{D3}$ to set the gain of the amplifier to 1, 2, 4 or 8, depending on which segment of the bit rate range within which the bit synchronizer is operating. The Vx signal is then amplified by the amplifier and becomes the tuning voltage. A summary of the parameters for the gain selectable amplifier and the resultant output frequency ranges are given in table 4-1.

Table 4-1. Derivation of VCO Output Frequency

SIGNIFICANT DIGITS OF DECADE	CONTROL LEVELS			Vx RANGE (volts)	AMPLIFIER GAIN	TUNING VOLTAGE (volts)	VCO FREQUENCY (MHz)
	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$				
1.000 to 1.499	H	H	H	0.5 to 0.75	8	4 to 6	16 to 24
1.500 to 2.999	H	H	L	0.75 to 1.5	4	3 to 6	12 to 24
3.000 to 5.999	H	L	H	1.5 to 3.0	2	3 to 6	12 to 24
6.000 to 9.999	L	L	L	3.0 to 5.0	1	3 to 5	12 to 20

The -6.2 volt reference generator establishes a reference level for the amplitude control circuit. The reference voltage is adjustable to preset the center frequency of oscillation. The VA signal, from automatic-calibrate section is a dc voltage to ensure the VCO frequency is accurate to crystal tolerances.

The VCOΔI signal, from the high frequency tracking loop filter section, is the error voltage representing the frequency difference between the generator frequency and the PCM bit rate. This error voltage changes the gain of an amplifier through which the tuning voltage is applied

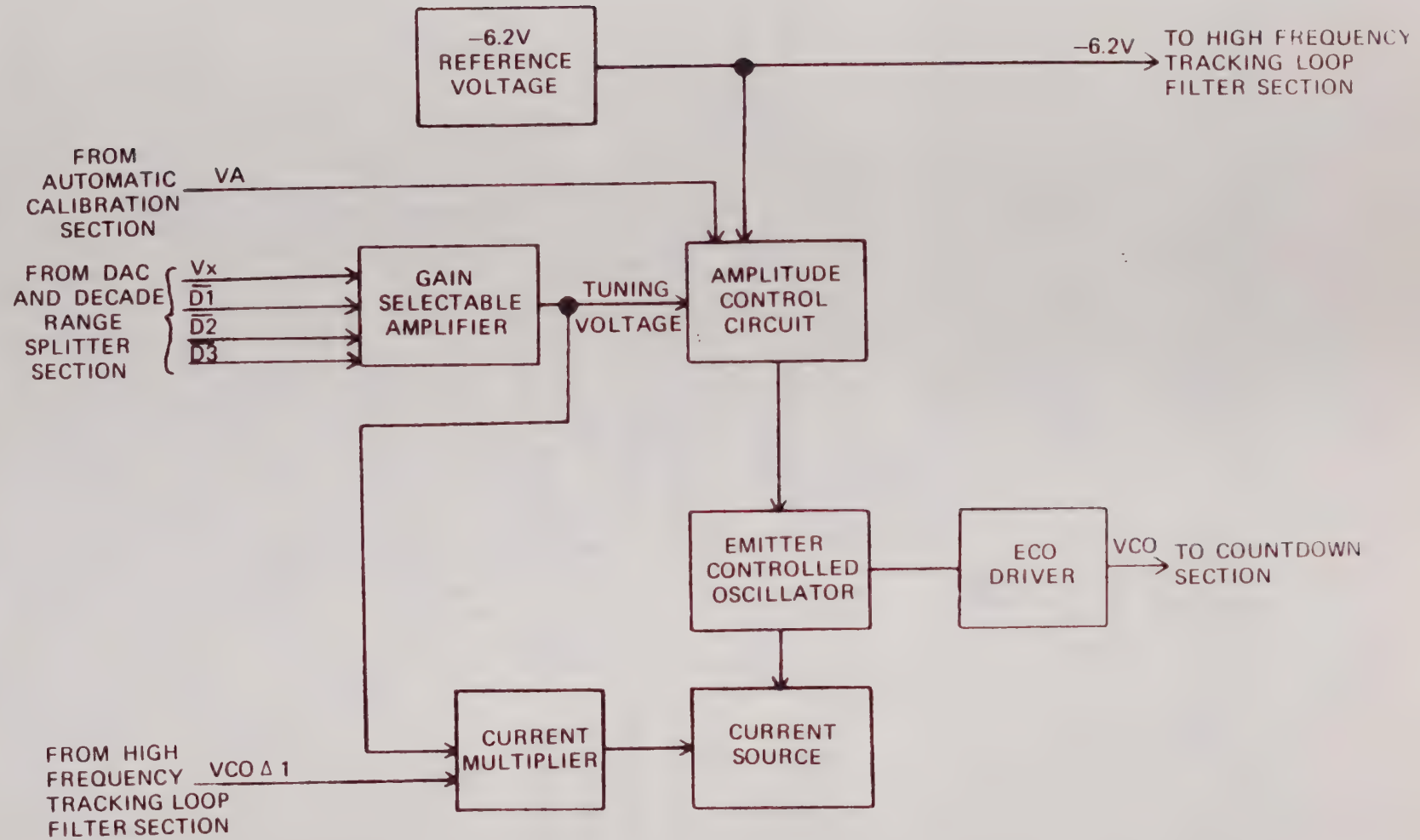


Figure 4-17. Voltage Controlled Oscillator Section, Detailed Functional Block Diagram

to current source and, thus, increases or decreases the frequency established by the tuning voltage until the generated frequency is the same as the PCM bit rate. The output of the ECO is applied through the ECO driver to the countdown section.

4.4.5 Countdown Section

Refer to figure 4-18. The range select prescaler, under control of the D1, D2, D3 and D4 control levels from DAC and the decade range splitter section, divides the incoming VCO frequency from the voltage controlled oscillator by 1, 2, 4 or 8. The dialed bit rate, the active control level, the VCO frequency range, the prescaler division factor and the prescaler output frequency range are as shown in table 4-2.

Table 4-2. Derivation of Prescaler Output Frequency

DIALED BIT RATE	ACTIVE CONTROL LEVEL	VCO FREQUENCY RANGE	PRESCALER DIVISION FACTOR	PRESCALER OUTPUT FREQUENCY RANGE
6.000 to 9.999	D1	12 to 20 MHz	none	12 to 20 MHz
3.000 to 5.999	D2	12 to 24 MHz	÷2	6 to 12 MHz
1.500 to 2.999	D3	12 to 24 MHz	÷4	3 to 6 MHz
1.000 to 1.499	D4	16 to 24 MHz	÷8	2 to 3 MHz

The selected output from the range select prescaler is applied directly to the clock select and also through the divide-by-ten divider to the AUTO-CAL section as ACL CLK. Therefore, the ACL CLK is 1/10 the frequency of the output from the prescaler. The output of the divide-by-ten divider also is applied directly to clock select and through decade divider to clock select. The decade divider includes five frequency dividers, each providing a frequency 1/10 lower than its input frequency. Therefore, clock select has seven input frequencies, each of which is 1/10 lower than its adjacent higher frequency; the highest frequency is within the output frequency range select prescaler. One of the seven frequencies is selected by the decoded decimal value of DEC 1, DEC 2 and DEC 4*. The selected frequency from clock select is then applied through the divide-by-two and quadrature generator where the input frequency is divded by two and four quadrature phases of the frequency are generated. Thus, the series of dividers provides a clock frequency to the buffer and multipliers that depends on the output frequency of the range select prescaler and the bit rate multiplier, which is represented by the decoded decimal value of DEC 1, DEC 2 and DEC 4*. This relationship is shown in table 4-3.

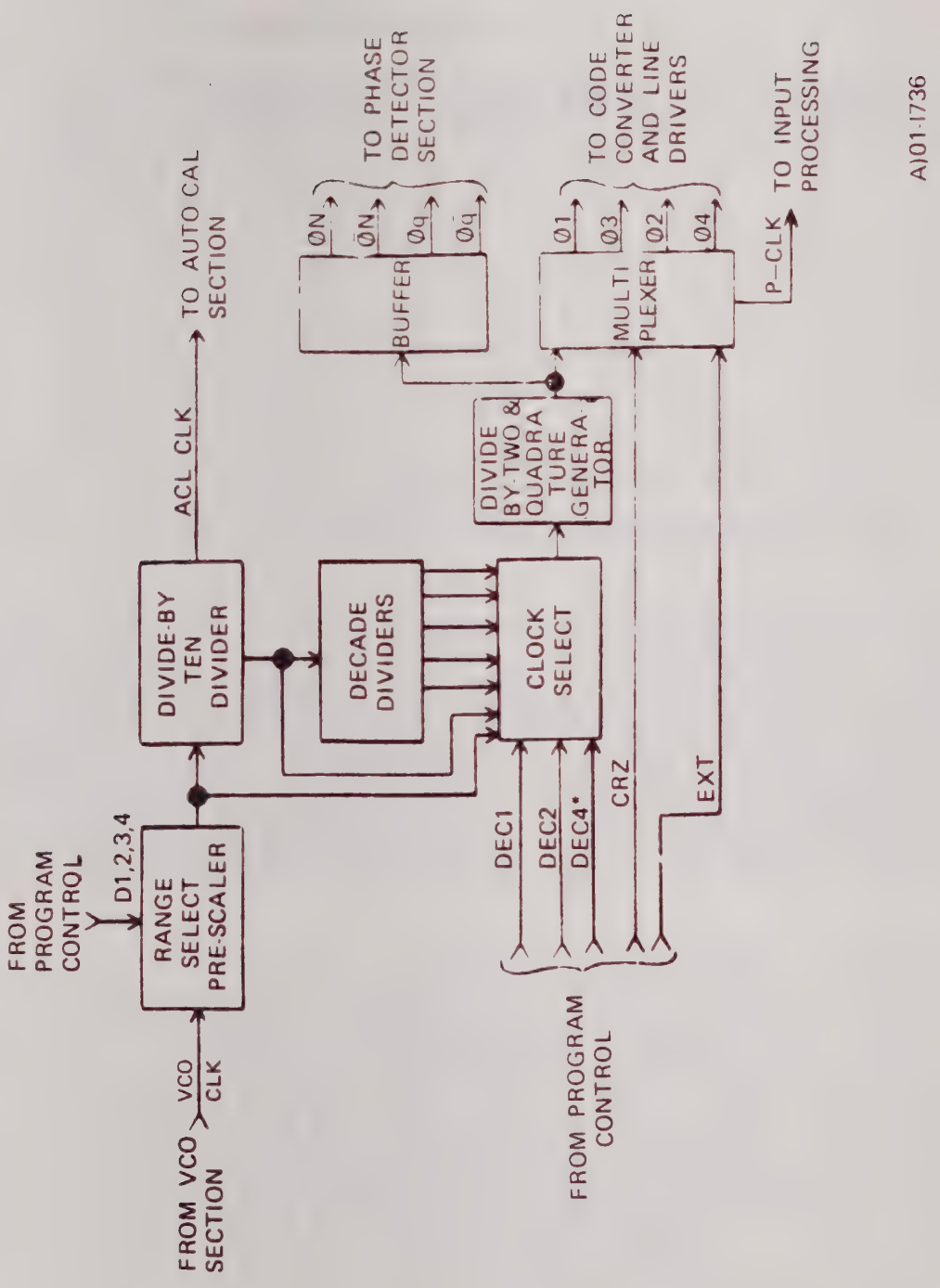


Figure 4-18. Countdown Section, Detailed Functional Block Diagram

Table 4-3. Derivation of Clock Rate

BIT RATE MULTIPLIER	CONTROL LEVELS			DECADE DIVIDER OUTPUT [1]	CLOCK RATE RANGE
	DEC 4*	DEC 2	DEC 1		
10^6	1	1	1	No divide	1 to 10 MHz
10^5	1	1	0	1/10	0.1 to 1 MHz
10^4	1	0	1	1/100	10 to 100 kHz
10^3	1	0	0	1/1,000	1 to 10 kHz
10^2	0	1	1	1/10,000	0.1 to 1 kHz
10^1	0	1	0	1/100,000	10 to 100 Hz
10^0	0	0	1	1/1,000,000	1 to 10 Hz

[1] Expressed as fractional value of output from range select prescaler

The divide-by-two and quadrature generator produces four phases of clock at the dialed bit rate, and these are fed to the multiplexer and buffer. The buffer derives Øn and Øq and their complements, $\overline{Ø}$n and $\overline{Ø}$q, which are fed to the phase detector section. The multiplexer, under control of CRZ and EXT from the program control, selects the correct phases of Øn and Øq to produce Ø1, Ø2, Ø3 and Ø4 clocks, which are in turn routed to the code converter and line amplifiers. The P-CLK signal, also derived in the multiplexer, is fed to the high frequency AGC and OFFSET control section of input processing. Sources for Ø1, Ø2, Ø3 and Ø4 clocks for the various PCM codes are shown in table 4-4.

Table 4-4. Derivation of Clock Phases

CODES	CLOCKS			
	Ø1	Ø2	Ø3	Ø4
NRZ or BIØ	$\overline{Ø}$n	Øq	Øn	$\overline{Ø}$q
RZ	Øn	$\overline{Ø}$q	$\overline{Ø}$n	Øq
ALL codes with EXT clock	Øq	Øn	$\overline{Ø}$q	$\overline{Ø}$n

4.4.6 Automatic Calibration Section

The AUTO-CAL section (see figure 4-19) automatically calibrates the voltage controlled oscillator section so that the counted-down clocks are within 0.1 percent of the selected bit rate, by comparing a derivative of the VCO output frequency (ACL CLK) with the dialed bit rate and then, using the results of the comparison to increase or decrease the VCO frequency by one increment. This process is repeated until the VCO frequency is correct. Basically, this operation uses the 4-digit comparator, the frequency counter and the associated circuits. When the ACL CLK, and therefore the VCO frequency, is correct, the number of pulses of ACL CLK within a 5-millisecond period is exactly equal to the four digits of the dialed bit rate, disregarding the decimal point. For example, at a dialed bit rate of 1.000, the ACL CLK should be 0.2 MHz, and within a 5-millisecond period this frequency provides 1000 pulses. Therefore, by gating ACL CLK into the frequency counter with a 5-millisecond pulse, the frequency counter counts the ACL CLK pulses for 5-milliseconds. This count is compared in the 4-digit comparator with the four digits of the dialed bit rate. If the number in the frequency counter is greater than the 4 digits of the bit rate, or if the frequency counter should overflow indicating the VCO frequency is too high, the A>B level from the 4-digit comparator, with or without OVERFLOW from the frequency counter, directs the up/down counter to be decremented. If the number in the frequency counter is less than the 4 digits of bit rate, indicating the VCO frequency is too low, the A>B level from the 4-digit comparator without OVERFLOW from the frequency counter directs the up/down counter to be incremented. The increment or decrement signal, as applicable, is clocked into the up/down counter circuits by a pulse from the timing generator after the 5-millisecond counting period. The output of the up/down counter circuits is continuously converted in the VA DAC to an analog voltage which in turn changes the VCO frequency.

For a full AUTO-CAL cycle, the process just described is repeated every 10 milliseconds for a 2-second period or thereafter until the RESET pushbutton is released. The final count in the up/down counter remains and thus affects the VCO frequency until another AUTO-CAL cycle is initiated. If the next AUTO-CAL cycle is a full one, the up/down counter is preset to midscale by the 8-nanosecond pulse; if the next AUTO-CAL cycle is a partial one, the count in the up/down counters is not preset but is updated from its previous count. For a partial AUTO-CAL cycle, the process just described also is repeated every 10 milliseconds; however, the partial AUTO-CAL cycle is terminated by the absence of $\overline{\text{SYNC}}$ or X-LOSS.

The basic timing, 1 kHz, for the AUTO-CAL section is obtained from the 1 kHz reference generator and applied to the timing generator where various timing signals are generated to program the operation of the AUTO-CAL section. Basically, the timing generator provides the following: a 10-millisecond square wave to establish a 5-millisecond period which counts an ACL CLK pulse, and a 5-millisecond

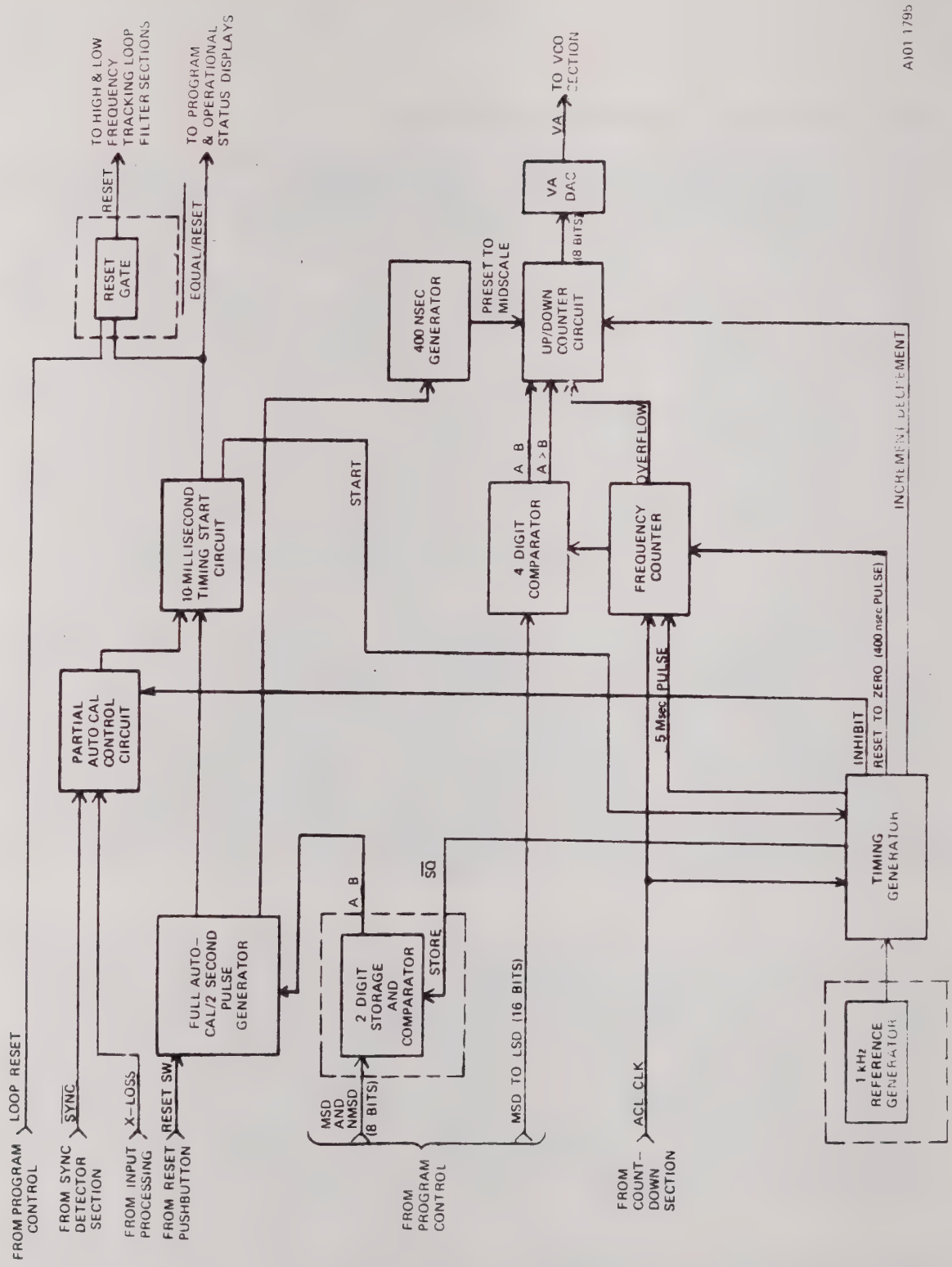


Figure 4-19. Automatic-Calibration Section, Detailed Functional Block Diagram

period which prepares the circuits for the next counting period; a 2-millisecond pulse which terminates 9 milliseconds after the start of counting to increment or decrement the up/down counter as determined by input control levels; and a 400-nanosecond pulse that resets the frequency counter and overflow detector immediately after the up/down counter is incremented or decremented.

A full AUTO-CAL cycle is initiated when the RESET pushbutton is pressed or when the MSD or NMSD bit rate thumbwheel is changed. When RESET pushbutton is pressed, the 2-second pulse generator is activated which holds the full AUTO-CAL control circuit activated for 2 seconds. When the MSD or NMSD bit rate thumbwheel is changed, A=B from 2-digit storage and comparator is directed through the equal storage select circuit to the full AUTO-CAL control circuit and activates this circuit. The output of the full AUTO-CAL control circuit is returned to the 2-second pulse generator whose output holds the full AUTO-CAL control circuit active for 2 seconds. An output from the 2-second pulse generator also inhibits the partial AUTO-CAL control circuit while the 2-second period is running. The full AUTO-CAL cycle terminates at the end of the 2-second period or thereafter when the RESET pushbutton is released. A partial AUTO-CAL cycle is initiated when SYNC and X-LOSS are present. This activates the partial AUTO-CAL control circuit. The partial AUTO-CAL cycle is terminated when SYNC or X-LOSS is absent.

The output of the partial or full AUTO-CAL control circuit, whichever is active, is applied through the 10-millisecond timing start circuit and accomplishes three functions as follows: a signal applied through an inverter on the LDY001 card to the high frequency tracking loop filter sections where it inhibits the tracking loop filter error signal, VCOΔI, and thus prevents this signal from changing the VCO frequency; a signal, EQUAL/RESET, is applied to the program and operational status displays where it lights the AUTO-CAL lamp to indicate the bit synchronizer is in AUTO-CAL mode; (The AUTO-CAL lamp is part of the multiplier digit of the bit rate indicators and appears as a dot of light adjacent to the digit.) A START signal is applied to the time generator to initiate the 10-millisecond square wave and the other timing signals obtained from the timing generator. The INCREMENT/DECREMENT pulse updates the up/down counter in accordance with the input level nine milliseconds after the start of the 10-millisecond updating cycle. 400-nanoseconds after updating, the RESET-TO-ZERO pulse resets the frequency counter and the overflow detector in preparation for the next 10-millisecond updating cycle. The TERMINATE pulse provides a positive transition 6 milliseconds after the start of the 10-millisecond updating period to ensure that termination does not occur during the first 5 milliseconds when ACL CLK is being counted; therefore, termination of the full AUTO-CAL cycle occurs 6 milliseconds after the count in the frequency counter is equal to the dialed bit rate.

4.4.7 DAC and Decade Range Splitter Section

The DAC and decade range splitter section (see figure 4-20) includes two eight-bit-digital-to-analog (DAC) converters that accept, in binary-coded decimal form, the four significant bits of the bit rate. DAC No. 1 accepts the two most significant digits and DAC No. 2 accepts the two least significant digits. The analog voltage from each DAC converter is applied to the combiner where one analog voltage, Vx, proportional to the value of the four digits, is produced.

The controlled gain amplifier has unity gain when the phase error signals are processed through the two narrowest bandwidths of the tracking loop filter. These bandwidths are configured when the LOOP BAND switch is in position 1 or 2. In LOOP BAND switch position 3 or 4 a high control level, LOOP 3 & 4, is generated and applied to the controlled gain amplifier. This high control level changes the gain of the amplifier from unity to 1.1. Therefore, for loop bandwidths 1 and 2, VD1 is equal to Vx and for loop bandwidths 3 and 4 VD1 is 10 percent larger than Vx.

The decade range splitter is a group of logic elements that decode the two most significant digits of the bit rate into four control levels. Each level, when high, represents a range of the two most significant digits as follows: for D4, the range is 1.0 to 1.4; for D3, the range is 1.5 to 2.9; for D2, the range is 3.0 to 5.9 and for D1, the range is 6.0 to 9.9.

4.4.8 Sync Detector Section

Refer to figure 4-21. The line receivers accept SD-CLK, SD-BD, ZR and UR and provide the desired output signals as determined by control levels CRZ and CSØ. The outputs, $\overline{CLK}$, $\overline{BD}$, Z and U are derivatives of SD-CLK, SD-BD, ZR and UR respectively. When LOSS is present, all outputs from the line receivers are inhibited.

When processing NRZ or DM type PCM, U and CLK are transferred to the main mixer; the remaining output signals are inhibited. The main mixer compares the phase of these two signals to determine whether or not they are in sync. This decision is transferred through the sync switch to the AUTO-CAL section and the input processing functional areas. When an out-of-sync condition exists, the AUTO-CAL section and the input processing functional area initiate separate processes to reinitiate synchronization. See paragraphs 4.4.6 and 4.3.9, respectively, for an explanation of these processes. The sync information also is transferred through a sync lamp driver to the SYNC lamp which indicates, when lit to full brilliance, that a hard sync condition exists; when lit dimly, that a sync condition exists but probably excessive noise is superimposed on the PCM signal; and when not lit, indicates clock and PCM are not synchronized. When processing RZ type PCM, $\overline{CLK}$ and $\overline{Z}$ are transferred to the main mixer and are processed in the same manner as described for CLK and U.

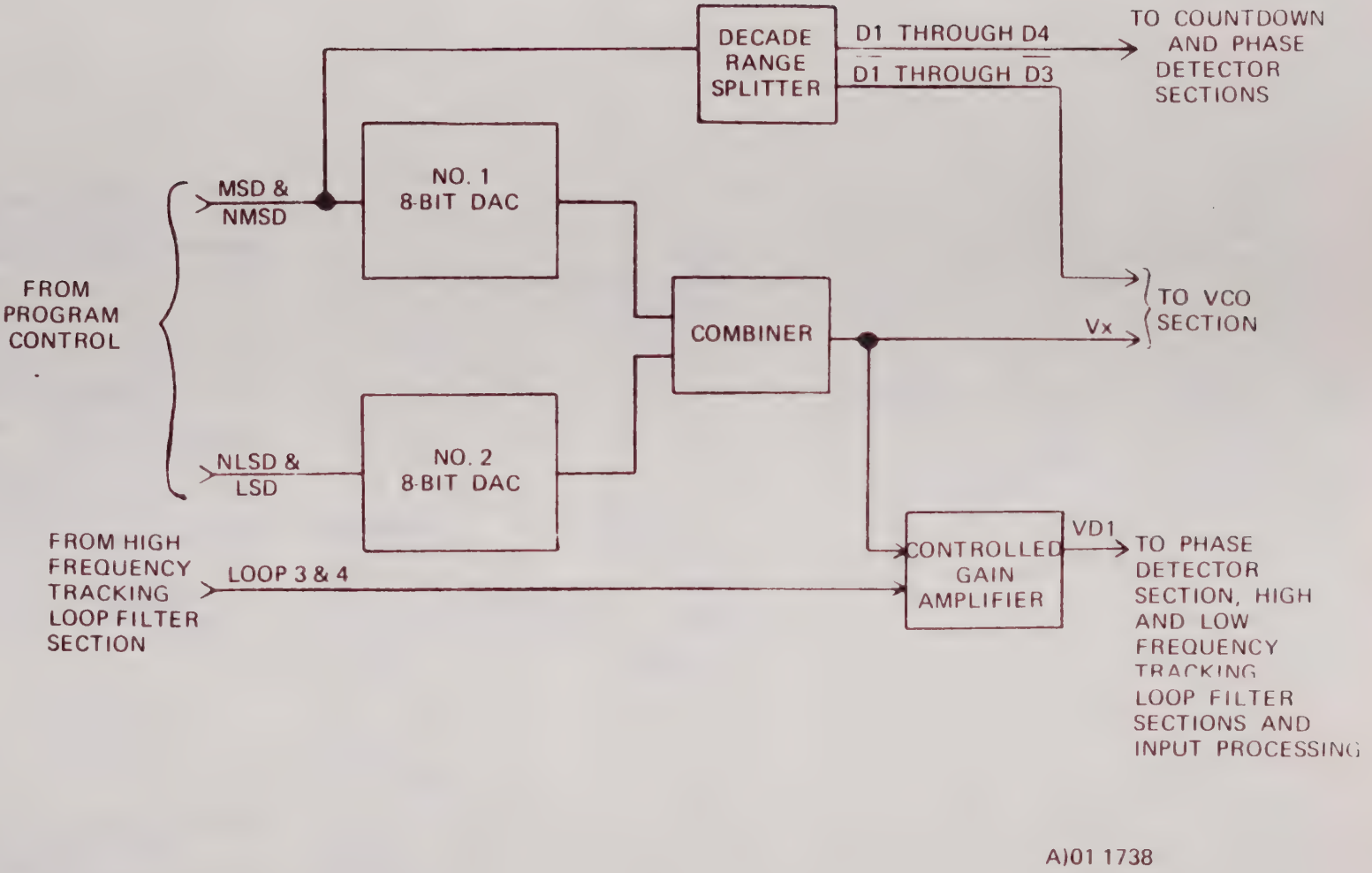


Figure 4-20. DAC and Decade Range Splitter Section, Detailed Functional Block Diagram

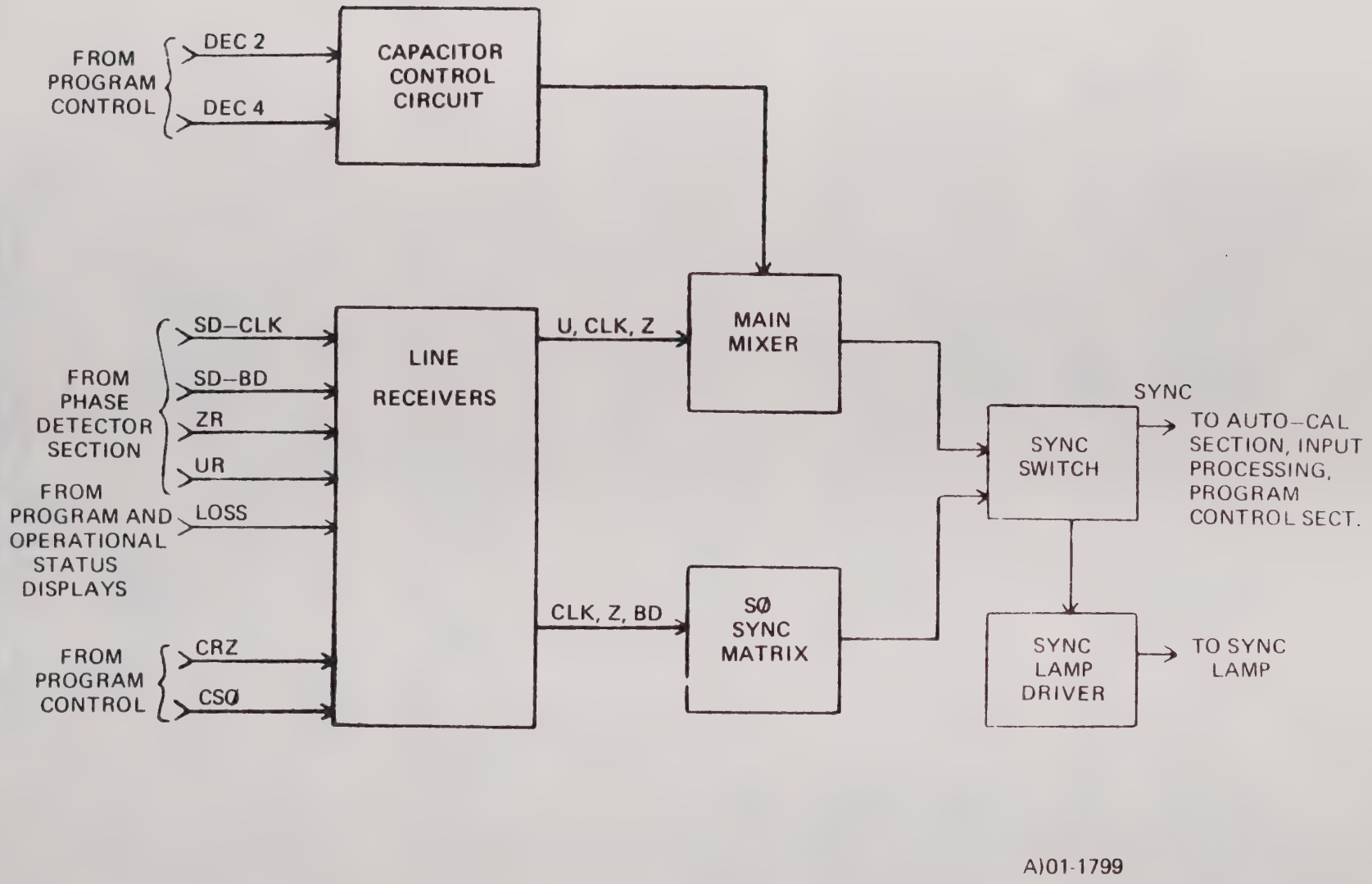


Figure 4-21. Sync Detector Section, Detailed Functional Block Diagram

When processing NRZ, DM or RZ type PCM, the main mixer provides a sync indication for at least 64 periods when there are no data transitions in the input signal, that is, when the input signal contains all ONEs or all ZEROs. During this period of time, U or Z, as applicable, is not present; therefore, it is assumed that synchronization exists. However, when processing SØ type PCM, the sync detector section has an extended requirement of providing a sync indication for at least 2000 bit periods when there is no data transition in the input signal. To implement this requirement, the SØ sync matrix compares $\overline{CLK}$, Z and $\overline{BD}$. This auxiliary circuit, which is enabled only when processing SØ type PCM, provides an indication of synchronization when the input data contains all or mostly ONEs or all or mostly ZEROs and, of course, when the data and clock are synchronized. When data transitions of the SØ input data occur most frequently, that is, maybe once every 64 bit times, the sync indication is obtained from the main mixer where U and $\overline{CLK}$ are being compared. The sync indication from either the main mixer or SØ sync matrix is ORed in the sync switch and from there is processed as explained previously.

The capacitor control circuit, under control of DEC 2 and DEC 4 from program control selects additional capacitors for an integrator circuit in the main mixer as the bit rate is decreased. When the bit rate is 10^4 or above, only one capacitor is used. For bit rates of 10^2 and 10^3, an additional capacitor is added to the integrator circuit and for bit rates of 10^0 and 10^1, a third capacitor is added to the integrator circuit.

4.5 CODE CONVERTER GENERATOR AND LINE DRIVERS FUNCTIONAL AREA

The code converter code generator and line drivers functional area is shown in figure 4-22. Because this functional area contains only two sections, both the code converter section and the code generator and line drivers section as well as the detailed interconnects of both sections are shown and identified in figure 4-22. A detailed explanation of each section is given in the following paragraphs.

4.5.1 Code Converter Section

The code converter section receives the BD-NRZ signal from the phase detector section of the phase lock loop functional area. This signal is converted to NRZ type PCM which is applied to the code generator section. During this process, Ø1, Ø2, Ø3 and Ø4 clocks are regenerated for the conversion process and also to provide the line drivers with properly phased clocks for external use. The code converter section is controlled by levels DM, S·SØ+SØ·M and RZ +L, received from the program decoder in the program control functional area. The signals from the phase lock loop functional area (BD-NRZ, from the phase detector section and the four phases of clock from the countdown section) are applied through line receivers. The BD signal is derived from the complementary inputs of BD-NRZ, CLK is derived from complementary clocks Ø1 and Ø3 and QUAD CLK is derived from complementary clocks Ø2 and Ø4.

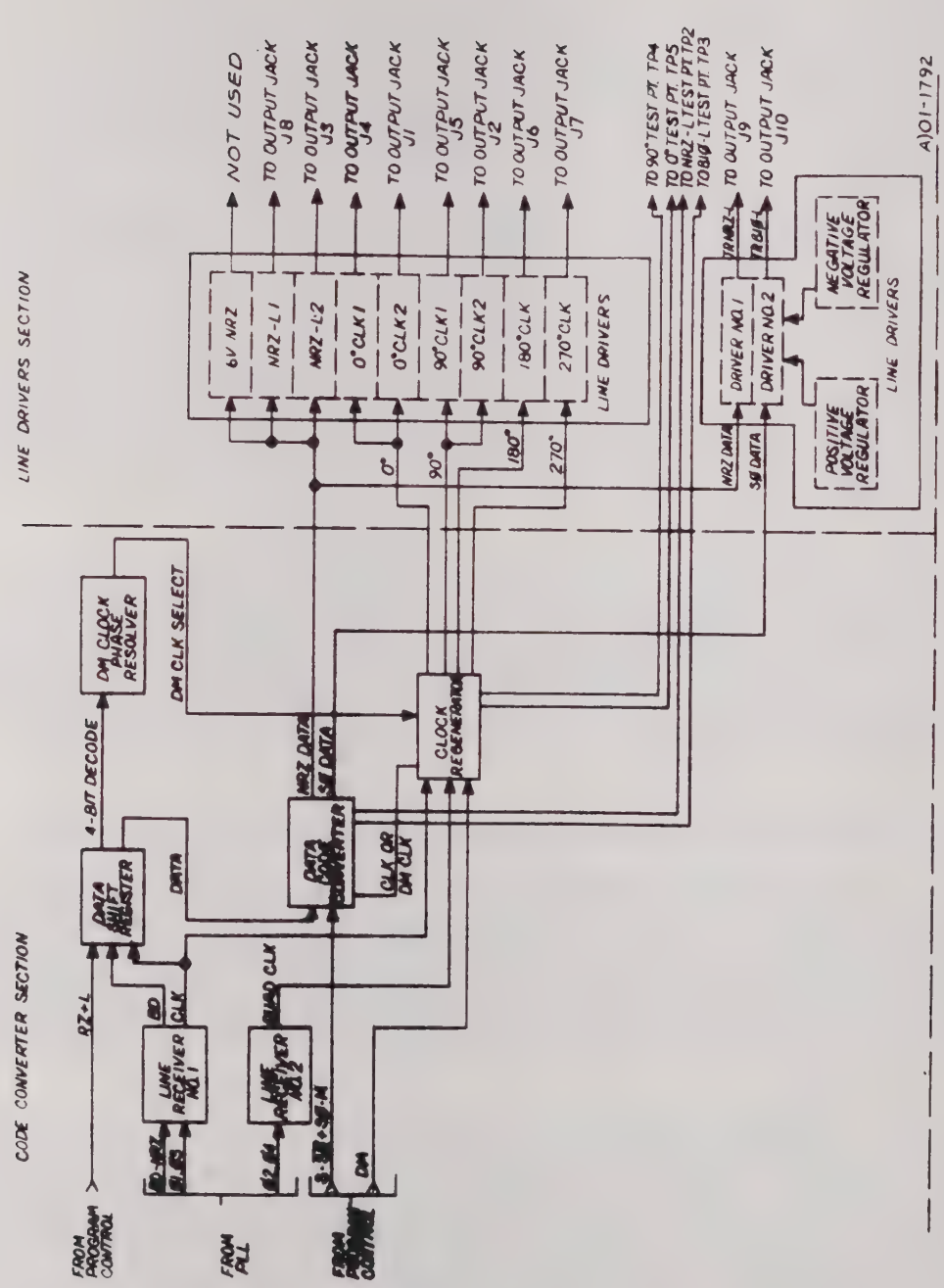


Figure 4-22. Code Converter and Line Drivers, Functional Block Diagram

When processing RZ, NRZ-L or BiØ-L type PCM, control level RZ+L is high and causes the data shift register to clock BD through to the data code converter one bit at a time. During this time, the 4-bit deccde output is not used. When processing any of the mark (M) or space (S) type PCM, control level RZ+L is low and causes the data shift register to operate as a 4-bit shift register in which the last four bits are stored. During this time, two consecutive bits are decoded to provide data. In addition, when processing DM-M or DM-S type PCM, the 4 bits are decoded to provide a signal for the DM clock phase resolver which selects one of the two possible phases available in the clock regenerator that is used to convert the data.

The clock regenerator using CLK, QUAD CLK, DM and DM CLK SELECT provides the required phases of CLK or DM CLK to the data code converter for code conversion. It also provides 0°, 90°, 180° and 270° clocks which are phase related to the clocks used during code conversion. These quadrature clocks are applied through line drivers for external use. The NRZ-L and SØ-L data from the data code converter and 0° and 90° clocks from the clock regenerator are transferred to test points located on the front panel.

4.5.2 Line Driver Section

The line driver section accepts all four clock phases, along with NRZ data and BiØ data and produces zero to +3 volt output signals. Drivers on the LDR024 card accepts NRZ data and SØ data and produce bipolar signals that can be varied from ±1 volt to ±3 volts. These outputs are provided to drive tape recorders, but only SØ data is used as an output driver. The other driver port is not used in this unit.

The positive and negative voltage regulators provide regulated voltages for operation of the drivers on the LDR024 card which process the data for the tape recorder outputs. All output lines are terminated at BNC type connectors located on the rear panel of the bit synchronizer. Each output is designed to drive a 50 ohm terminated load through a 50 ohm coaxial cable.

4.6 PROGRAM CONTROL FUNCTIONAL AREA

This section of the program control functional area is shown in figure 4-23 and explained in the following paragraphs. After an overall description of this functional area, each of its sections is explained in more detail. For ease of reference, each block in **figure 4-23 contains the figure number of its detailed functional block diagram.**

Figure 4-23. Program Control, Functional Block Diagram

The data distributor accepts binary coded data from an external source to program the selectable functions of the bit synchronizer. When the MANUAL-PROGRAM switch is in the PROGRAM position, the data is transferred to the program storage section.

The program storage section basically contains all front panel controls and four 8-bit storage registers whose outputs are transferred to the program decoding section. The position of the MANUAL-PROGRAM switch specifies whether the information from the front panel controls or the data distributor section is loaded into the storage registers. Switches S2 and S3 allow the operator to selectively override program specified contents of the storage registers.

The decoding section accepts the outputs of the storage registers and provides the logic levels required for the operation of the bit synchronizer.

4.6.1 Data Distributor Section

Refer to figure 4-24. The remote programming from external equipment interfaces through connectors J17/J18 on the rear panel of the bit synchronizer. These connectors are used for both data distributor section and program verify section mode of operation.

The programming information is contained in four 16-bit words which are loaded bit parallel, word serially. The four 16-bit words input to the bit synchronizer the same parameters that are, in manual mode, input from the front panel controls, however, to accept the programmed data, the MANUAL-PROGRAM switch must be in the PROGRAM position. Each of the four words is divided into an instruction, instruction address and unit address.

The instruction, bits CB0 through CB7, specifies the parameters to be input. Table 2-4 gives the bit assignment for each instruction. These bits are applied through data word buffers to one of the four 8-bit registers in the program storage section as specified by bits CB8, CB9, and CB10, which comprise the instruction address. Bits CB8, CB9, and CB10 of the instruction address are decoded in the write decode circuit to provide the four WRITE levels which direct the instruction into the assigned 8-bit storage register. When TRANSFER STROBE and WRITE EN are received from the unit address decode, this causes the instruction to be transferred to the specified 8- bit storage register. The four bits comprising the unit address are CB12, CB13, CB14, and CB15. The bit synchronizer is pre-assigned a certain unit address; when the proper unit address is received, the unit will then be enabled to either WRITE into the program storage register or READ the output of storage registers through the program verify section. The WRITE command is received in the unit address section where a selection is made as to which circuits will be enabled according to the desired mode of operation.

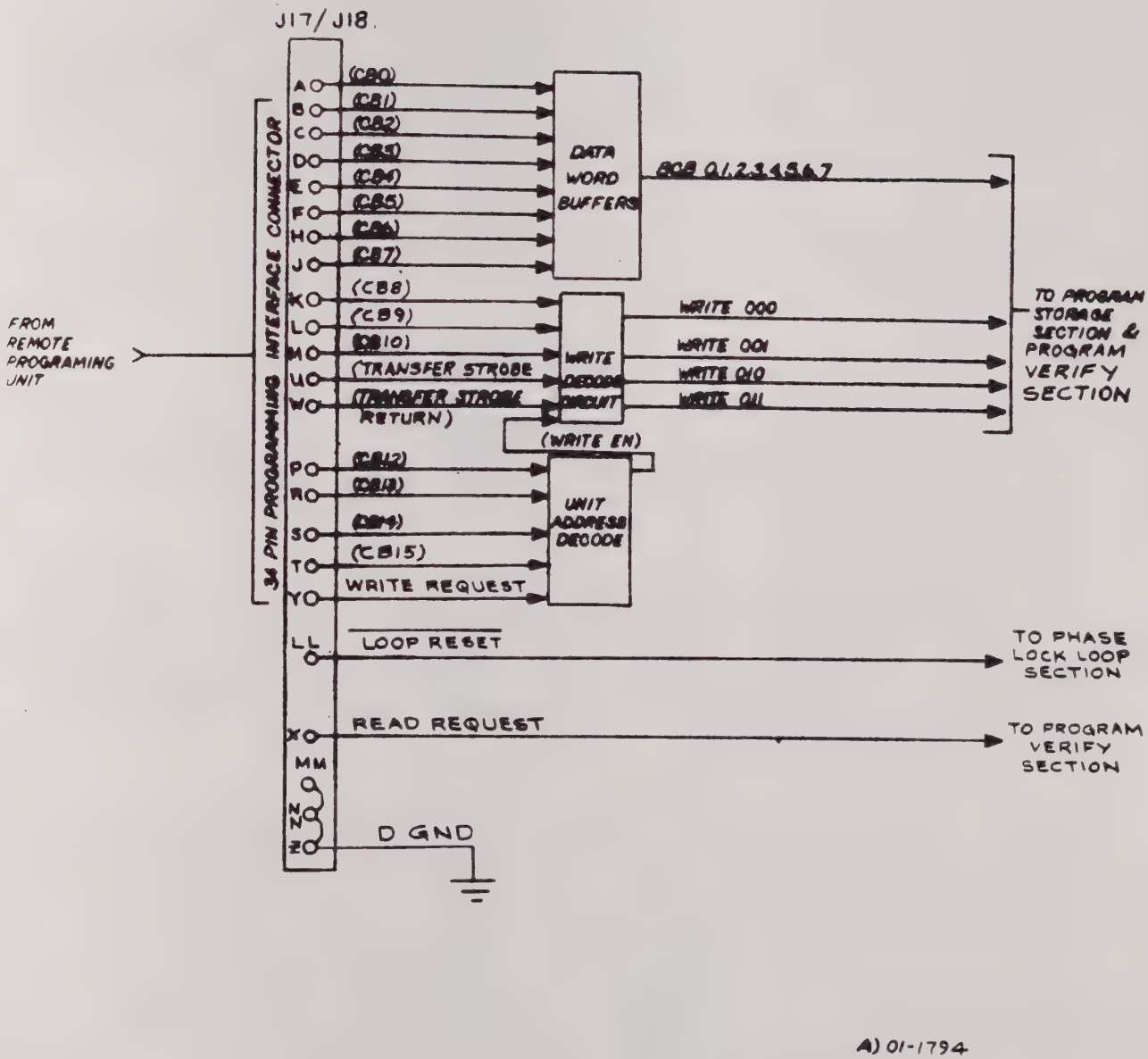


Figure 4-24. Data Distributor Section, Detailed Functional Block Diagram

4.6.2 Program Storage Section

Refer to figure 4-25. When MANUAL-PROGRAM switch is in PROGRAM position, information, as directed by the program is output from the four 8-bit storage registers. When MANUAL-PROGRAM switch is in MANUAL position, information, as directed by front panel controls, is output from the four 8-bit storage registers.

When MANUAL-PROGRAM switch is in PROGRAM position, updated information can be stored by setting switch S2 to the type of information to be overridden, setting the appropriate front panel switch to the position indicating the desired new information, and then depressing OVERRIDE pushbutton. As an example, if the bit synchronizer is programmed to receive RZ type PCM and this is to be changed to NRZ-L, rotate switch S3 to CODE position, rotate CODE switch S4 to NRZ-L position and then depress OVERRIDE pushbutton S2. All front panel switches that provide inputs to the storage registers provide those inputs in binary code. The binary code provided by each position of each switch is as indicated in table 2-4.

The outputs of the four 8-bit storage registers are transferred to the program decoding section and the program verify section where control levels required for the operation of the bit synchronizer are generated. Binary coded values of the significant digits of the bit rate from registers A3A1 and A3A2 and binary coded values of the multiplier of the bit rate (RDEC 1, 2, 4) from register A3A3 are also transferred to the BIT RATE indicator on the front panel. The $\overline{\text{POL +/-}}$ output from A3A3 also is transferred to POLARITY indicator on the front panel. The IB1 and IB2, from register A3A3 also are transferred to input processing functional area where these two bits select data input 1, 2, 3, or 4.

4.6.3 Program Decoding Section

The program decoding section (see figure 4-26) consists of the logic for the polarity inverter, bit rate multiplier, source select adder, loop bandwidth adder, program decoder, and decade adder with buffer. All inputs to this circuit are from the program storage register section.

$\overline{\text{POL +/-}}$ is inverted to become POL +/- and is routed to the variable gain and offset amplifier section of the input processing functional area to control the polarity of the input data.

When DM is low (code selected is other than DM), the bit rate multiplier provides outputs that are duplicates of the inputs; however, when DM is high, the bit rate as represented in binary form by the values of the inputs is doubled and is available in binary form at the output. If a carry is generated from this doubling process, DEC ADD

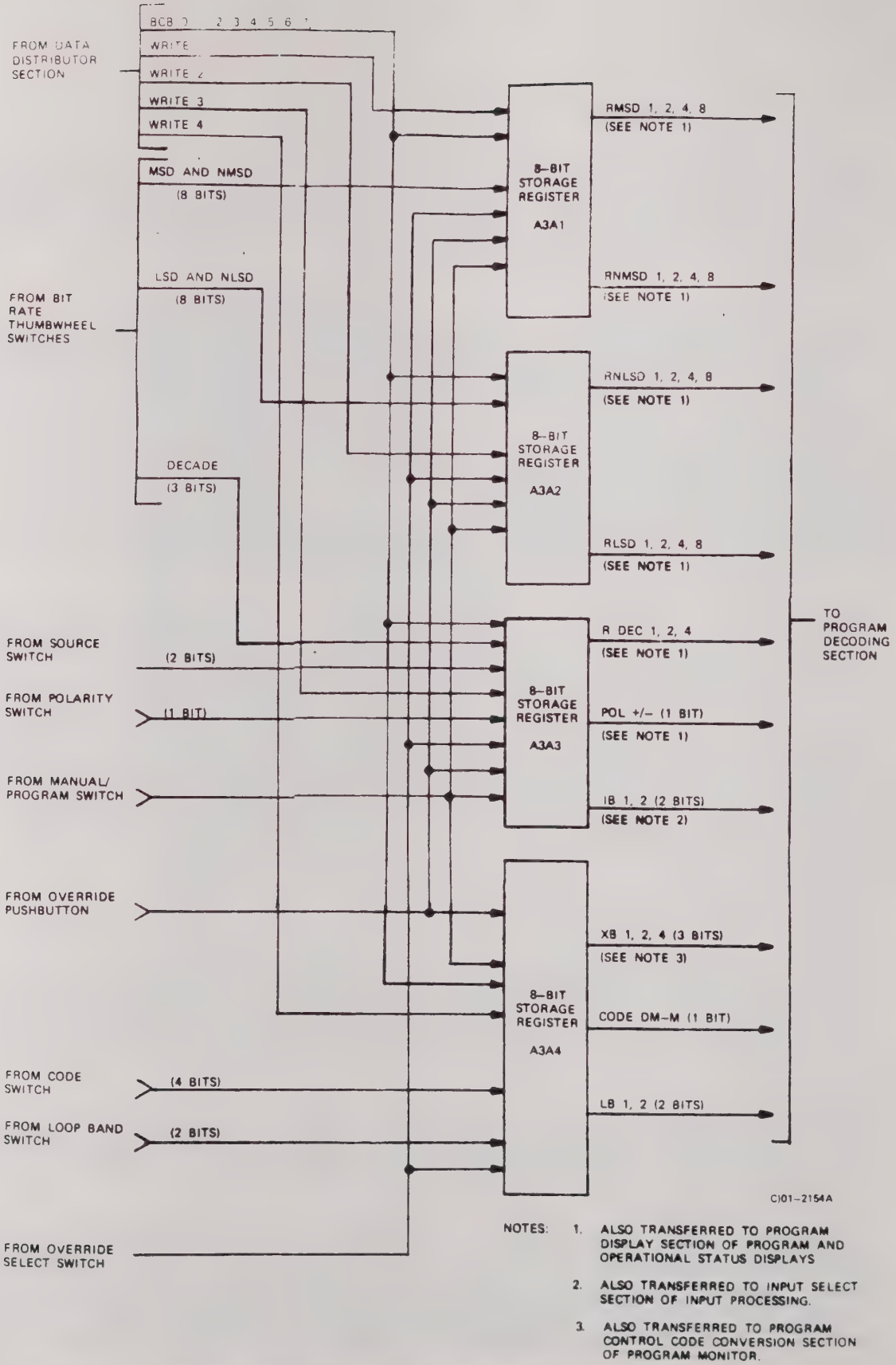


Figure 4-25. Program Storage Registers, Detailed Functional Block Diagram

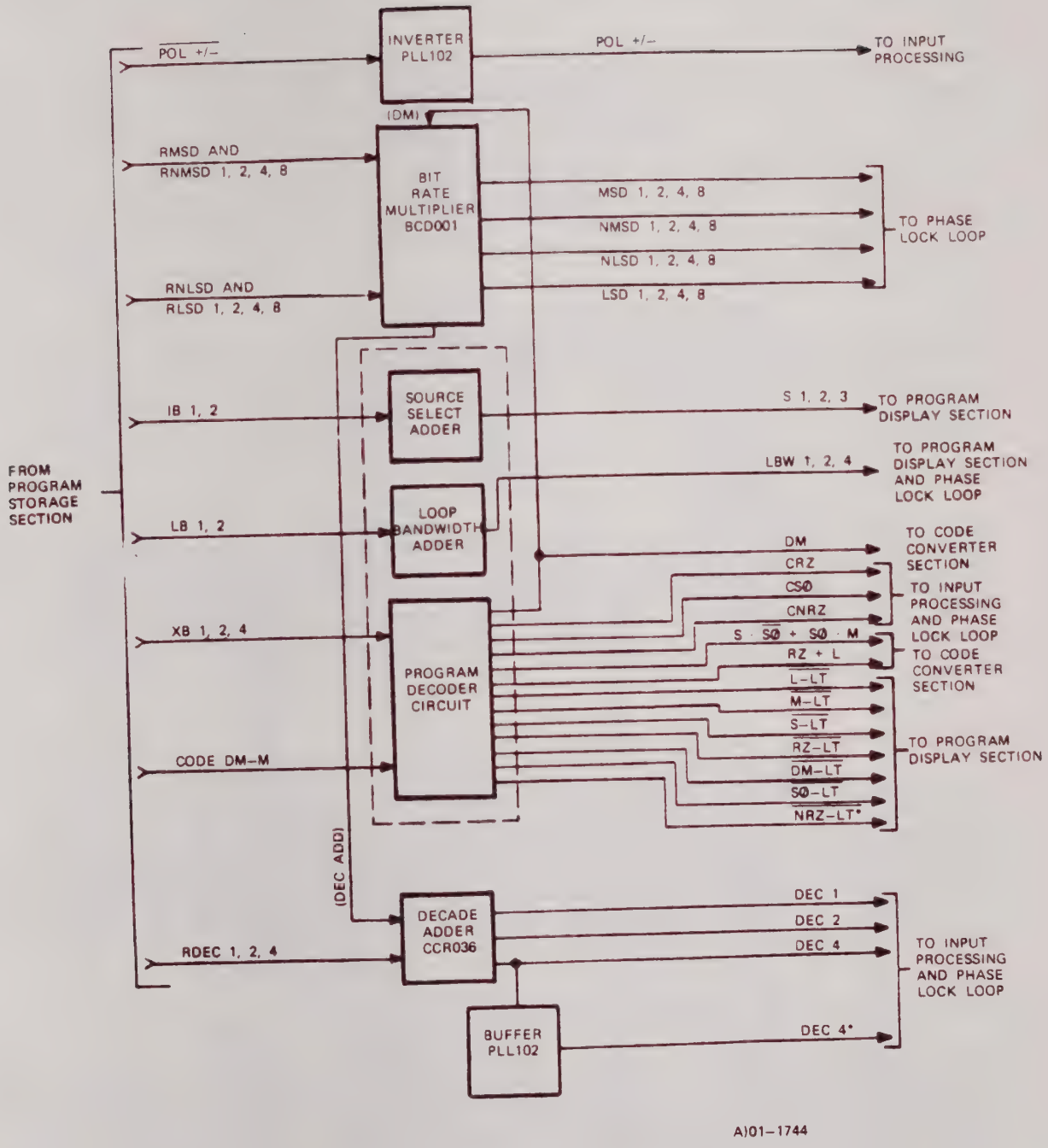


Figure 4-26. Program Decoding Section, Detailed Functional Block Diagram

is applied to the decade adder which increases the value of the bit rate multiplier representated by the binary values of DEC 1, DEC 2 and DEC 4.

The source select adder receives two bits, IB1 and IB2, which can be decoded to represent four possible outputs representing decimal numbers 0 through 3. The source select adder generates an additional bit to provide a 3-bit output representing decimal numbers 1 through 4 which the SOURCE indicator requires to display numbers 1 through 4, respectively. Decimal numbers 5 through 7, which also can be decoded from the 3 bits, are not valid. The loop bandwidth adder operates in the same manner as the source select adder to provide the proper inputs to the LOOP indicator.

The program decoder circuit receives XD1, XD2', XD4 and CODE DM-M from the program storage section. These four bits, when decoded, represent the nine possible PCM codes that the bit synchronizer can process. By decoding and combining these bits, control levels, as shown in figure 4-26, are generated and selectively routed to all functional areas of the bit synchronizer.

The decade adder normally provides three output bits whose values are the same as the three input bits. These three bits, when decoded, represent the multiplier of the bit rate. When processing DM type PCM, and when the DEC ADD signal is present, the output bits are changed to represent one number higher than that represented by the input bits.

4.6.4 Program Verify Section

The program verify section (see figure 4-27) accepts the instruction bits from the program storage registers, and with the instruction address decode from the data distributor selects one of the four 8-bit program verify formats. The output from the program verify section is sent to the external program equipment via connectors J17/J18 on the rear panel. The 8-bit verify instruction is described in the program section in section II.

4.7 PROGRAM AND OPERATION STATUS DISPLAYS FUNCTIONAL AREA

The program and operational status displays functional area, as shown in figure 4-28, includes the operational status display section, the program display section and a lamp test section. This functional area includes all indicators (lamps, displays and meters) on the front panel and their associated circuits. A detailed description of the three sections is given in the following paragraphs.

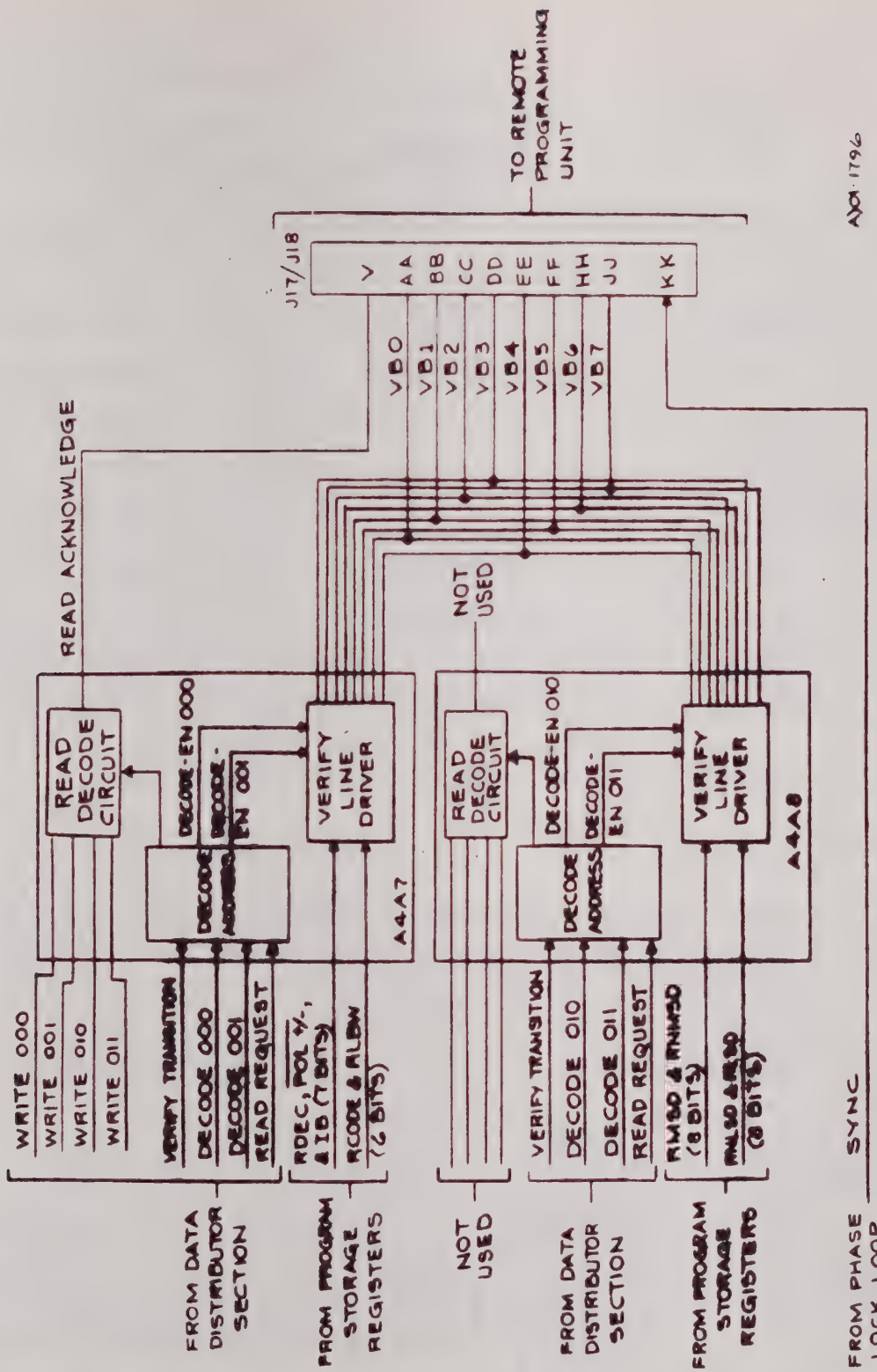


Figure 4-27. Program Verify Section, Detailed Functional Block Diagram

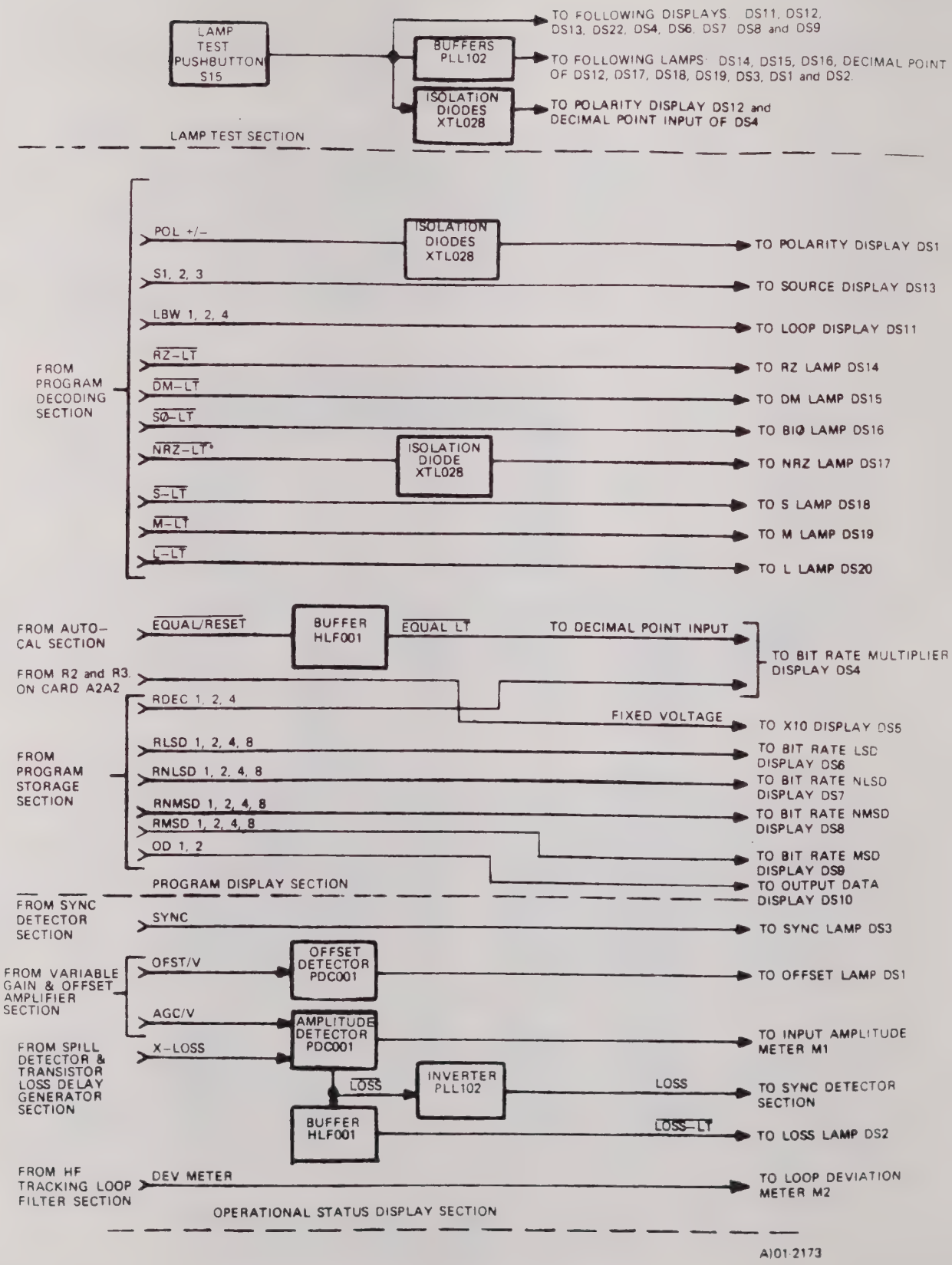


Figure 4-28. Program and Operational Status Displays, Functional Block Diagram

4.7.1 Operational Status Display Section

The operational status display section processes those signals which represent the operating conditions of the bit synchronizer. The sync detector section of the phase-locked loop functional area provides SYNC LT to light SYNC lamp DS3 when the incoming data is synchronized with the generated clock. The variable gain and offset amplifier section of the input processing functional area provides OFST/V to the offset detector and AGC/V to the amplitude detector. When OFST/V is between +2 and -2 volts, representing the maximum allowable offset of the incoming PCM signal, OFFSET lamp DS1 is not lit. When OFST/V exceeds these limits, OFFSET lamp DS1 is lit. AGC/V, whose normal range is between -0.5 and -4 volts, causes INPUT AMPLITUDE meter M1 to indicate the amplitude of AGC/V. In addition, when AGC/V goes positive or when X-LOSS is received from the spill detector and transition loss delay generator section of the input processing functional area, LOSS is generated. This signal is applied through a buffer to light the LOSS lamp DS2 and also through an inverter to the sync detector section of the phase-locked loop functional area where it provides the LOSS signal. The DEV METER signal from the meter driver (loop deviation monitor section) of the detector status interface drives the zero center LOOP DEVIATION meter, M2, and gives an indication of the error signal amplitude required to pull the voltage controlled oscillator to its proper operating frequency.

4.7.2 Program Display Section

The program display section includes nine light emitting diodes (LED) displays arranged in two groups, and seven CODE LED lamps. The Bit RATE display includes six LEDs which indicate the bit rate as stored in the program storage registers. Each LED, except DS5, is designed to accept four bits which cause the LED to display a numeral representing the BCD value of the four bits. DS5 is hard-wired to display X10. Because the highest required numeral is 6, BIT RATE multiplier DS4 decodes only three bits. These LEDs also can display a decimal point to the left of the numeral; this capability is used in the NMSD LED DS8 and in the multiplier LED DS4. In the former, the decimal point is hard-wired to provide the decimal point between the most significant and the next to the most significant numerals of the bit rate and in the latter, the decimal point is used as an indicator which, when lit, indicates that an automatic calibration cycle is occurring. The decimal points indication in DS4 is controlled by EQUAL/RESET received from the AUTO-CAL section in the phase-locked loop functional area. This signal is applied through a buffer and becomes EQUAL LT which is applied to DS4.

The remaining three LEDs that are grouped into an assembly include SOURCE DS13, POLARITY DS12 and LOOP DS11. DS11 and DS13 are identical to the LEDs used in BIT RATE display but, because the highest numeral required is 4, only three bits drive each. POLARITY display DS12 is driven by one bit, POL +/-, and indicates the polarity as + or -.

The seven CODE LED lamps include RZ DS14, DM DS15, BiØ DS16, NRZ DS17, S DS18, M DS19 and L DS20. Each of these lamps has one side connected to a +5 volt source; the other side of each lamp is driven by its associated signal from the program decoding section of the program control functional area. Thus, when the control signal goes low, its associated lamp lights. When processing RZ type PCM, only RZ lamp is lit. When processing NRZ, BiØ or DM type PCM, two lamps light; one to indicate the basic type of PCM and the other to indicate whether the PCM is level (L), mark (M) or space (S).

4.7.3 Lamp Test Section

The lamp test section, when LAMP TEST pushbutton S15 is depressed, lights all LED lamps, causes the decimal point serving as the AUTO-CAL indicator to light, causes + to appear on Polarity indicator and causes the numeral 8 to appear on the remaining LED displays. To provide isolation between the signals that normally control the lamps and the lamp test levels, the lamp test level is applied through an associated buffer to lamps DS1 through DS3, and DS14 through DS20. An isolation diode is used between S15 and DS12; another isolation diode is used between S15 and the decimal point input of DS4. Isolation diodes are also included in the signal lines for $\overline{\text{NRZ-LT*}}$ and $\overline{\text{POL +/-}}$ to prevent interaction. All LEDS that display numerals have noninterfering lamp test inputs that are connected directly to the LAMP TEST pushbutton.

4.8 PRINTED CIRCUIT CARD DESCRIPTIONS

The following paragraphs give a detailed description of each circuit contained on the plug-in printed circuit cards used in the bit synchronizer. Each circuit is referenced back to its next higher functional description to provide complete continuity within the theory of operation section. The schematic drawings for the pc cards are located in section VI.

4.8.1 Input Select Type INP050

The type INP050 card (see schematic drawing 460-0986) contains the circuits of the input select section (see figure 4-3). These circuits include input signal select, termination select and the ac/dc coupling select. The card also contains an external clock receiver which is a part of the low frequency threshold detector section (see figure 4-10) and an inverter which is part of the program display section (see figure 4-28). Each of these circuits is described in the following paragraphs.

Input Signal Select Circuit. The input signals from the four rear panel BNC connectors, J11 through J14, are fed to the signal select relays K1 through K4. The relay control logic, which includes U1B,

U1D, U2C, U2E, U2F, U3A, U3B, U3C and U3D, decodes the binary code input IB1 and IB2 from the program storage register. The decoded output is four decimal lines, one for the low side of each relay coil. Whenever the output of an individual line is low, the relay associated with that line is energized, thus selecting one of the four inputs. Table 4-5 shows the relationships among the logic levels of IB1 and IB2, the state of the relays and the input signal selected. The selected input signal is coupled directly to or through C1 to the SIG IN output pin 9 and across R24 to TP1. The SIG IN RET is fed to pin 37.

Table 4-5. Input Signal Selection

DATA INPUT	LOGIC LEVEL		RELAY ENERGIZED	INPUT SIGNAL SELECTED
	IB1 PIN 7	IB2 PIN 6		
J14 No. 1	0	0	K1	IN 1 (pin 17) IN 1 RET (pin 18)
J13 No. 2	0	1	K2	IN 2 (pin 28) IN 2 RET (pin 29)
J12 No. 3	1	0	K3	IN 3 (pin 22) IN 3 RET (pin 23)
J11 No. 4	1	1	K4	IN 4 (pin 34) IN 4 RET (pin 35)

Termination Select Circuit. The termination select relay K5 is controlled by the 50 ohm input at pin 38 from the HIGH/LOW TERMINATION switch S18. When the switch is in the LOW (ground) position, K5 is energized and R1 is connected across the SIG IN and SIG RET lines ahead of C1; thus, terminating the input signal in 51 ohms. When the switch is in HIGH (+5 volts) position, K5 is deenergized and the input signal is terminated in the input of the driver circuit (a high impedance).

Ac/dc Coupling Select Circuit. The inputs to the ac/dc coupling select gate U1A and DEC 4 and CSØ from the program control. DEC 4 and CSØ are applied via pins 5 and 4, respectively, to AND gate U1A. The output of U1A is inverted by U2B and applied to the low side of K6 coil. When either DEC 4 or CSØ is low, K6 is energized, shorting out C1 to provide dc coupling for the input signal. When DEC 4 and CSØ are both high, the high output from U2B keeps K6 deenergized and the input signal is ac coupled. The choice of coupling depends upon the type (code) and data bit rate of the selected signal. For CSØ signals with bit rates greater than 1 x 14 bps, ac coupling is in effect; for all other combinations of codes and bit rates, the input signal is dc coupled. Suppression diodes are connected across coils of all relays.

External Clock Receiver. The external clock receiver consists of FET Q1, Q2, U4 and associated parts. The EXT CLK is fed to pin 31 and coupled through C2 and R3 to the gate of Q1. The EXT CLK is referenced to ground by R5 and the return (RET) at pin 32 is grounded. The gate of Q1 is referenced to ground through R6. FET Q1 operates as a source follower with R4 and R7 serving as a divide-by-two voltage divider for the EXT CLK signal and as the source load resistor. Networks consisting of R2 and C3 and R8 and C5 are used to decouple the power supplies. The EXT CLK output appearing at the junction of R4 and R7, which is reduced in amplitude by half, is fed across R19 and C4 to the base of U4B and across R20 and R15 to the base of U4C. The base of U4C is bypassed by C6 so that only dc is present for bias. Integrated circuit U4B and U4C are emitter followers with R13 and R14 serving as the load resistors. Integrated circuit U4A is a differential amplifier and the right hand base (pin 2) is referenced to the dc output at the emitter of U4C. The EXT CLK appearing at the emitter of U4B is fed to the left hand base (pin 4) of U4A and also across R23 to TP2. Transistor Q2 and its associated components form the current source for the emitters of U4A and regulate the output at the collectors of U4A. The outputs, EXT U and $\overline{\text{EXT U}}$, from the collectors of U4A are fed via pins 10 and 11, respectively, to low frequency threshold detector section. Resistors R3, R9, R10, R11, R12 and R13 are damping resistors to prevent oscillations. Capacitor C7 in the +5 volt line provides a bypass for high frequencies.

Inverter. The EXT input which is applied to pin 8 is inverted in U2A to produce $\overline{\text{EXT LT}}$. The EXT input is derived when EXT/INT CLOCK switch is in the EXT position. The $\overline{\text{EXT LT}}$ output is fed via pin 9 to the EXTERNAL CLOCK indicator lamp on the front panel.

4.8.2 Signal Level Control Type SLC029

The type SLC029 card (see schematic drawing 460-0921) contains circuits included in the variable gain and offset amplifier section (see figure 4-4) and circuits contained in the low frequency AGC and offset control section (see figure 4-11). The variable gain and offset amplifier section contains a test point driver, a variable gain amplifier, polarity current (I) switch, offset current (I) correction circuit, output routing current (I) switch, a low frequency/high frequency AGC select circuit and a low frequency/high frequency offset select circuit. The low frequency AGC and offset control section contains the voltage-to-current converter, LF-1/2T, LF-3/4T, LF-OFST and LF-RZ line receivers, low frequency offset generator, low frequency AGC generator, SØ offset correction circuit, RZ offset safety circuit, overload and offset detectors and acquisition switch. Each of these circuits is explained in the following paragraphs.

Test Point Driver. The PCM signal, SIG IN, from the input select card (see schematic drawing 460-0986) is applied to pin 35 and is fed to the junction of resistors R27, R10 and capacitor C4 shown in schematic drawing 460-0921. Resistors R10, R11 and R13 form a divide-by-three

attenuator. Resistors R9 and R14 provide a bias about ground. Variable resistor R13 zeros the dc offset in the signal appearing at pin 37 (input TP). Variable capacitor C3 and fixed capacitor C4 provide suppression of the leading edge transient. The input signal, at 1/3 of the original amplitude, is fed across R8 to the base of Q4 and across R12 to the base of Q5; both transistors are emitter followers. The output of Q4 and Q5 is fed to the bases of Q1 and Q2, respectively, the test point drivers. The current source for supplying base drive to Q1 is Q3, CR1, R2, R3 and R4. Likewise, Q6, CR2, R17, R18 and R19 for supplying drive to the base of Q2. The test point drivers, Q1 and Q2, are emitter followers with the combined output taken across the current limiting resistors, R6 and R7. The output signal is fed from pin 37 to the IN test point TP1 on the front panel. Resistors R5, R8, R12 and R20 are damping resistors for the elements of Q4 and Q5. The GND test point TP6 on the front panel is connected to ground at pin 36 through isolation resistor R15. Networks R1-C1 and R16-C2 are decoupling networks for Q1 and Q2, respectively.

Variable Gain Amplifier. The major part of the variable gain amplifier (see schematic drawing 460-0921) is U2. Transistors U2Q1 and U2Q2 are configured to form a differential pair and U2Q3 and U2Q4 are connected as diodes. The remaining parts of the variable gain amplifier are U1Q5 temperature compensation, U3 negative current driver and current mirror, U4Q1, U4Q2 and U4Q5 current amplifiers, Q7, Q8 tracking current mirror, Q17 current source, and Q18 control of variable gain amplifier. Details of the variable gain amplifier are described in the following paragraphs.

The PCM signal input to the variable gain amplifier is across R27 which, in conjunction with CR4 and CR5, comprises the signal voltage-to-current conversion circuit. The input signal is applied to the differential amplifier at the base of U2Q1. The base of U2Q2, the opposite side of the amplifier, is grounded. Diodes CR4 and CR5 clamp the base of U2Q1 at plus and minus 0.4 volt. The diode connected transistors U2Q3 and U2Q4 provide a variable resistance that shunts, depending on the amount of AGC voltage, a part of the input PCM signal; the remaining portion of the input PCM signal is applied to the differential amplifier. The PCM signal, in the form of U2Q1 and U2Q2 collector currents, is applied to the polarity current (I) switch.

Signal VAGC is obtained from the LF/HF AGC select circuit and applied to voltage divider consisting of R53 and R54. The voltage developed across R54 is applied to the base of Q18A which is one-half of a differential pair. The other half of the differential pair, Q18B, has its base biased slightly negative by the network consisting of R58, R59 and R60. The value of R60, a select-by-test resistor, is selected to set the gain of the amplifier. Resistor R57, diode-connected transistor U1Q5 and resistor R84 form a temperature compensation network to stabilize the base current of Q18B. The collector output of Q18B, developed across R64 and the diode-connected transistor U4Q5, is fed to the bases of the parallel connected transistors U4Q1 and U4Q2 which, in turn, control the amount of current through the emitter of U2Q1

and U2Q2. The signal at the collector of Q18A, which is the opposite to that at the collector of Q18B and developed across U3Q3 and resistor R63, is applied through R55 to the base of Q17. The output signal developed across emitter resistor R52, is applied to the bases of transistors U3Q1 through U3Q4. Parallel connected transistors U3Q1 and U3Q2 and emitter resistor R62 control the amount of current flowing through shunt diodes U2Q3 and U2Q4.

Transistor U3Q4 and emitter resistor R61 are part of the current mirror circuit. Compensation for the current generated at the collector of U3Q4 is provided by U2Q5 which, together with R75, C5 and R50, form part of the U3Q4 emitter circuit. The collector of U3Q4 feeds the tracking current mirror circuit consisting of Q7 and Q8. Emitter source voltage (+6.2 volts) for Q7 and Q8 is obtained from Zener diode CR3 and applied through R22 to Q7A and through R21 and R23 to Q7B. Transistor Q7A acts as the collector load for U3Q4 and the signal developed across this transistor is fed to the base of Q8 which operates as an emitter follower. The output of Q8, across R25, feeds the base of Q7B. Potentiometer R21 adjusts the range of current flow through Q7B which feeds positive current to the base of U2Q1 and the diode-connected transistor U2Q4.

When VAGC is at 0 volts, the voltage developed at the collector of Q18B causes the emitter current of U2Q1 and U2Q2 to increase and the voltage at the collector of Q18A causes the positive and negative currents at diode-connected transistors U2Q3 and U2Q4 to decrease; this process causes a gain of 8. As the VAGC voltage decreases to -4 volts, the voltages at the collectors of Q18 switch sides, and cause the emitter currents of U2Q1 and U2Q2 to decrease and the currents through diode-connected transistors U2Q3 and U2Q4 to increase; this process causes a gain of 1/8.

Polarity I Switch. The polarity I switch (see schematic drawing 460-0921) consists of U1Q1 through U1Q4 differential current switches, Q10 and Q11 polarity driver differential amplifiers and associated parts. When signal POL (+/-) is high (a +5 volt level when POLARITY switch on the front panel is in + position), the base voltage of Q11 is more positive than the 1.5 volts on the base of Q10 which is obtained from the voltage divider R33 and R34; therefore, transistor Q11 is turned on and Q10 is turned off. The current through the common emitter resistor R37 causes the collector voltage of Q11 to drop to 5.1 volts. Since Q10 is turned off, its collector voltage remains at 6.2 volts as established by the voltage divider consisting of resistors R31 and R32 and Zener diode CR3. When signal POL (+/-) is low (a ground level when POLARITY switch on the front panel is in - position), the base voltage of Q11 is less positive than the 1.5 volts on the base of Q10; therefore, transistor Q11 is turned off and Q10 is turned on. Under these conditions, the collector voltage of Q11 is 6.2 volts and the collector voltage of Q10 is at 5.1 volts. These collector voltages are applied to two differential pairs of transistors and control which transistor in each pair is turned on.

Transistors U1Q3 and U1Q4 receive, via the common emitter connection, the PCM signal current from the variable gain amplifier. The other pair (U1Q1 and U1Q2) receives, via its common emitter connection, the complement PCM signal current from the variable gain amplifier. Thus, when POL (+/-) is high, the bases of the inside transistors are at a lower potential then the bases of the outside transistors. This causes the inside transistors to be off and the outside transistors to be on. Thus, the PCM signal is developed across R30 and the complement PCM signal is developed across R29. Conversely, when POL (+/-) is low, the inside transitors are on and the outside transistors are off, which switches the signal polarities so that the PCM input signal is developed across R29 and the complement PCM signal is developed across R30. These signals are then routed to the offset I correction circuit. Normal operation of the POLARITY switch routes the true PCM signal to R29 and the complement of the true PCM signal to R30. Source voltage for the collectors of the differential current polarity switches is obtained from the +15 volt source through transistor Q9 which is biased by resistors R31 and R32 and Zener diode CR3. Bias is such to produce +12 volts at the emitter of Q9.

Offset I Correction Circuit. The offset correction circuit (see schematic drawing 460-0921) consists of transistors U4Q3 and U4Q4 connected as a differential amplifier pair, transistor Q21 and associated parts. Transistor U4Q4 is biased at ground. Transistor U4Q3 receives the OFST/V signal from the LF/HF offset select circuit. The emitters of both transistors are returned through resistors R67 and R68 to the collector of Q21. Transistor Q21 with R71 and R69 form a constant current source. The collectors of U4Q3 and U4Q4 are connected to the collector circuits of the differential current switches (U1Q1 through U1Q4) which are part of the polarity I switch. This is where the true and complement PCM signals are amplitude normalized. By introducing additional current through the load resistors where these signals are developed, the baselines of both signals are equalized. When OFST/V is zero, the currents through U4Q3 and U4Q4 are equal. These same equal currents also flow through load resistors R29 and R30; thus, the baseline relationship between the true and complement signals is not affected. When OFST/V approaches +2 volts (to correct a positive offset) the current through U4Q3 increases and causes more current to flow through R30 which raises the dc baseline of the complement signal developed across R30. Simultaneously, the current through U4Q4 decreases and causes less current to flow through R29 which lowers the dc baseline of the true PCM signal developed across R29. When OFST/V approaches -2 volts (to correct a negative offset) a similar but opposite process occurs which lowers the dc baseline of the complement signal developed across R30 and raises the dc baseline of the true PCM signal developed across R29. The true and complement PCM signals which are now equalized in peak-to-peak amplitude, equally offset and polarity corrected, are routed to the output routing I switch.

Output Routing I Switch. The output routing I switch (see schematic drawing 460-0921) consists of a differential amplifier Q12A and Q12B, the routing switch Q13 through Q16 and the DEC 4 signal input circuit Q19 and Q20 with associated parts including Zener diode CR6. The true and complement PCM signals are applied to bases of transistors Q12A and Q12B, respectively. The differential amplifier boosts the signals and then routes each signal to a differential pair which directs each signal to a high frequency or low fequency input line as directed by the DEC 4 signal. When DEC 4 is low, Q20 is off and Q19 is on. Collector voltage from these transistors bias the differential switches so Q14 and Q15 are off and Q13 and Q16 are on. This biasing causes the true PCM signal to be routed through Q16 to become the LF INPUT signal and the complement PCM signal to be routed through Q13 to become the LF INPUT signal. When DEC 4 is high, Q20 is on and Q19 is off. Collector voltage from these transistors bias Q14 and Q15 on, and Q13 and Q16 off. This biasing causes the true PCM signal to be routed through Q15 to become the HF INPUT signal and the complement PCM signal to be routed through Q14 to become the HF INPUT signal.

LF/HF AGC Select Circuit. The LF/HF AGC select circuit (schematic drawing 460-0921) consists of differential pair Q39 and Q40, clamp diodes CR19 and CR21, isolation diodes CR20 and CR22, FET switches Q41 and Q42 and associated parts. When signal DEC 4 is high, Q40 and Q41 are off and Q39 and Q42 are on. This routes signal HF-AGC/V through Q42 to become signal VAGC which is used in the variable gain amplifier circuit. When signal DEC 4 is low, Q39 and Q42 are off and Q40 and Q41 are on. This routes signal LF/AGC/V through Q41 to become signal VAGC. Thus, when DEC 4 is high, VAGC is obtained from the high frequency AGC generator and when DEC 4 is low, VAGC is obtained from the low frequency AGC generator.

LF/HF Offset Select Circuit. The LF/HF offset circuit (see schematic drawing 460-0921) consists of differential pair Q62 and Q63, clamp diodes CR38 and CR39, FET switches Q65 and Q66 and associated parts. When signal DEC 4 is high, Q63 and Q65 are off and Q62 and Q66 are on. This routes signal HF-OFST/V through Q66 to become signal V OFST which is used in the variable gain amplifier circuit. When signal DEC 4 is low, Q62 and Q66 are off and Q63 and Q65 are on. This routes signal LF-OFST/V through Q65 to become signal V OFST. Thus, when DEC 4 is high, V OFST is obtained from the high frequency offset generator and when DEC 4 is low, V OFST is obtained from the low frequency offset generator.

Voltage-to-Current Converter. The voltage-to-current converter (see schematic drawing 460-0921) consists of operational amplifiers U8 and U9, inverters U7B and U7D, emitter followers Q30 and Q31, switch Q29 and associated parts. Signal VD1, which ranges from 0.5 to 5 volts dc, is applied through a switchable voltage divider to operational amplifier U8. The switchable voltage divider is formed by resistors R104 and R106 and transistor Q29; it is controlled by signals DEC 1 and DEC 2. When DEC 1, DEC 2 or both are high, the output of the

inverters U7B and U7D is low. This low level holds CR8 back biased which, in turn, holds Q29 off. Thus, signal VD1 is not attenuated at the input of U8. When DEC 1 and DEC 2 are both low, the output of inverters U7B and U7D is high which forward biases CR8 and Q29. With Q29 conducting, signal VD1 is divided across R104 and R106. Thus, the portion across R106, approximately one-tenth of the original amplitude of the VD1 signal, is applied to U8. The output of U8, which follows VD1 or one-tenth of VD1, is used in the AGC and offset generator circuits. This signal also is applied through R108, U9 and Q31. These parts are configured to operate as an inverting buffer with unity gain. Thus, the output at the emitter of Q31 is -VD signal which also is used in the AGC and offset generator circuits.

LF-1/2T, LF-3/4T, LF-OFST and LF-RZ Line Receivers. Identical line receivers are used for the LF-1/2T, LF-3/4T, LF-OFST and LF-RZ signals. These receivers convert differential currents to logic levels of 0 and 5 volts. Since the four circuits are identical, only the receiver for signal LF-1/2T is explained. The differential current signals (LF-1/2T and $\overline{\text{LF-1/2T}}$) are applied to the junctions of resistors R94 and R95 and resistors R92 and R93, respectively. Resistors R93 and R94 are the current-to-voltage load resistors which are returned to a 10 volt dc source developed across CR41. The signal voltage developed across these resistors (R93 and R94) is approximately 100 millivolts. These voltages are applied through oscillation suppressor resistors R92 and R95 to the bases of transistors Q25 and Q26, respectively. When LF-1/2T is high and $\overline{\text{LF-1/2T}}$ is low, Q25 is on and Q26 is off. The voltage at the junction of resistors R97 and R98, which are connected between -15 volts and ground, is slightly negative and near ground potential. This voltage, when applied through inverter U5E, becomes a logic 1 (5 volts dc). A reversal of the differential input signal causes Q25 to turn off and Q26 to turn on. Collector current for Q26 flowing through R96 and R97 causes the Q26 collector voltage to approach +3 volts. This voltage, applied through inverter U5E, produces a logic 0 (0 volts) at the output of U5E.

LF Offset Generator. The LF offset generator is operational amplifier U14 and its associated parts. The signal input is developed across R176 and then applied to the inverting input at pin 2. The output circuit, pin 6, has a quiescent level of zero volts established by the voltage divider consisting of R172 through R175 and connected between -15 volt and +15 volt sources. Voltages developed across R172 and R174 are fed back to the input through diode-connected Q54 and Q55 respectively to ensure the output does not exceed the input by more than ±2 volts. The FETs are used rather than conventional diodes because of their low leakage characteristics. Except under extreme signal conditions these FETs will not conduct. C24 provides feedback for frequency compensation. In addition, C25 is added to the feedback network when $\overline{\text{DEC 1}}$ is high and capacitors C26 and C28 are added to the feedback network when $\overline{\text{DEC 2}}$ is high.

When processing NRZ, DM, or RZ type PCM signals, the input signal to U14 is the algebraic sum of the currents applied through Q57 and Q59 and developed across R176. Current flow through Q57 is the +VD and it is gated on and off by the output signal from U12A. This output signal is affected by the type of PCM data being processed. In a similar manner, the current flow through Q59 is the -VD and it is gated by the output signal from U12F which is applied through amplifier Q60 to the base of Q59. The output signal from U12F also is affected by the type of PCM data being processed.

When processing NRZ type PCM signals, OFST is applied through inverter U20D to U20B and U19C. In U20B, OFST is ANDed with µL and the output, a negative pulse, is applied to U20A. The other input to U20A, from the RZ line receiver, is inhibited on the VAF027 card. Therefore, the output of U20A, +CHARGE, is the combined OFST and µL signals. This signal is applied to U12F and then through Q60 to Q59 to gate the -VD signal. The µL signal also goes through U20C which is enabled by CNRZ and then ANDed with OFST in U19C. The resultant output from U19C, a positive pulse, is applied through U19A and becomes -CHARGE which is applied through U12A. The positive pulse turns on Q57 and permits +VD current to flow through R176 for the duration of the pulse. As long as the transition in OFST occurs in the center of the bit time (zero offset), the +CHARGE and -CHARGE pulses generated at U20A and U19A are of equal width; therefore, -VD current and +VD current both flow through R176 for the same period of time and thus cause a zero volt input to the amplifier. If the offset is other than zero, the pulses are unequal in width. For a positive offset, the transition of OFST occurs sooner than normal and causes a more positive LF-OFST/V from the output of U14 which restores the offset to zero. For a negative offset, the transition of OFST occurs later than normal and causes a more negative LF-OFST/V from the output of U14 which again restores the offset to zero. During this time, the RZ input to pin 1 of U20A is held at a constant high and the RZ REF input to pin 3 of U19A is held at a constant low.

When processing RZ type PCM signals, OFST is held at a constant level and inhibits U20B and U19C. The RZ signal from the RZ line receiver is 1/2 bit period wide when offset is zero. This pulse at the output of U20A becomes +CHARGE. The RZ REF pulse, generated in the RZ offset safety circuit, is always 1/2 bit period wide. The RZ REF pulse is applied through U19A and becomes -CHARGE. Therefore, when there is zero offset in the RZ signal, +CHARGE and -CHARGE have equal widths and, as explained in the preceeding paragraph, result in a zero correction voltage from U14. When offset occurs in the RZ signal, the width of the RZ pulse changes and causes an unbalance between +CHARGE and -CHARGE which, in turn, causes an appropriate change in the correction voltage to counteract the offset.

When processing SØ type PCM signals, the circuits involved with the +CHARGE and -CHARGE pulses are held at constant levels. Instead, the SØ correction circuit, which is enabled by CSØ, provides positive and negative current pulses through Q50 and R176 to provide an average input to U14. As long as the offset in the SØ signal, obtained from

LF-NRZ, is zero, the positive and negative pulses are of equal duration and cause a zero correction voltage. When offset occurs, the pulses cause a correction voltage in the appropriate direction to restore the offset to zero.

LF AGC Generator. The LF AGC generator is operational amplifier U10 and its associated parts. The input signal is developed across R128 and then applied to the inverting input at pin 2. The other input to U10, at pin 3, is referenced to ground through R129. The output of U10, at pin 6, in LF-AGC/V which is developed across R102 and R101, is transferred to the LF/HF AGC select circuit. Voltages developed across R101 and R102 are fed back to the input through diode-connected Q27 and Q28 to limit the output signal voltage.

Capacitor C19 provides a feedback voltage for frequency compensation. Additional feedback capacitors are added to the circuit as the operating frequency range is progressively decreased from 10^3, 10^2 to 10^1. When $\overline{\text{DEC 1}}$ is low, the output of inverter U7E is high which causes a more positive voltage at the junction of CR17 and R120. This positive voltage, clamped at +0.7 volt by CR18, holds Q37 off which, in effect, opens the circuit to C18. When $\overline{\text{DEC 2}}$ is low, the output of U7F is high which causes a more positive voltage at the junction of CR15 and R114. This positive voltage, clamped at +0.7 volt by CR16, holds Q36 off which, in effect, opens the circuits to C17 and C27. When the operating frequency range decreases, $\overline{\text{DEC 1}}$ and/or $\overline{\text{DEC 2}}$, as appropriate, goes high and causes its associate transistor to go on. As an example, when Q37 turns on, C18 is connected into the feedback loop.

The input signal to U10 is obtained by gating +VD through Q32 by the 3/4T pulse obtained from U5C, and by gating -VD through Q33 by the 1/2T pulse obtained from U7A. Because of the emitter resistor values, twice the current flows through Q32 as flows through Q33; therefore, when the width relationship between 1/2T and 3/4T is 2-to-1, the voltage across R128 is equal to zero. Except for the amount of current flowing, both gating circuits operate in the same manner; therefore, only the 1/2T circuit is explained. During 1/2T time, the input to U7A is high and the output is low. This low holds Q34 off. The base of Q34 is clamped at +0.7 volt obtained from the junction of R124 and CR11. Because Q34 is off, the junction of CR10 and R126 goes low and turns Q33 on. The -VD current flows through Q33, R125 and R128 and thus provides a voltage across R128 (the input to the amplifier) that is proportional to the value of -VD and also to the width of the 1/2T pulse.

SØ Offset Correction Circuit. The enabling signal for the SØ offset correction circuit is CSØ which is applied through pin 9 and R171 to the base of emitter follower Q53. This high level is developed across R169 and applied through R168 to the emitter of Q52. The base of Q52 is grounded; therefore, the high level at its emitter

turns Q52 on and causes a high level at its collector. The resultant high level at the gate of Q50 permits Q50 to conduct in proportion to the amount of voltage developed across R164 and thus provides the input signal to the LF offset generator.

The SØ voltage from the output of the NRZ filter, LF-NRZ and $\overline{\text{LF-NRZ}}$, appears at the bases of Q44A and Q44B, both inputs to the differential amplifier. Circuit operation is such that when the positive excursions of LF-NRZ are equal to the negative excursions of LF-NRZ, the offset is zero which causes no current flow through R164 and thus no correction voltage to LF offset generator. For a positive offset, the positive excursions are reduced and the negative excursions are increased. This condition causes a positive voltage to be developed across R164 which, when applied to the LF offset generator, initiates a process to restore the offset to zero. For a negative offset, the negative excursions are reduced and the positive excursions are increased. This condition causes a negative voltage to be developed across R164 which, when applied to the LF offset generator, initiates a process to restore the offset to zero. The development of the positive and negative voltages are explained in the following paragraphs.

Transistor Q48 is held in conduction by the fixed bias (+0.7 volt) obtained from the junction of R165 and diode-connected transistor Q49. Current from -VD source flows through R170, Q48, R162 and diode-connected transistor Q43A to the +15 volt source. The resultant voltage at the base of Q43, which is directly proportional to -VD, controls the collector current through Q43B. This collector current is divided between Q44A and Q44B depending on the state of the LF-NRZ and $\overline{\text{LF-NRZ}}$ signals. When the positive and negative excursions of the LF-NRZ signal are equal, all the current flowing through Q44A flows through U11Q4 therefore, no current flows through R164. If the positive excursions are greater than the negative ones, Q44A will be held off for a greater length of time. Meanwhile, additional current flows through diode-connected transistor U11Q5, R150 and Q44B. This causes a positive voltage on the base of U11Q4 which increases the current flow through U11Q4. Since the current required by U11Q4 cannot be provided through Q44A, it must come through R164 and thus provides a negative correction voltage for the LF offset generator. A similar but opposite process occurs if the negative excursions are greater than the positive ones. In this case, the additional current required by Q44A cannot be supplied through U11Q4; instead, it is provided through R164 and thus provides a positive correction voltage for the LF offset generator. The junction of R160 and Zener diode CR23 provides -4.7 volts for proper operation of the circuit.

RZ Offset Safety Circuit. The RZ offset safety circuit includes an RZ REF generator and a divide-by-three circuit. The RZ REF generator includes a one-shot multivibrator composed of U19D and U13B, flip-flops U18A and U18B and gate U19B. The divide-by-three circuit includes flip-flops U17A and U17B, and gate U13D.

During normal operation, the output of U13D is high; therefore, it does not affect the operation of U18A. The RZ signal from the HF-RZ line receiver sets U18A each time there is a positive transition. One-half bit time later, a negative spike from U13B resets U18A. Thus, the $\overline{Q}$ Output of U18A (and the D input of U18B) is high from the start of the RZ positive-pulse until the spike is received from U13B. This spike is coincidental with the negative-going edge of the S-CLK; thus, it occurs in the middle of the bit period. The information at the D input of U18B is clocked into U18B by the positive-going transitions of S-CLK; thus, the output at Q is a waveshape that is low for the complete bit period in which a ONE was present. This output is applied to one input of gate U19B. The other input of U19B receives the S-CLK. When both of these signals are low, a high level RZ REF signal is generated for one-half a bit period.

When the S-CLK is applied through U12E and U12D to the input of U19D, the output would normally be the inversion of the input signal, but, because of R224 and C14, the output waveshape has increased fall time, which, in effect, lengthens the pulse width from U19D. Therefore, U13B is enabled on the positive-going edge of the clock pulse from U12D and remains enabled until the negative-going edge from R224 reaches approximately 2 volts. The resultant negative spike is applied to CLR input of U18A.

Flip-flops U17B and U17A are reset by the $\overline{Q}$ signal from U18A each time the RZ signal contains a ONE. Flip-flops U17B and U17A are arranged to count the 1/2T pulses which are applied to the clock input of U17B and occur each bit period. If the flip-flops are not reset for three consecutive bit periods, the Q outputs of both flip-flops are high and enable AND gate U13D. The low output of the AND gate sets flip-flop U18A to simulate the RZ input and thus produce an RZ REF pulse.

Overload and Offset Detectors. The overload and offset detectors contain the overload detector consisting of U11Q1, U11Q2, U11Q3, Q45, Q46, Q47 and associated parts, the dump generator consisting of U15A, U16A, U16B and associated parts, and logic elements U13C, U13A which combine the internally generated signals.

OVLD and $\overline{\text{OVLD}}$ are obtained from LF NRZ and $\overline{\text{LF NRZ}}$ which are applied through pins 7 and 8 and resistors R147 and R149 to the bases of U11Q2 and U11Q1, respectively. These transistors are connected as a differential amplifier and are sequentially turned on and off by the two input signals. The common emitter resistor R154 is connected through a current source transistor Q47 and its emitter resistor R158 to the -15 volt source. The differential signal developed across Q47 and R158 is applied to the base of Q46 which is one side of the differential amplifier composed of Q45 and Q46. Resistors R145 and R146 have equal resistance and are connected between the true and complement forms of the LF NRZ signal. The voltage at the

junction of these resistors, approximately 6.5 volts, is the average voltage of the two signals and remains constant even if the amplitude of the input signal increases. This reference voltage forward-biases U11Q3. Emitter current of U11Q3 causes a voltage drop across R151. This positive voltage from U11Q3 emitter is applied through R152 to the base of Q45. When the input signals have normal amplitudes, approximately 1 volt p-p, the base voltage of Q46 is approximately 5 volts. Since the base voltage of Q45 is more positive than the base voltage of Q46, Q46 is turned on. Thus, the collector voltage of Q45, the OVLD signal, is a negative voltage (a low level) and the collector voltage of Q46, the $\overline{\text{OVLD}}$ signal, is a positive voltage (a high level). When the amplitudes of the input signals increase, the currents through U11Q1 and U11Q2 increase and cause a larger voltage drop across Q47 and R158. If the amplitude of the input signals increases to the point of overload, the increasing voltage drop across Q47 and R158 causes the base voltage of Q46 to exceed the reference voltage on the base of Q45; therefore, Q46 turns off and causes Q45 to turn on. This condition causes OVLD to go high and $\overline{\text{OVLD}}$ to go low.

When the bit synchronizer is processing bit rates of 10^4 bps and higher, DEC 4 is a high level and allows U15A to be reset by the ground connected to its CLR input. The low level from the Q output resets U16A which provides a high DUMP level from the $\overline{Q}$ output and a low $\overline{\text{DUMP}}$ level from the Q output. The low level from the Q output holds U16B set and thus provides a high level at the Q output. The flip-flops remain in this condition until the bit rate range is changed to a value of 10^3 bps or lower, which causes DEC 4 to go low. Because low levels are applied to both the PR and CLR inputs of U15A, the Q and $\overline{Q}$ outputs are both high levels and thus, the Q output no longer holds U16A reset. On the next positive transition of S-CLK, after the bit rate change, the high level at the Q output of U16B is clocked into U16A to provide a high Q output ($\overline{\text{DUMP}}$) and a low $\overline{Q}$ output (DUMP). The circuit remains in this condition until a spill condition is initiated. When a spill condition is initiated, SPILL changes to a high level and resets U16B. On the next positive transition of S-CLK, the low level at the Q output of U16B resets U16A and provides a high level DUMP at the $\overline{Q}$ output of U16A. The low output from Q of U16A sets U16B. One bit time later, S-CLK clocks the high level from Q of U16B into U16A and causes its outputs to revert back to a high at the Q output and a low at the $\overline{Q}$ output. Therefore, in summation, when SPILL is received, DUMP goes high for one clock period and then the circuit is returned to its initial condition in preparation for another SPILL signal.

OVLD and ACQ are ANDed in U13C and then ORed with $\overline{\text{DUMP}}$ to provide ACQ-OVLD+DUMP which is applied through CR34 to the emitter of Q61. The base of Q61 is held at approximately 1.5 volts obtained from the junction of R195 and R197. Therefore, when the output of U13A goes high, Q61 is turned on and causes a high level to be applied from the collector through CR35 to the gate of Q64. Q64 turns on and places a low impedance across the LF offset generator which causes the output of the LF offset generator to go to zero. The DUMP signal is

applied to a circuit that is identical to that described above except FET Q38 is connected across the LF AGC generator.

Acquisition Switch. The acquisition switch includes flip-flop U15B, logic gates U6A, U6B and U6D and inverter U5D. Under normal conditions, U15B is continuously being set by the negative transitions of 3/4T. During this time, $\overline{ACQ}$ is high and is ANDed with 3/4T in AND gate U6D. The output is applied through NOR gate U6B to become the relatively narrow-window μL pulse. When a spill conditon exists, SPILL resets U15B. High ACQ from the $\overline{Q}$ output of U15B is ANDed with 1/2T in AND gate U6A. The output is applied through NOR gate U6B to become the relatively wide-window μL pulse.

4.8.3 Signal Level Control Type SLC030

The type SLC030 card (see schematic drawing 460-0927) contains circuits included in the high frequency AGC and control section (see figure 4-7); and contains five line receivers for the incoming signals (HF 1/2T, HF 3/4T, OF OFST, HF RZ, and P-CLK), voltage-to-current converter, acquisition switch, HF AGC generator, HF offset generator, SØ correction circuit and dump and overload detectors. Each of these circuits is explained in the following paragraphs.

HF 1/2T Line Receiver. The HF 1/2T line receiver consists of a differential pair including transistors Q7 and Q8, an emitter follower stage Q59, Zener diode CR2 and associated parts. The HF 1/2T pulses, in their true (pin 35) and complement (pin 34) forms, are received from the high frequency threshold detector section and are applied through oscillation suppression resistors R13 and R16 to the bases of Q7 and Q8, respectively. Common emitter resistor R14 sets the collector current through both transistors. A fixed bias source of approximately 9.9 volts is provided by Zener diode CR2 and is applied through R12 and R15 to the base circuit of each transistor. The output signal from Q7 ($\overline{1/2T}$) is developed across collector load resistor R45 and the output signal from Q8 (1/2T) is applied to the ACQ switch. The $\overline{1/2T}$ is buffered in Q59 and applied, as $\overline{1/2T}$ to RZ offset safety circuit. R10 and R178 are the emitter resistors for Q59 and R11 is the collector resistor.

HF 3/4T Line Receiver. The HF 3/4T line receiver consists of a differential pair including transistors Q5 and Q6, an emitter follower stage Q4 and associated parts. Zener diode CR2, part of the HF 1/2T line receiver, also provides a fixed bias source of approximately 9.9 volts for transistors Q5 and Q6. The HF 3/4T pulses, in their true (pin 33) and complement (pin 32) forms, are received from the high frequency threshold detector section (see figure 4-6) and are applied through oscillation suppression resistors R20 and R23 to the bases of Q5 and Q6 respectively. The output signal from Q5 ($\overline{3/4T}$) is developed across collector load resistor R27 and the output signal from Q6 (3/4T) is applied to the ACQ switch. The $\overline{3/4T}$ pulse is buffered in

Q4. The $\overline{3/4T}$ pulse, developed across R77, is applied to two consecutive inverters, U13B and U13C, and then applied as $\overline{HF\text{-}XNG}$ (with TTL levels of 0 and 5 volts) to the spill detector and transition loss delay generator section (see figure 4-12). This signal also is applied to the dump and overload detectors.

HF OFST Line Receiver. The HF OFST line receiver consists of a differential pair including transistors Q29 and Q30, Zener diode CR9 and associated parts. The HF OFST pulses, in their true (pin 9) and complement (pin 10) forms, are received from the high frequency threshold detector section (see figure 4-6) and applied through oscillation suppression resistors R82 and R79 to the bases of Q29 and Q30, respectively. Common emitter resistor R81 sets the collector current through both transistors. A fixed source of approximately 9.9 volts bias is provided by Zener diode CR9 and applied through R78 and R80 to the base circuit of each transistor. The output signal from Q29 (OFST) is developed across collector load resistor R83, and the output signal from Q30 (OFST) is developed across collector load resistor R84. Both output signals are routed to the HF offset generator.

HF RZ Line Receiver. The HF RZ line receiver consists of a differential pair including transistors Q27 and Q28, a level converter Q31 and associated parts. The HF RZ pulses, in their true (pin 8) and complement (pin 7) forms, are received from the high frequency threshold detector section (see figure 4-6) and are applied through oscillation suppression resistors R69 and R70 to the bases of Q27 and Q28, respectively. The output signal (RZ) from the collector of Q27 is applied through R175 to the HF offset generator. The output signal ($\overline{RZ}$) from the collector of Q28, which is developed across collector load resistor R74, is applied to the base of Q31. Diode CR25 shunts to ground any voltage that is more negative than -0.7 volt and thus prevents the transistor from going too far into cutoff. The signal is inverted within the transistor and developed across collector load resistor R75. The output signal has TTL levels of 0 and +5 volts and is applied to the RZ offset safety circuit.

P-CLK Line Receiver. The P-CLK line receiver consists of a differential pair including transistors Q56 and Q57, inverter U13D and associated parts. The P-CLK pulses, in their true (pin 31) and complement (pin 30) forms, are received from the phase lock loop section (see figure 4-13) and are applied through oscillation suppression resistors R166 and R167 to the bases of Q56 and Q57, respectively. The output signal ($\overline{P\text{-}CLK}$) from the collector of Q56, which is developed across collector load resistor R171, is applied to inverter U13D. Resistor R172 forms a voltage divider with R171 to reduce the collector voltage of Q56. The output of U13D (S-CLK) is applied through pin 21 to the low frequency AGC and offset control section (see figure 4-11). The same signal is also applied to the dump and overload detectors and the RZ safety circuit. Resistor R176 is an isolation resistor through which the S-CLK signal is applied to test point 2.

Voltage-to-Current Converter. The voltage-to-current converter consists of a differential amplifier (U1) and buffers (Q1 through Q3) which provide current in proportion to the amplitude of the VD1 signal received from the DAC secton (see figure 4-20). The voltage-to-current converter also contains current regulators to provide the +IDA and -2IDA currents for the HF AGC generator, the +2IDO and -2IDO current for the SØ correction circuit (see figure 4-7). Details of the voltage-to-current converter are explained in the following paragraphs.

The VD1 signal, a voltage level between 0.5 and 5 volts, is applied through the differential amplifier and developed across R4 to become VDX. Signal VDX is then applied through R7 and Q3 to become IDO, which is developed across the collector load (R123 and diode-connected transistor U8Q5) of transistor Q3. Signal VDX also is applied through R5 and Q1 to become IDA which is developed across the collector load (R50 and diode-connected transistor U2Q5) of transistor Q1. Diode-connected transistor Q2 and R8 are connected as a voltage divider to provide a bias of -0.7 volt on the bases of Q1 and Q3. Resistor R1 limits the input current of U1. Resistors R2 and R3 form a voltage divider that provides a feedback voltage for stabilization of the amplifier. Capacitors C1 and C2 eliminate any high speed transients on the power supply leads from affecting the operation of U1.

Before explaining how the +IDA, -2IDA, +2IDO, and -IDO currents are obtained to charge the tracking capacitors in the HF AGC generator and in the HF offset generator, the derivation of the names is first explained. The charging path for the capacitors is from a positive voltage source or a negative voltage source; thus, the currents obtained from a positive source are prefixed with a + sign and those obtained from a negative source are prefixed with a - signal. The current names which contain an O are associated with the offset generator while those containing an A are associated with the AGC generator. The names containing a 2 have a value of current that is twice that of those that do not contain a 2.

The -2IDA current for HF AGC generator is obtained when the IDA signal is applied to the bases of the parallel-connected transistors U2Q1 and U2Q2. The -2IDA current is provided from the -15 volt source through R53, the emitter-collector circuit of the parallel-connected transistors and R51 to the -2IDA switch Q22 in the HF AGC generator.

The +IDA current for the HF AGC generator is obtained when the IDA signal is applied to the base of U2Q3. This causes a current to flow through resistor R52, emitter-collector circuit of Q23, resistor R41 and diode-connected transistor Q16A to the +15 volt source. The signal developed across R41 and the diode-connected transistor Q16A biases Q16B which provides the +IDA current from the +15 volts source through R36, Q16B and R40 to the +IDA switch Q18 in the HF AGC generator.

The -IDO current for the SØ correction circuit is obtained when the IDA signal is applied to the base of U2Q4. The collector-emitter circuit of U2Q4 provides the -IDO signal to the SØ correction circuit where switch Q48B is turned on and allows Q52 to provide a bipolar current (±1) to the HF offset generator in response to the HF NRZ signal.

The +2IDO current for the HF offset circuit is obtained when the IDO signal is applied to the bases of the parallel-connected transistors U8Q1 and U8Q2. These transistors are forward biased which allows current to flow from -15 volt source through the parallel-connected transistors U8Q1 and U8Q2, R162, parallel-connected transistors U11Q1 and U11Q2, R160, Q50A and R153 to the +15 volt source. Transistor Q51 and its emitter resistor R155 provide the proper base voltages for Q50A and Q50B. Because transistors Q50A and Q50B are a matched pair and they are connected as shown in schematic drawing 460-0927, the +2IDO current flowing through Q50A is the same value as the current flowing through Q50B. The path for the +2IDO current is from +15 volt source through CR22, R154, Q50B and R91 to the +2IDO switch Q39 in the HF offset generator.

The -2IDO current for the HF offset circuit is obtained when the IDO signal is applied to the bases of parallel-connected transistors U8Q3 and U8Q4. The -2IDO current is provided from the -15 volt source through R125, the parallel-connected transistors U8Q3 and U8Q4 and R98 to the -2IDO switch Q37 in the HF offset generator.

Acquisition Switch. The acquisition switch consists of two inverters, U3E and U3F, the 1/2T gate composed of transistors Q12 and Q13 and the 3/4T gate composed of transistors Q14 and Q15. The circuit uses ACQ·NRZ and $\overline{\text{ACQ}}$·NRZ to gate the 1/2T or the 3/4T signal to form the µH pulse. When ACQ·NRZ is a high level, the output of inverter U3E is a low level. Current flowing through diode CR5 and R32 holds the junction of resistors R29 and R33 at approximately 4.3 volts. At this time, CR5 is reverse biased. The 4.3 volts applied through R33, a suppression resistor, turn Q12 on and Q13 off. Q12 provides the 1/2T pulse as the µH pulse. Meanwhile, the $\overline{\text{ACQ}}$·NRZ is a low level and when applied to inverter U3F, causes the output of the inverter to go high. The high output of the inverter causes current from the inverter to flow through R30. As the voltage at the junction of R28 and R31 starts to go positive towards 15 volts, it is clamped at 5.7 volts by diode CR3. Diode CR4 is reversed biased. The high level applied through R31 to Q14 holds Q14 off and holds Q15 on. Transistor Q15 provides an alternate path to ground for the 3/4T pulse. When the levels of the ACQ.NRZ and $\overline{\text{ACQ}}$.NRZ are reversed, a similar, but opposite, condition to that just described occurs. The result is that Q14 is turned on and provides the 3/4T pulse to form the µH pulse and Q13 is turned on to provide an alternate path to ground for the 1/2T pulse.

HF AGC Generator. The HF AGC generator contains operational amplifier U4, the capacitor switching circuit including capacitors C4, C5 and C6, transistors Q24, Q25 and Q26 and associated parts, the 3/4T switching transistors Q9, Q10, Q21 and Q22, and the 1/2T switching transistors Q17 through Q20. The 1/2T and 3/4T pulses from their respective line receivers gate the -IDA and the -2IDA currents, respectively, from the voltage-to-current converter into the input circuit of operational amplifier U4. Selectable capacitors C5 and C6, which are used in conjunction with C4, also are connected to the input circuit of the operational amplifier. The total capacitance of these capacitors with resistors R67 and R68 form two RC networks which are charged and discharged by two gated current pulses. The net result is an average voltage value in response to the width relationship of the 1/2T and the 3/4T pulses and the value of VD1. The output of the operational amplifier is HF-AGC/V. Details of this circuit are explained in the following paragraphs.

The portion of the HF AGC generator that provides the positive charging path for capacitors C4, C5 and C6, as applicable, during 1/2T pulse time includes transistors Q17 through Q20 and associated parts. The 1/2T pulse from the HF 1/2T line receiver is developed across load resistor R45 and reverse biases Q20. Because Q19 and Q20 are connected as a differential amplifier, Q19 is turned on, causing its collector to become less positive. This voltage causes Q18 to be turned on. When Q18 is turned on, the charging current (+IDA) flows through R67, Q18 and R40. The capacitors tend to charge exponentially towards +15 volts; however, the negative current (-2IDO), explained in the following paragraph, opposes the positive charging current.

The fixed bias for the base of Q20 is established by the voltage divider R45 and R46 connected between ground and -15 volts. Resistor R44 is a suppression resistor to prevent oscillations. A fixed bias of 0.7 volt, for the base of Q19, is obtained from the network consisting of R42 and diode CR8. The common emitter resistor, R43, sets the collector currents through the differential amplifier. When the 1/2T pulse is not present, Q20 is on and pulls the base of Q17 to a less positive value which turns Q17 on. Because at this time Q18 is off, Q17 provides a load for the +IDA current and thus prevents changing current demands from the power supply. R38 and R39 are the collector load resistors for Q20 and Q19, respectively. The network consisting of R37 and Zener diode CR7 provides 5.1 volts for the collector source voltages of Q19 and Q20.

The portion of the HF AGC generator that provides the negative charging path for capacitors C4, C5 and C6, as applicable, during 3/4T pulse time includes transistors Q9, Q10, Q21 and Q22 and associated parts. The 3/4 T pulse from the HF 3/4T line receiver is developed across load resistor R27 and forward biases Q10. Because Q9 and Q10 are connected as a differential amplifier, Q9 is turned off. Because Q10 is on, the base voltage of Q22 becomes less negative and causes Q22 to be turned on. When Q22 is turned on, the charging current

(-2IDA) flows through R51, Q22 and R68. The capacitors charge exponentially towards -15 volts; however, the positive current (+IDA), explained in the preceding paragraph, opposes the negative charging current. The capacitors then are charged to a value that represents the difference between the two exponential voltages that would be developed individually across the capacitors.

The fixed bias for the base of Q10 is established by the voltage divider R26 and R27 connected between ground and -15 volts. Resistor R25 is a suppression resistor to prevent oscillations. A fixed bias of 0.7 volt, for the base of Q9, is obtained from the network consisting of R17 and diode CR1. The common emitter resistor, R24, sets the collector currents through the differential amplifier. When the 3/4T pulse is not present, Q9 is on and pulls the base of Q21 to a less negative value which turns Q21 on. Because at this time Q22 is off, Q21 provides a load for the -2IDA current and thus prevents changing current demands from the power supply. R47 and R48 are the collector load resistors for Q9 and Q10, respectively. The network R49 and Zener diode CR10 provides -6.8 volts for the collector source voltages of Q9 and Q10. Transistor Q11, whose collector-emitter circuit is connected in parallel with Q10, normally is held off by $\overline{\text{OVLD}}$. When an overload condition occurs, Q10 is turned on and overrides the 3/4T pulses such that -2IDA current is continuously applied to the capacitors until the overload condition is normalized.

The capacitors in the input circuit of the differential amplifier are selected by the DEC 1 and the DEC 2 control signals obtained from the program decoding section (see figure 4-26). When bit rate has a multiplier of 10^4, DEC 1 and DEC 2 are both low levels. The low level applied to inverter U3B produces a high level at the output. This high applied through CR12 to the base of Q25, turns Q25 on and, in effect, connects the low side of capacitor C5 to ground. The network consisting of R60, R61 and CR12 establishes the proper biases for U3B and Q25. Resistor R59 provides a high impedance return for the capacitor when the equipment is deenergized. Zener diode CR12 develops 4.7 volts across its terminals. The low levels applied to U3A and U3D produce a high level at the common output. The outputs of these inverters are ORed together such that if either input is high, the common output is low. The high level at the common output of the inverters is applied through CR13 to the base of Q26 and turns Q26 on. Emitter-collector current flowing through Q26, in effect, connects the low side of capacitor C6 to ground. The remaining parts of this circuit perform the same functions that were described for their counterparts in the circuit previously described. In a manner similar to that just described, the DEC 1 and DEC 2 signals select neither capacitor, select C5 and C6, or select C5, as indicated in table 4-6.

Table 4-6. Capacitor Selection

BIT RANGE	DEC 1	DEC 2	CAPACITORS SELECTED
10^4	0	0	C5 and C6
10^5	1	0	C5
10^6	0	1	Neither

Transistor Q24, inverter U3C and associated parts provide a means of discharging capacitors C4, C5 and C6 when the DUMP signal is obtained from the dump and overload detectors. When signal DUMP, a low level, is applied to inverter U3C, the output of the inverter is a high level which is applied through R57 to the base of Q24 and turns Q24 on. Therefore, any charge on the capacitors is then dissipated through R55 and the emitter-collector circuit of Q24. The network composed of R56, R57 and R58 which is connected between -15 volts and +15 volts provides the proper biases for the output circuit of the inverter and the base of Q24. Diode CR11 clamps the input to differential amplifier (voltage across capacitors C4, C5, and C6, as applicable) to -0.7 volt.

HF Offset Generator. The HF offset generator contains operational amplifier U10, the capacitor switching circuit including capacitors C17, C18 and C19, transistors Q40 through Q43 and associated parts, the -2IDO switching transistors Q36 and Q37, the +2IDO switching transistors Q38 and Q39 and the combining transistors Q32 and Q33. Details of the circuit are explained in the following paragraphs.

The combining transistors which receive the μH pulse and the true and complement forms of the HF OFST signal gate the +2IDO and -2IDO currents from the voltage-to-current converter into the input circuit of the operational amplifier U10. Selectable capacitors C17 and C19, which are used in conjunction with C18, also are connected to the input circuit of the operational amplifier U10. The total capacitance of these capacitors and resistors R92 and R96 form two RC networks which are charged and discharged by the two gated current pulses. The net result is an average voltage value in response to the time relationship between the center of the μH pulse and the transition time of the HF OFST signal. The output of the operational amplifier is HF OFST/V which is fed back to the variable gain and offset amplifier to normalize the offset. When offset is normalized, the transition time of the HF OFST signal occurs in the middle of the μH pulses.

When the µH pulse is absent, transistors Q32 and Q33 are cut off; therefore, Q37 is held off by the -7.5 volts developed across Zener diode CR15. Because Q37 is off, Q36 turns on and conducts the -2IDO current to ground. Also, because µH pulse is absent, Q34 is off and the other half of the differential amplifier, Q35, is on. The voltage drop across R90 lowers the positive voltage on the base of Q38 and turns Q38 on to conduct the -2IDO current to ground. When the µH pulse is present the HF OFST signal is low, Q30 is turned on and at the same time the $\overline{\text{HF OFST}}$, a high level, turns Q29 off. The resultant signals developed across R83 and R84 are applied to the bases Q32 and Q33, respectively. The low signal from Q29 is applied to Q32 and turns Q32 on and the high signal from Q30 is applied to Q33 and turns Q33 off. The high signal from Q32, developed across R97, causes Q37 to be turned on. When Q37 is turned on, the -2IDO current charges the selectable capacitors until the transition of the HF OFST signal occurs. When the transition occurs, the transistors that were previously on are turned off and the transistors that were previously off are turned on, consequently, Q39 which was previously off is now turned on and conducts the -2IDO current into the selectable capacitors. Thus, when no offset correction is required, the HF OFST signal transition occurs at the midpoint of the µH pulse. The +2IDO and -2IDO currents flow for an equal period of time; otherwise, one current flows for a longer length of time than the other.

Capacitors C17 and C19 are selected by DEC 1 and DEC 2 signals in the same manner as are capacitors C5 and C6, explained previously, in the HF AGC generator section. During a dump condition or during an overload condition, after acquisition time, DUMP+ OVLD·ACQ from the dump and overload detectors is high and is applied to inverters U9F and U9B. The low output from U9F turns on Q40 which discharges the tracking capacitors in the HF offset generator. Resistors R101, R102 and R103 and diodes CR16 and CR17 provide the proper biasing for U9F and Q40. The high level applied to U9B is again inverted by U9A to provide a high level to the base of Q41. Transistor Q41 is turned on and assists Q40 in discharging the tracking capacitors. Resistors R104 through R107 provide the proper biasing for U9B, U9A and Q41.

SØ Correction Circuit. The enabling signal for the SØ correction circuit is CSØ which is applied through pin 16 and R126 to the base of emitter follower Q47. This high level signal is developed across emitter resistor R128 and applied through R127 to the base of U11Q3. The voltage at the base of U11Q3 is limited to +0.7 by CR23. CR21 limits the base voltage to -0.7 when CSØ is low and thus prevents U11Q3 from going too far into cutoff. The high CSØ turns U11Q3 on and allows -IDO current from the voltage-to-current conversion circuit to flow through U11Q3, R157, R130 and the diode-connected transistor Q48A to the +15 volt source. The low level signal developed across R130 is applied to the base of Q48B and turns on Q48B. When Q48B is on, current can flow through Q52A or Q52B, depending on the state of the HF NRZ and $\overline{\text{HF NRZ}}$ signals. These two signals are developed across resistors R131 through R135 and applied to the bases of Q52A

and B. When HF NRZ is high (and $\overline{\text{HF NRZ}}$ is low), Q52A is on and Q52B is off. Positive current (+I) flows from operational amplifier U10 through R136, transistor Q52A and Q48B, and R129 to the +15 volts source. Because Q52B is off, a low level is obtained through R142 and diode-connected transistor U12Q5 which is connected to a voltage source of -5.1 volts. This source is obtained from the junction of R147 and Zener diode CR24. The low level from R142 holds U12Q4 off. After the transition of the HF NRZ signal, HF NRZ is low (and $\overline{\text{HF NRZ}}$ is high) which causes Q52A to be turned off and Q52B to be turned on. Because Q52B is on, the high level developed at its collector turns on U12Q4. Negative current (-I) then flows through U12Q4 and R136 to the input circuit of operational amplifier U10.

RZ Offset Safety Circuit. The RZ offset safety circuit includes an RZ REF generator and a divide-by-three circuit. The RZ REF generator contains switch Q44, an AND gate composed of Q45 and Q46, a one-shot multivibrator composed of U7B and U7C and two flip-flops U6A and U6B. The divide-by-three circuit includes inverter U13A, two flip-flops U5A and U5B and AND gate U7D. Details of the circuit are explained in the following paragraphs.

During normal conditions, the output of U7D is high; therefore, it does not affect the operation of U6A. The RZ signal from the HF RZ line receiver sets U6A each time there is a positive transition. One-half bit time later, a negative spike from U7C resets the flip-flop. Thus, the $\overline{Q}$ output of U6A (and the D input of U6B) is high from the start of the RZ positive pulse until the spike is received from U7C. This spike is coincidental with the negative-going edge of the S-CLK; thus, it occurs in the middle of the bit period. The information at the D input of U6B is clocked into U6B by the positive-going transitions of S-CLK; thus, the output at $\overline{Q}$ is a waveshape that is high for the complete bit period in which a ONE was present. This output is applied to one input of an AND gate (base of Q46). The other input of the AND gate (base of Q45) receives the S-CLK. When both of these signals are high, both transistors are cut off. Transistor Q44 is therefore allowed to turn on during the positive half cycle of the S-CLK to complete the path for the RZ REF signal which turns on Q37 for one-half a bit period. As was explained earlier, Q37 in the high frequency offset generator circuit provides the -2IDO current to the operation amplifier. Resistors R118 and R119 provide the proper base bias for Q44. Resistors R121 and R122 are suppression resistors to prevent oscillation.

When the S-CLK is applied to the input of U7B, the output would normally be the inversion of the input signal, but, because of R76 and C3, the output waveshape has increased fall time which, in effect, lengthens the pulse width from U7B. Therefore, U7C is enabled on the positive-going edge of the clock pulse from U15-11 and remains enabled until the negative-going edge from R76 reaches approximately 2 volts. The resultant negative spike is applied to CLR input of U6A.

Flip-flops U5A and U5B are reset by the $\overline{Q}$ signal from U6A each time the RZ signal contains a ONE. Flip-flops Q5A and Q5B are arranged to count the 1/2T pulses which are applied through i verter U13A and occur each bit period. If the flip-flops are not reset for three consecutive bit periods, the Q outputs of both fl p-flops are high and enable AND gate U7D. The low output of the A D gate sets flip-flop U6A to simulate an RZ input and thus produce an RZ REF pulse.

Overload and Offset Detectors. The overload and offset detectors contain the overload detector consisting of U12Q1, U12Q2, U12Q3, Q53, Q54, Q55 and associated parts, the dump generator consisting of U14B, U15A, U15B and associated parts, an acquisition flip-flop U14A, and logic elements U16A, U16C, U16D, U7A, U13E and U13F. The logic elements combine the internally generated signals with SPILL and CNRZ to produce DUMP, $\overline{\text{OVLD}}$, ACQ NRZ, $\overline{\text{ACQ}}$ NRZ and DUMP + OVLD·ACQ. Details of this circuit are explained in the following paragraphs.

OVLD and $\overline{\text{OVLD}}$ are obtained from HF NRZ and $\overline{\text{HF NRZ}}$ which are applied through pins 6 and 5 and resistors R139 and R141 to the bases of U12Q2 and U12Q1, respectively. These transistors are connected as a differential amplifier and are sequentially turned on and off by the two input signals. The common emitter resistor R146 is connected through a current source transistor Q55 and its emitter resistor R152 to the -15 volt source. The differential signal developed across Q55 and R152 is applied to the base of Q54 which is one side of the differential amplifier composed of Q53 and Q54. Resistors R137 and R138 have equal resistance and are connected between the true and complement forms of the HF NRZ signal. The voltage at the junction of these resistors, approximately 6.5 volts, is the average voltage of the two signals and remains constant even if the amplitude of the input signal increases. This reference voltage forward biases U12Q3. Emitter current of U12Q3 causes a voltage drop across R143. This positive voltage from U12Q3 emitter is applied through R144 to the base of Q53. When the input signals have normal amplitudes, approximately 1 volt p-p, the base voltage of Q54 is approximately 5 volts. Since the base voltage of Q53 is more positive than the base voltage of Q54, Q54 is turned on and Q53 is turned off. Thus, the collector voltage of Q53, the OVLD signal, is a negative voltage (a low level) and the collector voltage of Q54, the $\overline{\text{OVLD}}$ signal, is a positive voltage (a high level).

When the amplitudes of the input signals increase, the currents through U12Q1 and U12Q2 increase and cause a larger voltage drop across Q55 and R152. If the amplitude of the input signals increases to the point of overload, the increasing voltage drop across Q55 and R152 causes the base voltage of Q54 to exceed the reference voltage on the base of Q53; therefore, Q54 turns off and causes Q53 to turn on. This condition causes OVLD to go high and $\overline{\text{OVLD}}$ to go low.

When the bit synchronizer is processing bit rates of 10^3 bps and lower, DEC 4 is a low level and holds U15B set and consequently holds $\overline{DUMP}$ at a low level. When processing bit rates of 10^4 bps and higher, DEC 4 is a high level and therefore, does not inhibit the operation of dump flip-flops U14B, U15A and U15B.

When a spill condition is initiated, SPILL changes to a high level and resets U14B. On the next positive transition of S-CLK, the high level at the $\overline{Q}$ output of U14B sets U15A and provides a high level at the Q output of U15A. One bit time later, S-CLK sets U15B. The resultant low level at the $\overline{Q}$ output of U15B presets U14B in preparation for the next spill condition and also provides a low level $\overline{DUMP}$ signal to indicate a dump condition. This signal is applied to the HF AGC generator and to the combining gates (U16A).

The acquisition flip-flop U14A is cleared each time $\overline{HF\text{-}XNG}$ is low and is clocked by SPILL when a spill condition is initiated. The flip-flop remains set and provides a high level ACQ signal at its Q output until $\overline{HF\text{-}XNG}$ again goes low, indicating that signal transitions are being received. The ACQ signal is ANDed with CNRZ and U16C, then inverted by U13F. The resultant signal, $\overline{ACQ}\cdot NRZ$ is applied to the acquisition switch. The $\overline{ACQ}$ signal from $\overline{Q}$ output of U14A also is ANDed with CNRZ in U16D and then inverted by U13E. This resultant signal $\overline{ACQ}\cdot NRZ$ also is applied to the acquisition switch. ACQ from the Q output of U14A and OVLD from the collector of Q53 are ANDed in U7A to produce $\overline{OVLD.ACQ}$. This signal is then ORed with $\overline{DUMP}$ in U16A to provide DUMP + OVLD·ACQ which is applied to the HF offset generator.

Resistor R173 provides isolation and a positive voltage (from the +5 volt source) to those inputs of the flip-flops that must be held high. These inputs include CLR of U14B, U15A and U15B, PR of U14A and U15A and D of U14A. The ACQ signal is applied through R177 to test point 1 and the OVLD.ACQ signal is applied through R179 to test point 3.

4.8.4 HF Matched Filter Type VAF026

The type VAF026 card (see schematic drawing 460-0903) contains the circuits of the high frequency tracking filter section (see figure 4-5). These circuits include the line receiver, buffer amplifier, filter sections, feedback and bypass capacitor banks, Raysistor control circuit, Raysistor drivers, HF-NRZ-MF summing amplifier and HF-SØ-MF summing amplifier. Each of these circuits is explained in the following paragraphs.

Line Receiver. The line receiver converts the true and complement forms of the HF INPUT signal to a single-ended signal that is applied to the buffer. The input signals control the amount of current flowing through transistors Q1 and Q2. The current flowing through Q1 also flows through the input leg of a current mirror circuit which includes U10Q4 and R4. Resistor R5 is connected to a voltage source of -7.5.

volts obtained from the junction of R9 and Zener diode CR13. Because the voltage drop across R4 plus the diode drop of the base-emitter junction of U10Q4 is equal to the voltage drop across R5 plus the diode drop of diode-connected transistor U10Q5 and also because the resistors and transistor junctions in each leg are matched, the current in the output leg of the current mirror circuit is equal to the current in the input leg. Transistor U10Q3 and diode-connected transistor U10Q2 divert excess current from the output leg into load resistor R3. Thus, when the current of the HF INPUT is relatively high and the current of the HF INPUT is relatively low, the excess current flowing in the output leg flows into R3 and causes a negative voltage (approximately -1 volt) to be developed across R3. When the polarity of the input signal changes, the current of the HF INPUT is relatively low and the current of HF INPUT is relatively high. The output leg supplies only a portion of the current required by Q2; the remainder is supplied through R3 and causes a positive voltage (approximately +1 volt) to be developed across R3. The series circuit consisting of R1 and R2 provides approximately +6 volts for the fixed base bias of Q1 and Q2. This circuit is bypassed by capacitor C1.

Buffer. The buffer receives the signal developed across R3 and applied through R125. This signal is applied to the base of Q5 which serves as both an amplifier and an emitter-follower. The signal from the collector, developed across R10, is applied to the base of Q4. The collector output of Q4 is developed across R126. Meanwhile, the signal developed across R13 limits, via diode-connected transistor Q6, the Q4 collector voltage to a value of +0.7 volt above the Q5 emitter voltage. Because the Q5 emitter voltage is +0.7 volt below the Q5 base voltage, the voltage excursions at the Q4 collector are the same value as the voltage excursions at the Q5 base. Therefore, the voltage at the Q4 collector (and test point 1) is ±1 volt. This signal is applied to the Q filter. Capacitors C2, C3, C5 and C6, together with R11 and R14, form two decoupling networks to prevent signal currents from entering the power supply leads. Capacitor C4 provides high frequency compensation.

Filter Sections. There are four filter sections identified as Q, R, S, and T that sequentially affect the HF INPUT signal. The output of each filter is selectively routed to two summing amplifiers. The values of selected parts in each filter are changed as the input signal frequency is changed to ensure the bandpass characteristics remain constant over the operating frequency range of 1.000×10^4 to 5.000×10^6 bps. This tracking capability is implemented by selecting, for each frequency range, 10^4, 10^5 and 10^6 bps, the input bypass capacitors in the R and T filters, the feedback capacitors from the R filter to the Q filter and the feedback capacitors from the T filter to the S filter. Tracking also is implemented by automatically adjusting the series input resistance of each filter in accordance with the operating frequency within each frequency range. A different set of capacitors is selected for each function when the operating frequency range is within 10^4, 10^5 and 10^6 bps. The method of selection is described later, in the paragraph headed Feedback and Bypass Capacitors

Bank and Control. The series variable resistance is part of a Raysistor that changes its resistance value in inverse proportion to the operating frequency within each decade frequency range. Operation and control of the Raysistor is described later, in the paragraph titled Raysistor Control Circuit. Details of each filter are explained in the following paragraphs.

The Q filter includes the resistive element connected to pins 3 and 4 of Raysistor Z1, input transistor Q7, output transistor Q9 and diode-connected transistor Q8. The input signal from the buffer is applied through the Raysistor element and R132 to the base of Q7. A feedback voltage from the output of the R filter also is applied through the selectable capacitor bank and R132 to the base of Q7. These two signals are amplified in Q7 and appear across the collector load resistor R18. The signal is applied to the base of Q9 when it is again amplified and developed across R129. Diode-connected transistor Q8 limits the output waveform excursions to 0.7 volt below the Q7 emitter signal swing. The collector voltage of Q9, which is the output of the Q filter, has amplitudes of ±0.9 volt about ground. Decoupling networks composed of R16, C7, and C8 for the +15 volt source and R20, C10, and C11 for the -15 volt source prevent signal currents from entering the power supply leads. Capacitor C9 is included for high frequency compensation.

The R filter, except for the input bypass capacitors, is identical to the buffer explained previously. Capacitor C33 provides high frequency compensation for the R filter when the operating frequency range is within 10^6, 10^5 and 10^4 bps. For frequencies within the range of 10^6 and 10^5 bps, C56 and C57 are added to the circuit and for the lowest frequency range, C58 and C59 are also added. Thus, the bypass capacitance is increased for each progressively lower frequency range. The feedback capacitors are also selectable and, for each lower range of operating frequencies, their total capacity increases progressively. The S and T filters operate in a manner identical to the Q and S filters, respectively.

Feedback and Bypass Capacitor Banks and Control Circuit. This circuit includes the R-to-Q feedback capacitor bank (C17 through C22, K1, and K2), the T-to-S feedback capacitor bank (C47 through C49, C64, C71, K5 and K6), the R bypass capacitor bank (C33, C56 through C59, and part of K7 and K8), the T bypass capacitor bank (C60 through C63 and part of K7 and K8), and capacitor decade control (U1C, U1B, U2A, U2B, U2D and U2E). The logic elements within the capacitor decade control decode signals DEC 1 and DEC 2 to determine the operating frequency range. Table 4-7 gives the levels of these signals for each applicable frequency range, the relays that are energized, and the active capacitors of each affected circuit.

Table 4-7. Tracking Capacitor Selection

	BIT RATE RANGE		
	10^4	10^5	10^6
*DEC 2 *DEC 1	0 0	0 1	1 0
Relays Energized	K1, K2, K5, K6, K7, K8	K1, K5, K7	None
R to Q Feedback Capacitors Selected	C17 thru C22	C17 thru C20	C17, C18
T to S Feedback Capacitors Selected	C47 thru C49 C64, C71	C47, C48, C71	C47
R Bypass Capacitors Selected	C33, C56 thru C59	C33, C56, C57	C33
T Bypass Capacitors Selected	C40, C60 thru C63	C40, C60, C61 C62	C40, C60

* DEC 4 is high when HF tracking filter is processing PCM; thus, DEC 1 and DEC 2 are decoded as 10^4, 10^5 and 10^6 rather than 10^0, 10^1, 10^2 and 10^3. When processing HF PCM (>104) DEC 1 = 1 and DEC 2 = 1 is not a valid combination.

Raysistor Control Circuit. The Raysistor control circuit includes operational amplifier U3 and emitter follower Q13 which provide amplification for the VD1 signal, relays K3 and K4 with their associated logic elements U1A, U1B, U2A and U2B, which direct the amplified VD1 signal to one of two inputs of each Raysistor driver, and emitter follower Q14 which, from the -6.2 volt reference signal provides a +2 volt reference signal for each Raysistor driver.

Signal VD1 is applied through R6 to one input of the operational amplifier. The other input is referenced to ground through R131. The output of U3 is applied to the Q13 base and then developed across one of two circuits depending on whether K3 or K4 is energized. When the two most significant bits of the most significant digit of the operating frequency are ZERO, indicating that the operating frequency is equal to or less than 3.999×10^x bps, K3 is energized and K4 is de-energized. Thus, during the lower frequency range, the output signal from Q13 is developed across the circuit composed of R27 and one of the two input circuits of each Raysistor driver to the +2 volt reference signal. In the Q Raysistor driver, which is typical of the remaining drivers, this input circuit includes the parallel-connected resistors R35 and R36 and the resistive element (pins 1 and 6) of Raysistor Z1. When either MSD 8 or MSD 4 is a ONE, indicating that the operating frequency is equal to or greater than 4.000×10^x bps, K3 is de-energized and K4 is energized. Thus, during the higher frequency range, the output signal from Q13 is developed across the circuit composed of R27 and the other input of each Raysistor driver to the +2 volt reference signal. In the Q Raysistor driver, this input circuit includes the parallel-connected resistors R33 and R34 and the resistive elements (pins 1 and 6) of Raysistor Z1.

Resistor R7 and capacitor C27 are included to stabilize the gain versus frequency characteristics of U3 and Q13. Capacitors C24 and C25 bypass to ground any signal currents from the source voltage lines. Resistor R130 provides isolation for test point 3 and prevents damage to the circuit if the test point is accidentally grounded.

The -6.2 volts reference signal is applied through R28 to one input of U5, the other input is referenced to ground through R29. The output of U5 is applied to the Q14 base. Transistor Q14 provides the return path to -15 volts for the amplified VD1 signal and is controlled, via its base voltage, to provide a constant +2 volts at the junction of R30 and R8. Parts R8, C26, C29 and R133 perform the same function in this circuit as their corresponding parts performed in the U3 and Q13 circuit (see preceeding paragraph).

Raysistor Drivers. The Q, R, S and T Raysistor drivers are all identical; therefore, only the Q driver is explained. Raysistor Z1 is a device whose resistive elements change their value from 2000 to 200 ohms as the current is increased through the bulb element (pins 2 and 5). Current control for the bulb element is provided by the amplified VD1 signal which is developed across the resistive element connected to pins 1 and 6 of Z1. One end of this element is connected to the +2 volt reference signal. Thus, the input to U6 is the 2 V ±IR drop across pins 1 and 6 of Z1. The other input to U6 is grounded. Circuit operation is such that as VD1 increases with frequency, the input to U6 also increases. Because of the feedback effect of the resistive element connected to pins 1 and 6 of Z1 and by selection of the proper input resistors (R33 and R34 or R35 and R36), the increased voltage to U6 decreases the value of the resistive element connected to pins 6 and 1 of Z1 and also decreases the resistive element connected to pins 3 and 4 of Z1, which is the resistive element in series with each filter section. Therefore, when the operating frequency is increased, VD1 is increased, the value of the resistive element is decreased, and the RC time constant of the filter section is decreased.

The output of U6 is applied through R32 to the base of Q15 which controls the current through the bulb element of Z1. The voltage at the emitter of Q15 varies from approximately +1.2 volts at the low end of the frequency range to 3.5 volts at the high end of the frequency range. The network C30 and R31 decreases the time required for the circuit to respond to changes in VD1. Diode CR5 prevents the base of Q15 from going negative. Capacitors C31 and C32 bypass to ground any signal currents on the voltage source lines.

HF-NRZ-MF Summing Amplifier. This summing amplifier includes Q31 through Q35, the elements of U13 and associated parts. Filtered NRZ input (pin 30) is not used in this equipment; it is connected to digital ground. Because this input is grounded, and because approximately 2.3 volts from the junction of R106 and R107 is applied to the base of Q32, transistor Q32 is conducting. The current flowing from the -15 volt source through Q33, Q32 and R109 provides approximately

+12 volts on the base of Q34 to hold this transistor in conduction. Resistors R102 and R103 provide approximately 7.5 volts for the base of Q33.

The S input is applied through R120 to the emitter of U13Q3, the other two inputs, R and T, are applied through R123 and R124 respectively to the emitter of U13Q4. The bases of these two transistors are clamped to 0.7 volt obtained from the junction of R119 and the diode-connected transistor U13Q5. The output voltages are developed across collector load resistors R113 and R114 and applied to the bases of the matched-pair transistors Q35A and B. The positive source voltage for the collectors of Q3 and Q4 is applied through R112 and the collector-emitter circuits of U13Q1 and U13Q2. The bases of these transistors are held at approximately +10 volts obtained from the junction of R111 and R118.

The outputs of the collectors of Q35 are the HF-NRZ-MF and $\overline{\text{HF-NRZ-MF}}$ signals. The emitters of these transistors are returned through respective isolation resistors, R115 and R116, to a source of approximately +10 volts obtained from the collector of Q34. Both output signals are superimposed on a dc voltage of approximately +6 volts.

HF-SØ-MF Summing Amplifier. This summing amplifier which combines the Q, R, S and T filter outputs, operates in the same manner as the HF-NRZ-MF summing amplifier described in the preceding paragraph; however, in this circuit the current source transistor Q23 is kept conducting by a fixed bias rather than the gating circuit as in the HF-NRZ-MF summing amplifier. The fixed bias of approximately +12 volts is obtained from the junction of R55 and R56.

4.8.5 LF Matched Filter Type VAF027

The type VAF027 card (see schematic drawing 460-0908) contains the circuits of the low frequency tracking filter section (see figure 4-9) and the circuits of the low frequency threshold detector section (see figure 4-10). Circuits in the low frequency tracking filter section include the line receiver, VD1 buffer, the filter sections with their resistive feedback circuits, decade control circuit, LF-SØ-MF summing amplifier and LF-NRZ-MF summing amplifier. Circuits in the low frequency threshold detector section include the control gating circuit, LF-NRZ-MF receiver amplifier, LF-SØ-MF receiver amplifier, voltage reference generator, 3/4T comparator, SØ comparator, 1/2T comparator, offset comparator, RZ mixer, RZ comparator, SØ-RZ comparator, 3-way UL select circuit, internal-external U select circuit, and drivers No. 1 through No. 8. Each of these circuits is explained in the following paragraphs.

Line Receiver. The line receiver converts the true and complement forms of the LF INPUT signal to a single-ended signal that is applied to the Q filter. The input signals control the amount of current flowing

through transistors Q5 and Q6. The current flowing through Q5 also flows through the input leg of a current mirror circuit which includes U7Q4 and R15. Resistor R15 is connected to a voltage source of -7.5 volts obtained from the junction of R16 and Zener diode CR1. Because the voltage drop across R15 plus the diode drop of the base-emitter junction of U7Q4 is equal to the voltage drop across R17 plus the diode drop of diode-connected transistor U7Q5, and also because the resistors and transistor junctions in each leg are matched, the current in the output leg of the current mirror circuit is equal to the current in the input leg. Transistor U7Q3 and diode-connected transistor U7Q2 divert excess current from the output leg into load resistor R14. Thus, when the current of the LF INPUT is relatively high and the current of the LF INPUT is relatively low, the excess current flowing in the output leg flows into R14 and causes a negative voltage (approximately -1 volt) to be developed across R14. When the polarity of the input signal changes, the current of the LF INPUT is relatively low and the current of the LF INPUT is relatively high. The output leg supplies only a portion of the current required by Q2; the remainder is supplied through R14 and causes a positive voltage (approximately +1 volt) to be developed across R14. The series circuit consisting of R11 and R13 provides approximately 6 volts for the fixed base bias of Q5 and Q6. This circuit is bypassed by capacitor C3.

VD1 Buffer. The VD1 buffer is operational amplifier U8 and associated parts. The VD1 signal is applied through R19 to the non-inverting input of U8. The output is applied to the four filter sections. Capacitors C5 and C6 bypass to ground any signal currents on the +15 and -15 volt lines, respectively.

Filter Sections. There are four filter sections identified as Q, R, S and T that sequentially affect the LF INPUT signal. The output of each filter is selectively routed to two summing amplifiers. The values of selected parts in each filter are changed as the input signal frequency is changed to ensure the bandpass characterisitics remain constant over the operating frequency range of 1.000×10^0 to 9.999×10^3 bps. This tracking capability is implemented by selecting for each of four frequency ranges a combination of resistance values.

The selected resistance is developed across field effect transistors (FETs). Each of the FETs is placed in the high or low resistance condition by control levels from the decade control circuit which decodes DEC 1 and DEC 2 to establish the frequency range of 10^0, 10^1, 10^2, or 10^3 bps. There are a total of 12 FETs used in the four filter sections, 6 in the first pair (Q and R) and 6 in the second pair (S and T). The two pairs of filters are identical. In the first pair, the FETs control the following circuits. Q8 controls the RC time constant to the input of U1. During frequency ranges of 10^0 and 10^2 bps, Q8 is off and causes a long time constant and in the other two frequency ranges, 10^1 and 10^3 bps, Q8 is on and causes a short time constant. To compensate for the short time constant (or long time constant) for two

different ranges, and to provide the desired tracking through U1, FET Q9 provides a high resistance in series with feedback capacitor C7. This decreases the feedback voltage during frequency ranges of 10^2 and 10^3 bps. During frequency ranges of 10^0 and 10^1, Q9 provides a low resistance and, in effect, connects C7 in parallel with C8 which increases the feedback voltage. Therefore, because of FETs Q8 and Q9, four sets of conditions exist for the RC time constant and feedback voltage which provide the desired bandpass characteristics for U1 for the four frequency ranges. FETs Q11 and Q12 provide frequency compensation for U6 in the same manner Q8 and Q9 provide frequency compensation for U1. FET Q7 controls the feedback voltage from the output of the Q filter (output of U3) to the input of the Q filter and FET Q10 controls the feedback voltage from the output of the R filter (output of U6) to the input of the Q filter. These feedback circuits are used with the previously described methods of frequency compensation to provide the desired frequency versus gain tracking characteristics for the first two filter sections. The second two filter sections contain identical frequency compensation hardware.

The Q filter includes operational amplifiers U1 and U3 and multiplier integrated circuit U2. The input signal is applied from the line receiver through FET Q8 and operational amplifier U1 to pin 9 of differential input No. 1 of U2. U2 has two differential inputs; differential input No. 1 is at pins 6 and 9 and differential input No. 2 is at pins 10 and 13. The single-ended output is at pin 14. Pins 1 and 3, 7 and 8, and 11 and 12 are provided for the connection of external resistors to establish parameters within the integrated circuit. The pin 6 input is referenced to ground through R32. The output of VD1 buffer is applied through R35 to pin 13 of differential input No. 2 of U2. The pin 10 differential input No. 2 receives a dc voltage from potentiometer R31 which is connected between +4.3 and -4.3 volts generated within U2. This potentiometer is used to set the static gain of the multiplier. The output from the multiplier (pin 14) is applied through another operational amplifier, U3, whose output is the Q bus. Potentiometer R36 and resistor R37 form a feedback circuit for U3. This potentiometer is adjusted to set the overall gain of the filter section.

The R filter includes multiplier integrated circuit U4 and operational amplifiers U5 and U6. Operation of this filter is practically identical to that of the Q filter. The difference is in the sequence of the elements, that is, the signal flow is through U4, U5 and then U6 to the R bus. An additional control, R9, also is provided. This control compensates for any offset in the output signal that is caused by different values of VD1. The final difference is that, because of polarity considerations, the input signal (Q bus) is fed to pin 6 of differential input No. 1 of U4 and pin 9, the other input, is grounded. Except for potentiometer R88, the S and T filters are identical to the Q and R filters, respectively. This potentiometer is used to eliminate any offset that may occur in the output signal on the T bus.

Decade Control Circuit. The decade control circuit contains the DEC 1 differential amplifier and the DEC 2 differential amplifier. Each amplifier operates as follows. The DEC 1 differential amplifier consisting of Q1 and Q2 receives, through pin 34 and R1, the control level DEC 1 from program control. When DEC 1 is high, the base voltage applied to Q1 is more positive than the Q2 base voltage of the +1.5 volts obtained from the junction of R6 and R7, therefore, Q1 is cut off and Q2 is conducting. During this time, it is the Q2 emitter current flowing through R2 that causes a common emitter voltage of approximately +2.2 volts. It is this voltage that reverse biases Q1. Because Q2 is on, the Q2 collector goes to approximately +1 volt due to the voltage drop across R3. The Q2 collector voltage is applied to parallel-connected gate input circuits for FETs Q7, Q8, Q10, Q12, Q13, Q15, Q17 and Q36. Each input circuit consists of series-connected diode and resistor. For FET Q8, CR2 is the diode and R22 the resistor, and this is typical for the remainder of the FETs. The high Q2 collector voltage produces approximately 0 volts at each junction between diodes and resistors. This 0 volts holds the FETs on. When DEC 1 is low, the base voltage applied to Q1 is less positive than the Q2 base voltage of 1.5 volts; therefore, Q1 is conducting and Q2 is off. During this time, it is Q1 emitter current flowing through R2 that causes a common emitter voltage of approximately +0.7 volt. It is this voltage that reverse-biases Q2. Because Q2 is off, the Q2 collector goes to approximately -15 volts. This voltage, when applied to the gate input circuits of FETs Q7, Q8, Q10, Q12, Q13, Q15, Q17 and Q36, causes the FETs to be off and thus provides a high impedance path between the source and drain elements.

The DEC 2 differential amplifier consisting of Q3 and Q4 receives, through pin 33 and R4, the control level DEC 2 from the program control. When DEC 2 is high, the base voltage applied to Q3 is more positive than the Q4 base voltage of 1.5 volts; therefore, Q3 is cut off and Q4 is conducting. During this time, it is the Q4 emitter current flowing through R5 that causes a common emitter voltage of approximately +2.2 volts. It is this voltage that reverse-biases Q3. Because Q3 is off, the Q3 collector goes to approximately -15 volts. This voltage, when applied to the gate input circuits of FETs Q9, Q11, Q14 and Q16, causes the FETs to be off and thus provides a high impedance path between the source and drain elements. When DEC 2 is low, the base voltage applied to Q3 is less positive than the Q4 base voltage of 1.5 volts; therefore, Q3 is conducting and Q4 is off. During this time, it is Q3 emitter current flowing through R5 that causes a common emitter voltage of approximately +0.7 volt. It is this voltage that reverse-biases Q4. Because Q3 is on, the Q3 collector goes to +1 volt due to the voltage drop across R8. This voltage applied to the gate input circuits of FETs Q9, Q11, Q14 and Q16, causes the FETs to be on and thus provides a low impedance path between the source and drain elements.

LF-SØ-MF Summing Amplifier. The LF-SØ-MF summing amplifier includes operational amplifier U11 and associated parts. The R, S and T signals from their respective filters are applied through resistors R63, R62 and R61, respectively, to the inverting input (pin 2) of operational amplifier U11. The output of the Q filter is divided across the series circuit consisting of R59 and R60; that portion of the Q signal across R60 is applied to the non-inverting input (pin 3) of operational amplifier U11. The output (pin 6) of U11 is LF-SØ-MF. Resistor R64 provides the necessary feedback for the operational amplifier. Capacitors C25 and C26 bypass to ground any ac currents from the +15 and -15 volt source lines, respectively.

LF-NRZ-MF Summing Amplifier. The LF-NRZ-MF summing amplifier includes operational amplifier U10 and associated parts. The R and S signals from their respective filters are applied through resistors R55 and R56, respectively, to the inverting input (pin 2) of operational amplifier U10. The output of the T filter is divided across R54 and R53; that portion of the T signal across R53 is applied to the non-inverting input (pin 3) of operational amplifier U10. The output (pin 6) of operational amplifier U10 is LF-NRZ-MF. Resistor R57 provides the necessary feedback for the operational amplifier. Capacitor C23 bypasses to ground any ac currents from the +15 volt dc source line.

Control Gating Circuit. The control gating circuit includes the logic elements of ICs U27 and U31. The elements of U27 are inverters. The elements of U31 are positive, non-inverting AND gates; therefore, only when both inputs are high is the output high. The four input levels of CNRZ, CSØ, CRZ and DEC 4 are combined in these elements to produce output levels $\overline{\text{DEC 4}}$.NRZ from the combined outputs of U27E and U27F, NRZ from the output of U31B, $\overline{\text{DEC 4}}$ from the output of U27D, $\overline{\text{SØ1}}$ from the output of U27A, $\overline{\text{SØ2}}$ from the output of U27B, NRZ·$\overline{\text{DEC 4}}$ from the output of U31A, SØ·$\overline{\text{DEC 4}}$ from the output of U31D and RZ·$\overline{\text{DEC 4}}$ from the output of U31C.

LF-NRZ-MF Receiver Amplifier. Essentially, the LF-NRZ-MF receiver amplifier is differential amplifier U25 which receives its input signal from the LF-NRZ-MF summing amplifier through FET Q18 and R134. FET Q18 operates as a switch; however, because the FNRZ circuit is not used, FET Q18 is held in conduction by the circuitry including Q21 through Q23 and associated parts. Basically, pin 11 is wired to a ground level which turns Q23 on, Q22 off, Q21 on and Q20 off. Thus, the resultant high level at the gate of FET Q18 holds the FET in conduction and allows the input signal to be applied to U25. The network consisting of CR19, R141 and R43 limits the negative excursion of the input signal to approximately -2.3 volts. The network consisting of CR20, R144 and R145 limits the positive excursion of the input signal to approximately +3.7 volts. The output signal from pin 6 of U25 is fed back to the inverting input (pin 2) for feedback. Capacitors C49 and C50 bypass to ground any ac currents on the +15 volt and -15 volt source lines.

LF-SØ-MF Receiver Amplifier. Essentially, the LF-SØ-MF receiver amplifier is differential amplifier U23 which receives its input signal from the LF-SØ-MF summing amplifier through R132 and C46. This input signal is applied to the non-inverting input (pin 3) of U23. The output voltage from pin 6 (approximately ±1 volt referenced about ground) of U23 drives differential amplifiers in the 1/2T comparator, 3/4T comparator, RZ mixer and offset comparator. Feedback for U23 is provided from pin 6 through the parallel combination of R128 and C45 to the inverting input (pin 2). The network consisting of CR12, R130, U22Q5 and R131 provides a fixed bias of 7 volts for the base of U22Q1. This transistor (U22Q1) and its emitter resistor R129 function as the load for LF-SØ-MF summing amplifier. The signal at the junction of U22Q1 collector and R132 is approximately 2 volts peak-to-peak and is referenced about -4 volts. Diode CR17 limits the positive excursion of this signal to -0.7 volt and diode CR18, which is returned to a reference voltage of -6 volts at Zener diode CR14, limits the negative excursion of this signal to -6.7 volts. Capacitors C47 and C48 bypass to ground any ac currents on the -15 volt and +15 volt source lines.

Voltage Reference Generator. The voltage reference generator includes differential amplifiers U18 and U19. A reference voltage is established with the network of R99 and Zener diode CR40. The reference voltage is applied to pin 2 and develops a voltage of +0.75 volt at pin 6. The relationship between R101 and R100 establishes the gain through the amplifier. The +0.75 volt is applied across resistor divider network R105 and R104 to obtain the +0.50 volt reference. The +0.75 volt also is applied through R102 to the inverting input (pin 2) of U19. The output at pin 6 is the -0.75 volt reference. The -0.75 volt is applied across resistor divider network R107 and R109 to obtain the -0.5 volt reference.

The 3/4T Comparator. The 3/4T comparator is U24 and is enabled through pins 9 and 13 when DEC 4 is a high level. The U24A receives through R123 the +0.75 volt reference. The other input to U24A is the output of the LF-SØ-MF receiver amplifier which is applied through R124. This signal also is applied to the pin 6 input of U24B. The pin 5 input of U24B receives the -0.75 volt reference through R125. The output of each amplifier is connected to pin 10 which provides a pulse that remains high as long as the positive portion of the input signal exceeds 0.75 volt, and as long as the negative portion of the input signal is more negative than -0.75 volt. Resistors R122 and R147 establish the proper gain through their associated amplifiers. An approximate -12 volts obtained from Zener diode CR13 and applied through pin 11 provides bias voltage for the pair of amplifiers. Another bias voltage (approximately -9 volts from Zener diode CR14) also is applied to the pair of amplifiers through pin 4.

The 1/2T Comparator. The 1/2T comparator is U20 and its operation is practically identical to that of the 3/4T comparator described in the preceding paragraph. The only difference is that a reference voltage of +0.5 volt is applied to pin 2 and a reference voltage of -0.5 volt is applied to pin 5 rather than the ±0.75 volt references as in the 3/4T comparator. Thus, at the output of the 1/2T comparator, is a

pulse that remains high as long as the positive portion of the input signal exceeds 0.5 volt, and as long as the negative portion of the input signal is more negative then -0.5 volt.

Drivers No. 1 and No. 2. Driver No. 1 includes U21Q1, U21Q2, U21Q6 and associated parts; driver No. 2 includes U21Q3, U21Q4, U21Q5 and associated parts. Both drivers are identical; therefore, only driver No. 1 is explained. U21Q1 and U21Q6 form a differential pair whose common emitter connection is returned through U21Q2 and R119 to the -15 volt source. U21Q2 is held in conduction because approximately -9 volts from CR14 is applied to its base. The input signal is applied to the base of U21Q1; the base of U21Q2 is biased with a fixed voltage of +1.4 volts obtained from the networks including R117, CR15 and CR16. The output signal, in its true and complement forms, is developed in the collector circuits of U21Q1 and U21Q2 for transfer to another card.

Offset Comparator. The offset comparator is U28; however, only one amplifier is enabled at any one time. When processing NRZ type PCM signals, NRZ·$\overline{\text{DEC 4}}$ enables U28B. This amplifier accepts through R168 and pin 6, the output of the LF-NRZ-MF receiver amplifier. The other input (pin 5) to U28 is referenced to ground through R167. The output at pin 10 is applied to drivers No. 3 and No. 4. When processing SØ type PCM signals, SØ·$\overline{\text{DEC 4}}$ enables U28A. This amplifier accepts the output of the LF-SØ-MF receiver amplifier through R166. The other input (pin 3) to U28 is referenced to ground through R164. The output at pin 10 is applied to drivers No. 3 and No. 4.

Drivers No. 3 and No. 4. Driver No. 3 includes U34Q1, U34Q2, U34Q6 and associated parts; driver No. 4 includes U34Q3, U34Q4, U34Q5, Q33 and associated parts. Both drivers are practically identical; therefore, driver No. 3 is first explained and the operation of the additional transistor Q33 is explained. U34Q1 and U34Q6 form a differential pair whose common emitter connection is returned through U34Q2 and R228 to the -15 volt source. U34Q2 is held in conduction because approximately -9 volts from CR26 is applied through R227 to its base. The input signal, applied to pin 2 base, is received from the offset comparator. The other input (+1.4 volts) to the differential pair is obtained from the voltage divider containing R231, CR35 and CR36. The output signal, in its true and complement forms, is developed in the collector circuits of U34Q1 and U34Q6 for transfer to another card. Transistor Q33 is an emitter follower that accepts at its base the output signal from the offset comparator. This signal is applied through R241 and developed across emitter resistor R237. When control level $\overline{\text{SØ2}}$ from control gating circuit is low (SØ type PCM signals are being processed), the dc level at the junction of CR37 and R236 is approximately 0 volt which holds U34Q3 off and U34Q4 on, because the 0 volt is below the 1.4 volts from the junction of R231 and CR35. Therefore, LF-OFST and $\overline{\text{LF-OFST}}$ are constant levels. When control level $\overline{\text{SØ2}}$ is high, the dc level at the junction of CR37 and R236 is approximately +4 volts. Since this voltage is more positive than the 1.4 volts on the base of

U34Q4, U34Q3 is turned on until the OFFSET signal from the emitter of Q33 drives the junction of R236 and CR37 below 1.4 volts, which causes U34Q3 and U34Q4 to change states. Thus, the output signals, LF-OFST and LF-OFST, are developed in the collector circuits of U34Q3 and U34Q4, respectively, when processing other than SØ PCM.

The RZ Mixer. The RZ mixer is U26 and associated parts. The outputs from both the LF-SØ-MF and LF-NRZ-MF receiver amplifiers are developed across resistors R148 and R154, respectively, and the input impedance of the inverting input (pin 2) of U26. The combined output at pin 6 is applied to SØ-RZ comparator and RZ comparator. Resistor R153 establishes the gain of the amplifier. Diodes CR21, CR22 and CR23 limit the excursions of the input signal between -0.7 and +1.4 volts.

The RZ Comparator. The RZ comparator is amplifier U30B and associated parts. The circuit is enabled only when a high RZ·DEC 4 control level from control gating circuit is applied to pin 9 of U30. One input, to pin 6, is +0.5 volt obtained from the junction of R186 and R187. This voltage is developed when the +0.75 volt from the voltage reference generator is applied across the series connected resistors R186 and R187. The other input, to pin 5, is from the RZ mixer and is applied through R184. The output, which is high as long as the input at pin 5 exceeds +0.5 volt, is applied to the 3-way UL select circuit.

The SØ Comparator. The SØ comparator is U29 and associated parts. It is enabled through pins 9 and 13 only when SØ·DEC 4 is a high level. The U29A section receives +0.75 volt reference through R171 to pin 2. The other input to U29A is the output of the LF-NRZ-MF receiver amplifier which is applied through R174. This signal also is applied to the pin 6 input of U29B. The pin 5 input receives the -0.75 volt reference through R175. The output of each amplifier is connected to pin 10, which provides a pulse that remains high as long as the positive portion of the input signal exceeds +0.75 volt, and as long as the negative portion of the input signal is more negative than -0.75 volt. Resistors R172 and R173 establish the proper gain through their associated amplifiers. An approximate -12 volts obtained from Zener diode CR25 and applied through pin 11 provides bias voltage for the pair of amplifiers. Another bias voltage (approximately -9 volts from Zener diode CR26) also is applied to the pair of amplifiers through pin 4.

The 3-Way U Select Circuit. The 3-way U select circuit includes Q26, Q27, Q28 and associated parts. The base of Q26 receives the U signal derived from SØ comparator only when processing SØ type PCM signals. During this time, Q27 and Q28 are cut off. Thus, the U signal derived from the output of the SØ comparator is developed across common emitter resistor R177 and then applied to driver No. 6. When processing

NRZ type PCM signals, the U signal derived from the 3/4T comparator is applied through Q27 and developed across R177. It is then applied to driver No. 6. During this time, Q26 and Q28 are cut off. In the third situation, when processing RZ type PCM signals, U signal derived from the RZ comparator is applied through Q28 and developed across R177. It is then applied to driver No. 6. The two transistors that are inactive when processing each type of PCM signals are held off by a low level from the comparator to the base of its respective transistor.

Internal-External U Select Circuit. The internal-external U select circuit includes Q34, Q35 and assoicated parts. When the EXT level, received through pin 12, is high, Q34 is held off and allows Q35 to be turned on. The base voltage of Q35 is fixed at +1.4 volts by the voltage divider consisting of CR38, CR39 and R240. Because Q34 is off, U33Q2 (part of driver No. 6) cuts off and inhibits the internally generated U signal. Because Q35 is on, the positive collector voltage of Q35 holds U33Q5 (part of driver No. 6) on and allows the external U signal to be applied through driver No. 6. When the EXT level is low, Q34 is turned on and, in turn, cuts off Q35 by increasing the positive voltage across common emitter resistor R239. Because Q34 is on and Q35 is off, the internally generated U signal is applied through driver No. 6 and the external U signal is inhibited.

Driver No. 5. Driver No. 5 includes differential pair U22Q3 and U22Q4, regulator transistor Q24 and associated parts. The output signal from LF-NRZ-MF receiver amplifier is applied to the pin 9 input of the differential pair; the other input is referenced to ground through R158. Transistor Q24, which regulates the current through the differential pair, is held at the proper state of conduction by the bias resistors R161, R162 and R163. Resistors R159 and R160 are included to establish the proper emitter voltages of U22Q3 and U22Q4. The output signal, in its true and complement forms, is developed in the collector circuits for transfer to another card.

Driver No. 6. Driver No. 6 includes the six transistors in the U33 integrated circuit and associated parts. This driver processes the output signal from the 3-way U select circuit in transistors Q1, Q2 and Q6; it also processes the EXT-U signal received from another card in transistors Q3, Q4 and Q5. However, only one of these circuits is enabled at a time as determined by the internal-external U select circuit. When Q34 is off, -9 volts from Zener diode CR32 is applied through R215 to the base of U33Q2 and holds U33Q2 off. Because U33Q2 is off, the differential pair, U33Q1 and U33Q6 is disabled. Meanwhile, Q35 is on and causes a voltage drop across R216. Because the voltage on the base of U33Q5 is less negative than the voltage on the base of U33Q2, U33Q5 is turned on and controls the current flow through differential amplifier U33Q3 and U33Q4. Input signals EXT-U and $\overline{\text{EXT-U}}$ are developed across terminating resistors R214 and R206, respectively, and are then applied through R212 and R205, respectively, to the inputs

of this differential pair. When this differential pair is operational, the output signal is applied from the collectors to the common output lines and through R210 and R211 to another card. When Q34 is on and Q35 is off (Q34 and Q35 are part of the internal-external U select circuit), -9 volts from Zener diode CR32 is applied through R216 to the base of U33Q5 and holds U33Q5 off which disables the differential pair, U33Q3 and U33Q4. Because Q34 is on, the voltage drop across R215 causes the base voltage of U33Q2 to be less negative than that on the base of U33Q5. Therefore, U33Q2 is turned on and controls the current through the differential pair, U33Q1 and U33Q6. The input to this differential pair is the output signal from the 3-way U select circuit; the input to the base of U33Q6 is a fixed voltage (+0.7 volt) from the junction of CR38 and CR39. When this differential pair is operational, the output signal is applied from the collectors to the common output lines and through R210 and R211 to another card.

The SØ-RZ Comparator. The SØ-RZ comparator is amplifier U30A and associated parts. This circuit is enabled only when a high $\overline{\text{NRZ·DEC 4}}$ control level from control gating circuit is applied to pin 2 of U30. One input, to pin 12, is obtained from the RZ mixer; this input is applied through R183. The other input, to pin 13, is referenced to ground through R188. The output which is applied to driver No. 7 is a pulse that is high as long as the input signal is above ground level.

Driver No. 7. Driver No. 7 contains a differential pair, U32Q1 and U32Q6, its associated control transistor U32Q2, Q29 and associated parts. Driver No. 7 is enabled only when control level $\overline{\text{SØ1}}$ is high. (SØ type PCM is not being processed). This high level permits Q29 to operate as an emitter follower, develop the signal from the output of the SØ-RZ comparator across R190 and then apply this signal through CR29 and R195 to the base of U32Q1 which is half of the differential pair. The input to the other half has a fixed bias of +1.4 volts obtained from the divider network composed of CR30, CR31 and R199. The control transistor U32Q2 has a fixed bias of -9 volts obtained from Zener diode CR28 and applied to the base through R196 which holds U32Q2 in conduction.

Driver No. 8. Driver No. 8 includes differential pair including U32Q3 and U32Q4, control transistor U32Q5 and associated parts. A fixed bias of +1.4 volts is obtained from the divider network composed of CR30, CR31 and R199 and is applied to one input of the differential pair, the base of U32Q4. The other input, at the base of U32Q3, receives its signal from the output of SØ-RZ comparator. The output signal, in true and complement forms, is developed in the collector circuits of the differential pair and then transferred to another card. The control transistor U32Q2 has a fixed bias of -9 volts obtained from Zener diode CR28 and applied to the base through R202. This bias holds U32Q2 in conduction.

4.8.6 Threshold Detector Type THD001

The type THD001 card (see schematic drawing 460-0906) contains circuits of the high frequency threshold detector section (see figure 4-6) and includes the following: control gating circuit, HF-NRZ-MF receiver amplifier, HF-SØ-MF receiver amplifier, voltage reference generator, 3/4T comparator, SØ-U comparator, 1/2T comparator, NRZ comparator, SØ comparator, CSØ inverter, RZ-U mixer, RZ mixer, LF/EXT-U receiver, drivers No. 1 through No. 9 and the U select circuit. Each of these circuits is explained in the following paragraphs.

Control Gating Circuit. The control gating circuit includes the logic elements of ICs U19 and U20, transistor Q23 with its associated parts and transistor U10Q1 with its associated parts. The elements of U19 are positive, non-inverting AND gates; therefore, only when both inputs are high is the output high. The elements of U20 are positive, inverting AND gates; therefore, only when both inputs are high is the output low. The five input levels of CNRZ, DEC 4, EXT, CSØ and CRZ are combined in these gates to produce output levels $\overline{\text{DEC 4}}\cdot\text{NRZ}$ from gate U20D, $\text{NRZ}\cdot\text{DEC 4}\cdot\overline{\text{EXT}}$ from gate U19B, $\text{CSØ}\cdot\text{DEC 4}\cdot\overline{\text{EXT}}$ from gate U19D, $\text{CRZ}\cdot\text{DEC 4}$ from gate U20C, $\text{CRZ}\cdot\text{DEC 4}\cdot\overline{\text{EXT}}$ from gate U19C and $\overline{\text{DEC 4}}$ from gate U20B. Level $\overline{\text{DEC 4}}$ is applied through R191 to the base of emitter follower Q23 and through R162 to the base of emitter follower U10Q1. Transistor U10Q2 is non-operational and considered an open circuit. The output signal from Q23, developed across emitter resistor R192, is applied through R193 to driver No. 4 and is applied through R190 to driver No. 8. The output signal from U10Q1, developed across emitter resistor R163, is applied through R160 to driver No. 1 and is applied through R223 to driver No. 7.

HF-NRZ-MF Receiver Amplifier. The HF-NRZ-MF receiver amplifier provides amplification and conversion from double-ended (complementary) signals to signals identified as N1 through N4. The conversion is accomplished by using a current mirror circuit consisting of Q11, U3AQ3 and R48 in one leg and U3AQ4, R49 and the diode-connected transistor U3AQ5 in the other leg. It is the characteristics of this circuit to cause the current through the second leg to equal the current through the first leg. Thus, as the current through the first leg is varied proportionally to the amplitude of HF-NRZ-MF, the voltage at the base of Q21 is the amplified complement of $\overline{\text{HF-NRZ-MF}}$. The amount of amplification is determined by Q11. Meanwhile, the current flowing through Q10 and R51 is proportional to HF-NRZ-MF. Because the two input signals are complementary to each other, when $\overline{\text{HF-NRZ-MF}}$ causes an increase in the mirror circuit and a resultant less positive voltage at the base of Q21, the HF-NRZ-MF signal causes a decrease in current through Q10 and R51 and thus, reinforces the less positive voltage at the base of Q21. When the complementary input signals change direction from that just described, the base voltage of Q21 goes more positive. Q21 is an emitter follower; the signal voltage developed across its emitter resistor R60 is applied through

isolation resistors R54, R56, R57 to the various circuits of the HF threshold detector card. The N1 output is applied through R59 and C13; the capacitor C13 blocks the dc level of the Q21 emitter voltage from appearing at the input of the SØ-U comparator. Resistors R45, R46 and R47 provide isolation for transistor elements to which they are connected. The network consisting of R50, C12 and CR8 provides a source of 7.5 volts for operation of the circuit. R52 and the diode-connected transistor Q22 form a pull-up circuit for the emitter of Q21.

HF-SØ-MF Receiver Amplifier. The HF-SØ-MF receiver amplifier, except for reference designations and signal names, is practically identical to the HF-NRZ-MF receiver amplifier described in the preceding paragraph. The one difference is in the output stage of the amplifier. The output signal from the emitter of Q1 is applied to the base of emitter follower Q3. The output signal, developed across R16, is applied through capacitive-resistive networks to the five driven circuits. The diodes CR1, CR2 and CR3 establish the proper bias for the emitter of Q3.

Voltage Reference Generator. The voltage reference generator provides sources of +1, +1.5 and +6 volts. Reference levels of 6.2 and 6.9 volts are established in the circuit consisting of R82, CR10 and CR9. From ground, the Zener diode CR9 develops 6.2 volts, and diode CR10 accounts for another 0.7 volt drop. This places the junction of CR10 and R82 at 6.9 volts. The remaining voltage to the +15 volt source is dropped across R82. The +6.2 volts from the Zener diode is divided in the series circuit of R80, R77 and R79. The 1 volt dropped across R79 is applied to the base of U1Q2 which establishes an emitter voltage of +0.3 volt. This emitter voltage establishes the voltage levels in the circuit from the -15 volt source through R78, the diode-connected transistor U1Q1 and R73, to the +15 volt source. Because of the fixed diode drop of 0.7 volt, the voltage at the junction of U1Q1 and R73 is the regulated 1 volt output. Capacitor C15 bypasses any signal currents to ground. The 1.5 volts dropped across R77 and R79 provide the regulated 1.5 volt output in the same manner as the 1 volt circuit. The +6 volt output is obtained by feeding 6.9 volts from the junction of R82 and CR10 to the base of Q16. This voltage is fed to the base through current limiting resistor R83. The resultant emitter voltage of Q16 is the regulated +6 volt output. Capacitor C17 bypasses any signal currents to ground.

The 3/4T Comparator. The 3/4T comparator receives the S3 output of the HF-SØ-MF receiver amplifier. This signal is developed across R119 and then applied through R120 to the base of U8Q4. The 1.5 volts from the voltage reference generator is dropped across R118 and R119. The voltage (0.75 volt) at the junction of these resistors provides the dc base bias for U8Q4. The output signal, developed across emitter resistor R123, is applied through R124 to the bases of U9Q4 and U9Q6. The dc level at these bases is zero volts and the input signal varies between +1.0 and -1.0 volt. Transistors U9Q4 and U9Q6 form differential pairs with U9Q3 and U9Q1, respectively.

Transistors U9Q2 and U9Q5 with their associated resistors (R132, R134, R135 and R136) provide current control through their associated differential pairs. Bias voltage for the current control transistors is obtained from the junction of resistors R170 and R174 in the SØ-U circuit.

Dc reference levels are individually applied to the base of one transistor in each differential pair. One reference, for U9Q1, is obtained from the emitter of U8Q3. The +1.5 volts from the voltage reference generator is applied through R117 to the base of U8Q3. The constant current flowing through R121, U8Q3 and R112, develops a constant voltage (0.75 volt) at the emitter of U8Q3. This voltage, applied through R129, is the reference voltage at which U9Q6 will be turned on when the base voltage of U9Q6 exceeds the reference voltage. The other reference voltage (-0.75 volt) is developed at the emitter of U8Q5 and applied through R131 to the base of U9Q3. Each reference voltage circuit contains a capacitor (C18 and C19) connected to ground. These capacitors bypass to ground any signal currents in the reference voltage circuits.

During the quiescent state, no signal is applied to the bases of U9Q6 and U9Q4; thus, transistors U9Q1 and U9Q4 are conducting. Because the conducting transistors are drawing current through R128, the collectors of U9Q1 and Q9Q4 are at a low level of approximately +6 volts. Because transistors U9Q6 and U9Q3 are off, their collectors are at a high level limited to 0.7 volt above the other output by CR17. Thus, this level is approximately +6.7 volts.

When a positive-going ramp voltage starting at zero is applied to the bases of U9Q4 and U9Q6, the circuit remains in its quiescent state as described above until the ramp voltage reaches +0.75 volt. At this time, U9Q6 turns on and U9Q1 turns off. Thus, U9Q6 and U9Q4 are both conducting and U9Q1 and U9Q3 are off. Because U9Q4 is drawing current through R128 and U9Q6 is drawing current through R122, the two output lines have equal voltages of approximately 6.3 volts. The circuit remains in this condition until the positive-going ramp reaches its peak voltage (approximately +1 volt) and then continues in a negative-going ramp. As the ramp voltage goes below +0.75 volt, the base of U9Q6 goes negative with respect to the reference voltage on the base of U9Q1 and causes U9Q6 to turn off and U9Q1 to turn on. Now both U9Q1 and U9Q4 are drawing current through R128 which is the same condition that existed in the quiescent state. The circuit remains in the quiescent state until the negative-going ramp voltage reaches -0.75 volt. At this time, U9Q4 turns off and U9Q3 turns on. Now, only U9Q1 is drawing current through R128 and only U9Q3 is drawing current through R122. This causes the two output voltages to be equal and approximately 6.3 volts. The circuit remains in this condition until the negative-going ramp reachs its peak negative voltage of approximately -1 volt and then continues in a positive-going ramp.

As the ramp voltage goes above -0.75 volt, the base of U9Q4 goes positive with respect to the base voltage of U9Q3 and causes U9Q4 to turn on and U9Q3 to turn off. Because both U9Q1 and U9Q4 are drawing current through R128, the circuit is again in the quiescent state.

The resultant two output signals are complementary to each other and have pulses whose width is proportional to the time that the input signal is above the high reference level of +0.75 volt or below the low reference level of -0.75 volt. Therefore, as the amplitude of the input signal (S3 which is derived from HF-SØ-MF) increases, the width of the output pulses increases and conversely, as the amplitude of the input signal decreases, the width of the output pulses decreases.

The SØ-U Comparator. The SØ-U comparator receives the N1 output of the HF-NRZ-MF receiver amplifier. This signal, superimposed on a dc level of 0.75 volt obtained from the junction of R110 and R111, is applied through R114 to the base of emitter follower U8Q1. Transistor U8Q2 is connected so that it is disabled and is considered an open circuit. The output signal from U8Q1 has a quiescent level of zero volts and is developed across emitter resistor R125. The signal is applied to two pairs of differential amplifiers; one pair is formed by U12Q1 and U12Q6 and the other pair is formed by U12Q4 and U12Q3. Transistor U12Q1 receives a +0.75 volt dc reference voltage and transistor U12Q3 receives a -0.75 volt dc reference voltage. These voltages are obtained from the 3/4T comparator. The operation of the two differential pairs and their associated current control transistors U12Q2 and U12Q5, is identical to that of the comparable parts in the 3/4T comparator described previously.

The 1/2T Comparator. The 1/2T comparator receives S2 output of the HF-SØ-MF receiver amplifier. This signal, superimposed on a dc level of 0.5 volt obtained from the junction of R139 and R145, is applied through R144 to the base of emitter follower U10Q4. The output signal from U10Q4 has a quiescent level of approximately -0.2 volt; thus, when a normalized signal of ±1.0 volt is superimposed on the quiescent level, the signal developed across emitter resistor R146 varies between +0.8 and -1.2. This signal is applied through R149 to two pairs of differential amplifiers; one pair is formed by U11Q1 and U11Q6 and the other pair is formed by U11Q4 and U11Q3. Transistor U11Q1 receives a +0.2 volt dc reference voltage from the emitter of U10Q3 and U11Q3 receives a -0.6 volt dc reference voltage from the emitter of U10Q5. These parameters result in complementary output signals; one from the collectors of U11Q1 and U11Q4 and the other from the collectors of U11Q3 and U11Q6. These output signals are pulses whose transistions occur at 1/2 the amplitude of the normalized input signal. When the input signal is above normalized amplitude, the width of the output pulses is increased, and when the input signal is below normalized amplitude, the width of the output pulses is decreased. These output pulses are developed in the same manner as those in the 3/4T comparator.

NRZ Comparator. The NRZ comparator includes transistors U2Q4, U2Q5, U4Q3, U4Q4, U4Q5 and U12 and associated parts. The input signal, N2, is applied to one side of a differential pair composed of U4Q4 and U4Q3. The other side of the differential pair receives, at its base, an approximate zero volt reference signal. Transistor U4Q5, which is connected in series with Q12, controls the current through the differential pair; also Q12 is turned on or off by CSØ from the CSØ switch. When processing signals other than split-phase, CSØ is low. The low level applied to the base of Q14 turns Q12 on, enabling the NRZ comparator circuit. When processing CSØ signals, CSØ is high and thus inhibits the circuit. The reference voltage is developed in the circuit consisting of U2Q4, U2Q5, Q4, R20, R22 and R25. The approximate zero potential is developed across resistor R25 and applied to the base of U4Q3. Operation of the differential pair is such that U4Q3 is turned on until the input signal exceeds approximately zero volts. When this occurs U4Q4 is turned on and U4Q3 is turned off. The circuit remains in this condition until the input signal returns to a value below zero volts. The input signal thus provides complementary signals across the collector load resistors R35 and R36. These load resistors are used in common with the differential pair in the SØ comparator; however, when the NRZ comparator is enabled, the SØ comparator is inhibited and when the SØ comparator is enabled, the NRZ comparator is inhibited. The differential voltage of the complementary output signals is limited to 0.7 volt by diodes CR6 and CR7.

SØ Comparator. The SØ comparator includes transistors U2Q3, U2Q1, U4Q1, U4Q2, U4Q6 and Q13 and associated parts. The input signal, S1, is applied through emitter follower U2Q3 to one side of a differential pair composed of U4Q1 and U4Q6. The other side of the differential pair receives, at its base, a -0.7 volt reference signal. Transistor U4Q2 which is connected in series with Q13, controls the current through the differential pair; also Q13 is turned on or off by CSØ from the CSØ switch. When processing split phase signals, CSØ is high. The high level applied to the base of Q13 turns Q13 on, enabling the SØ comparator circuit. When processing other than split phase signals, CSØ is low and thus inhibits the circuit. The reference voltage is developed in the circuit consisting of R21, U2Q1, R23, R38, R39 and C11. The -0.7 volt reference is developed at the junction of R38 and R39 and applied through R39 to the base of U4Q6. Operation of the differential pair is such that U4Q6 is turned on until the input signal exceeds -0.7 volt. When this occurs, U4Q1 is turned on and U4Q6 is turned off. The circuit remains in this state until the input signal returns to a value below -0.7 volt. The input signal thus provides complementary signals across the collector load resistors R35 and R36. These load resistors are used in common with the differential pair in the NRZ comparator; however, when the NRZ comparator is enabled, the SØ comparator is inhibited and when the SØ comparator is enabled, the NRZ comparator is inhibited. The differential voltage of the complementary output signals is limited to 0.7 volt by diodes CR6 and CR7.

The CSØ Switch. The CSØ switch is a differential pair containing Q14 and Q15. The CSØ control level is applied through R70 to the base of Q14. The other input to the differential pair is a dc reference voltage (approximately 1.5 volts) obtained from the voltage divider, R69 and R72, connected between +15 volt source and ground. The common emitter resistor R71 controls the current through the differential pair. When split phase PCM signals are being processed, CSØ is high, which turns off Q14 and because of the common emitter resistors, permits Q15 to be turned on. The resultant high level developed across R68 enables the SØ comparator circuit. Because Q14 is off, the low level developed across R67 inhibits the NRZ comparator circuit. When CSØ is a low level, the circuit parameters are reversed to inhibit the SØ comparator circuit and enable the NRZ comparator circuit.

The RZ-U Mixer. The RZ-U mixer includes emitter follower U15Q4, a differential pair including U16Q1 and U16Q6, a current control transistor U16Q2, emitter follower U15Q1 and associated parts. Transistor U15Q2 is disabled and considered an open circuit. One input signal, S4, is applied through U15Q4 to one side of the differential pair, the base of U16Q1. The other side of the differential pair receives, at its base, the N3 signal which is applied through emitter follower U15Q1. The N3 signal is dc coupled; thus, a separate biasing arrangement for U15Q1 is not necessary. Transistor U16Q2 controls the current through the differential pair; it has its base connected to a source of -0.17 volt obtained from SØ-U comparator circuit. The output signal, which is the sum of the two input signals, is developed in its true and complement forms across collector load resistors R215 and R216. The differential amplitude between the true and complement outputs is limited to 0.7 volt by diodes CR27 and CR28. The voltage divider, consisting of R202 and R203, which is connected between +1 volt and ground, provides a 0.5 volt base bias for U15Q4. The ac coupled signal, S4, from HF-SØ-MF receiver amplifier, is superimposed on this dc bias. Resistors R204, R217 and R218 are current limiting resistors that prevent oscillations from occurring in their associated transistors.

The RZ Mixer. The RZ mixer includes emitter follower U15Q3, differential pair including U16Q3 and U16Q4, a current control transistor U16Q5 and associated parts. One input signal, S5, is applied through U15Q3 to one side of the differential pair, the base of U16Q4. The N3 signal from emitter follower U15Q1 in the RZ-U mixer circuit is applied to the other side of the differential pair, the base of U16Q3. The base of U15Q3 is referenced to ground through resistors R208 and R209. The remaining parts of the circuit operate in the same manner as corresponding parts in the RZ-U mixer which is described in the preceding paragraph.

The LF/EXT-U Receiver. The LF/EXT-U receiver includes resistors R230 through R234 and Zener diode CR34. This circuit accepts the LF/EXT-U and LF/EXT-U from the type VAF027 card (see schematic drawing 460-0908) and superimposes the signals on a dc level of +6.2 volts which is developed across Zener diode CR34. The dc level establishes the proper bias voltages for the differential amplifier in the U select circuit.

Drivers No. 1 through No. 9. All drivers are very similar, so rather than explain each individually, driver No. 1 is explained as a typical driver and where necessary, other drivers are used as typical to explain features not incorporated in driver No. 1. Parts of some drivers are used in common with other drivers as in the case of the output circuits of drivers No. 1 and 2 and the input circuits of drivers No. 2 and 3. These circuits are also discussed.

The complementary signal inputs are applied to the bases of a differential pair formed by U7Q3 and U7Q4. R103 and R108 are isolation resistors which prevent oscillation. The current control transistor U7Q5 has as its base input, a control level derived from DEC 4 control level. A high signal at this base, turns U7Q5 on and thus allows the driver to be operational when processing low frequency PCM signals. Thus, when a high level enables U7Q5, the higher common emitter voltage holds U7Q2 off and thus inhibits driver No. 2. When a low level turns U7Q5 off, the fixed base bias of 0.7 volt from CR14 allows U7Q2 to conduct and thus inhibits driver No. 1. A similar arrangement exists for drivers No. 4 and No. 5. The output signals from the collectors of the differential pair in driver No. 1 or No. 2, as applicable, are fed through common isolation resistors, R100 and R101, to a common input receiver on a different card. The differential pair is essentially a current driver designed to drive the bases of a receiver (differential pair) on another card. The differential signals transmitted through this low impedance circuit minimize the possibility of crosstalk.

The control level that specifies whether or not a driver is enabled is applied to the base of the current control transistor, typically U7Q5. A high level applied to this base enables the driver and a low level inhibits the driver. In addition, in drivers No. 3, No. 6, No. 7 and No. 8, a transistor, typically Q17 of driver No. 3, is connected in parallel with the current control transistor and one of the transistors of the differential pair. When this transistor is held off by a low control level, the transistor has no effect on the driver; however, when a high control level applied to its base turns the transistor on, the larger current flow through the current control transistor emitter resistor, typically R98, biases the current control transistor off and thus inhibits the driver. Control levels derived from DEC 4-CRZ, DEC 4 and DEC 4-NRZ enable or inhibit the drivers as required. Derivation of the control levels were discussed earlier in the explanation of the control gating circuit.

The U Select Circuit. The U select circuit includes ICs U14 and U17, each containing 6 transistors. Basically, the circuit provides complementary signals identified as U and $\overline{U}$ which are derived from the output signals from the SØ-U comparator, the 3/4T comparator, the RX-U mixer or the LF/EXT-U receiver. Each of the four input signals is applied to a differential amplifier. Individual control levels from the control gating circuit are applied to the bases of current

control transistors associated with three of the differential amplifiers. The base of the fourth current control transistor (U17Q5) is connected to a source of 1.4 volts. When one of the control levels is present (high), its associated circuit is enabled and allows that signal to be applied through its differential amplifier and isolation resistors to the output pins where the U and $\overline{U}$ signals become available. When all three control levels are absent (low), the differential amplifier for the LF/EXT-U signal is enabled and thus allows this signal to be applied through its differential amplifier and isolation resistors to the output pins. Because the four circuits are practically identical to one another, only the transistors and associated parts that process the signal from the 3/4T comparator are explained in detail in the following paragraphs. Also, a more detailed explanation is given of how the LF/EXT-U circuit is enabled.

The input signal, in true and complement forms, is applied through R187 and R189 to the bases of U14Q1 and U14Q6 which form the differential amplifier. The emitters of the differential amplifier are connected to the -15 volt source through the current control transistor U14Q2 and R198. Resistor R198 is common to all current control transistors. When the control level applied to the base of U14Q2 is low, U14Q2 is turned on and thus prevents current flow through its differential amplifier. When the control level is high, U14Q2 is turned on to complete the current path of the differential amplifier. The high level at the base of U14Q2 is limited to approximately 2.1 volts by CR25 whose cathode is returned to the 1.4 volts available at the junction of R201 and CR32.

The base voltage of U17Q5 is held at +1.4 volts obtained from the series circuit of CR33, CR32 and R201 connected between ground and the +15 volt source. When any of the other three current control transistors are conducting, the common emitter voltage is +1.4 volts. Thus, U17Q5 is held off. When control levels to the other three current control transistors are all low, the common collector voltage would tend towards -15 volts; however, when it reaches approximately +0.7 volt, U17Q5 turns on. Thus, the LF/EXT-U circuit is enabled by the absence of the three control levels.

4.8.7 Code Converter Type CCR036

The type CCR036 card (see schematic drawing 460-0982) contains the circuits of the spill detector and transition loss delay generator section (see figure 4-12), the circuits of the code converter section (see figure 4-22), and the decade adder circuit of the program decoding section (see figure 4-26). The circuits of the spill detector and transition loss delay generator section include the transition detector, the clock counter and the delay select circuit. The circuits of the code converter section include the line receivers, the data shift register, the data code converter circuit, the DM clock phase resolver and the clock regenerator.

Transition Detector. The transition detector includes logic elements that provide a positive and negative 50-nanosecond RESET pulse each time the negative transition of HF-XNG or LF-XNG, as applicable, is received or when SPILL is generated in the delay select circuit. When the output of U29D goes high or SPILL goes high, the output of U30B goes low and triggers a one-shot circuit composed of U27C, U27B and U27A. During the quiescent condition, both inputs to U27C are high and the output is low. This low applied through U27B provides a high at U27B-6 which charges C7 to a high level through R2. The low from U27C-8 inhibits U27A. When the negative transition of HF-XNG or LF-XNG is received at U29D or the position transition of SPILL is received at U30B, the output of U30B goes low and provides a high at the output of U27C. This high primes U27A and also, through U27B, starts to discharge C7; however, the voltage across C1 holds U27A enabled for 50 nanoseconds. To ensure the output of U27C remains high for at least 50 nanoseconds, the low level at U27A-3 is applied back to U27C-10. The negative-going RESET pulse is used to clear U24. This pulse is inverted by U27D and used to clear U28 and U31.

Clock Counter. The clock counter contains three 4-stage binary counters, U24, U28 and U31, connected to form a 12-stage binary counter. The 90° CLK from the code converter section is applied to the input of the counter and continuously increments the counter until the counter is reset. Normally, the counter is reset before a count of 128 is reached. The output of U28-11 goes high when a count of 128 is reached and the output U31-11 goes high when a count of 2048 is reached. Both of these inputs are transferred to the delay select circuit.

Delay Select Circuit. The delay select circuit includes select gates U30A and inverter U29C. When SYNC is high, U30A provides a low output when the count from the clock counter reaches 128; otherwise, U30A provides a low output when the count from the clock counter reaches 2048. The low output from U30A is inverted by U29C and becomes SPILL. SPILL is applied through R4 to TP5.

Line Receivers. Line receivers U17 and U18 are identical elements; each contains two amplifiers that accept complementary signals and provide a single-ended signal. The signals applied to pins 1 and 2 appear as an output signal at pin 4 and the signals applied to pins 11 and 12 appear as an output signal at pin 9. The strobe inputs at pins 5, 6 and 8 are held high by the 5 volts applied through R11; therefore, these inputs do not affect the operation of the amplifiers. A collector voltage of approximately -5 volts obtained from the emitter of Q1 is applied to pin 13. Resistors R12, R13 and R14 establish the proper operating values for Q1. C4 is a bypass capacitor. Each input line is terminated in 75 ohms by resistors R7 through R10 and R15 and R16.

Data Shift Register. The data shift register includes the shift register U19, inverters C through F of U20, logic gates U21A, U21B and U16C and logic gates contained in U9B. When RZ, NRZ-L or SØ-L type PCM data is being processed, RZ+L applied to U19-6 is high and causes the four inputs at U19-2 through U19-5 to be transferred to U19-13, U19-12, U19-11 and U19-10 respectively, when CLK input applied to U19-8 and U19-9 goes low. Because inputs to U19-3, U19-4 and U19-5 are connected to ground, outputs at U19-12, U19-11 and U19-10 are low. The output at U19-13 is data (BD) in NRZ code.

Typical input data obtained at test point 6 is shown in waveform B of figure 4-29. This data is strobed through U19 by CLK, waveform A; the output at U19-13 is shown in waveform C. Notice in waveform C that the bits are delayed one clock period from those in waveform B. This occurs because the data is slightly delayed with respect to clock and is desired to prevent a race condition between data and CLK.

The outputs of U19-12 and U19-13 and their complements at the output of U20-8 and U20-6 are monitored by U9B. Because of the high applied to U9-9, this AND gate is primed while the low applied to U9-13 inhibits its associated AND gate. Thus, data applied through pin U9-10 appears at U9-8 and is then transferred to U10-12 in the data code converter. This signal is as shown in waveform D.

When NRZ-S or M, SØ-M or S or DM type PCM is being processed, RZ+L applied to U19-6 is low and causes the data at U19-1 to be serially shifted into the four flip-flops of U19 so that when processing NRZ-M, NRZ-S, SØ-M or SØ-S type PCM data, the last two bits can be monitored simultaneously; and when processing DM type PCM data, the last four bits can be monitored simultaneously. Four-bit monitoring, required by the DM clock resolver, is provided at the output of U16C which provides a low output when the four bits contains a mixture of ONEs and ZEROs or provides a high output when the four bits are all ONEs or all ZEROs. Two bit monitoring, required by the data code converter, is provided at the output of U9B which provides a high output when the two bits are different or a low output when the two bits are the same.

Data Code Converter Circuit. The data from U9-8 is shifted through U10B, U23B and U10A. When processing other than DM type PCM data, the shifting process is controlled by CLK from U18-9 or when processing DM type PCM data, the shifting process is controlled by DM CLK from U7-9. Selection of CLK is controlled by DM control level applied to U9A. The $\overline{Q}$ output of U10B when processing other than DM type PCM data is shown in waveform F. The CLK input of U10B is shown in waveform E. The Q output of U10B is the complement of the $\overline{Q}$ output of U10B. When $S \cdot S\emptyset + S\emptyset \cdot M$ is high the Q output of U10B is transferred through U23B; otherwise, the $\overline{Q}$ output of U10B is transferred through U23B. The signal applied to U10-2 when processing NRZ-L type PCM is shown in waveform G. The clock to U10-3 is shown

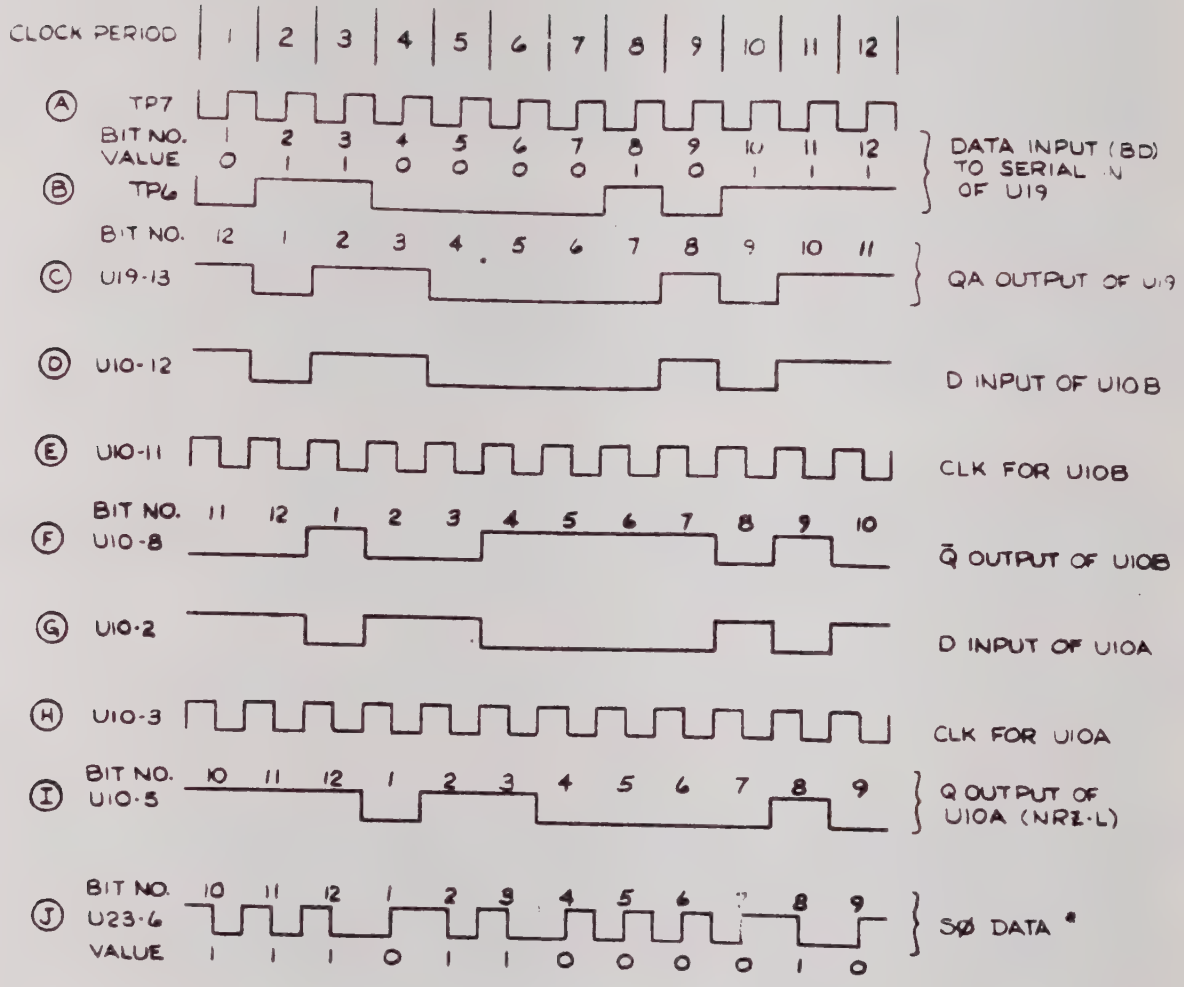


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Figure 4-29. Typical Waveforms of Code Converter when Processing NRZ-L Type PCM

in waveform H. The Q output of U10A, shown in waveform I, is the NRZ-L output data applied to the line drivers. This output and its complement obtained from $\overline{Q}$ of U10A is gated through U23A by complementary outputs of clock obtained from U26C and U22B. The output of U23A, shown in waveform J, is the SØ-L output data applied to the line drivers. This output also is applied through buffer U22A and R18 to the front panel test point labeled BiØ-L. The $\overline{Q}$ output of U10A is applied through inverter U26A and R19 to the front panel test point labeled NRZ-L.

DM Clock Phase Resolver. The DM clock resolver drives the DM clock from either the Q or $\overline{Q}$ output of U7B in the clock regenerator by clocking the output of U16C with Q output of U7B through one of two identical circuits and clocking the output of U16C with the $\overline{Q}$ output of U7B through the other identical circuit. Each of these circuits includes a flip-flop, U14A or U15A. When the J and K inputs of these flip-flops are high and the negative transition of clock occurs, the Q output changes states; otherwise, the Q output does not change. The two possible phases of DM clock from U7B, only one of which is the correct phase for code conversion, are applied to U15A-5 and U14A-5. The clock whose negative transition occurs first after the output of U16C goes high is the one with the proper phase. Because of the possibility of noise within the circuits, an indication of incorrect clock phase must occur eight times before the other phase of clock is selected for code conversion. The output transitions are applied to the clock input of an associated flip-flop,U15B or U14B, which changes the state of the Q and $\overline{Q}$ outputs each time the clock input goes negative. The Q output of each of these flip-flops is transferred to the input of an associated BCD counter.

Cross-coupled OR gates U5D and U16A form a flip-flop whose output at U5D-11 is normally high. Cross-coupled OR gates U16B and U16D also form a flip-flop whose output at U16D-11 is normally high. These high outputs are transferred to OR gate U5C and a flip-flop consisting of cross-coupled OR gates U5A and U5B. The state of this flip-flop gates the Q or $\overline{Q}$ output of U7B through U8B. The output of U8B is then clocked through U7A to become the DM clock.

Normally, the phase applied to U15A is the desired phase; therefore, the pulses through this flip-flop cause BCD counter U4 to reach a count of 8 before counter U3 reaches a count of 8. At a count of 3, U4-11 goes high and causes U5D-11 to go low immediately after the clock, applied to this OR gate, goes high. The low from U5D-11 is inverted to a high by U5C whose output resets both BCD counters and restores the DM clock phase resolver to its normal condition so that the process can be repeated. The low from U5D-11 also resets U14A and U14B; however, it does not affect the condition of the flip-flop formed by U5A and U5B.

If the desired phase of DM clock is applied to U14A-5, the pulses through this flip-flop cause BCD counter U3 to reach a count of 8 before counter U4 reaches a count of 8. At a count of 8, U3-11 goes high and causes U16D-11 to go low immediately after the clock, applied to this OR gate, goes high. The low from U16D-11 is inverted to a high U5C whose output resets both BCD counters. This low also changes the state of the flip-flop composed of U5A and U5B whose outputs change the source of DM clock through U8B. The low from U16D-11 also resets flip-flops U15A and U15B. Thus, the correct phase of DM clock was selected and the DM clock phase resolver is returned to normal condition.

Clock Regenerator. When processing DM type PCM signals, DM is high and directs the DM clock from U7A-9 through U9A into the data code converter. When processing other than DM type PCM signals, DM is low. The high from U6A directs the clock from U18-9 through U9A to the data code converter. In addition, the selected clock is applied through inverters U26F and U26C and becomes the 0 degree clock which is applied to the line drivers. The output of U26F is also applied through buffer U22B and becomes the 180 degree clock which is applied to the line drivers. The 180 degree clock is also inverted by U26B and applied through R20 to the 0° test point on the front panel.

When processing DM type PCM signals, DM, a high level, is applied to U8A-4 and directs the output of U8B-8 through U8A and then through U22C, U26D and U26E to provide the 90 degree and the 270 degree clocks. The output of U8B is 90 degrees displaced from the DM clock at U7A-9 because of U7A. The 90 degree and 270 degree clocks available at pins 11 and 13 are transferred to the line drivers. The 90 degree clock available at pin 10 is transferred to 90° test point on the front panel. The quadrature clock applied to U8A-3 is the source of the 90 degree and the 270 degree clocks when processing other than DM type PCM signal.

Decade Adder. The decade adder contains eight logic elements that perform AND, OR and inversion functions and a quadruple 2-line-to-1-line data selector U25. However, in U25, only three sets of inputs and three outputs are used. When the level to select (S) input is low, the A input of each pair is transferred to its associated output pin (Y) and when S is high, the B input of each pair is transferred to its associated output pin. The strobe (STR) is held enabled by a ground connected to pin 15. Thus, when DEC ADD is low, indicating that no carry is generated in the bit rate multiplier (see schematic drawing), RDEC 1, RDEC 2 and RDEC 4 are transferred through the A inputs of U25 and become DEC 1, DEC 2 and DEC 4, respectively. When DEC ADD is high, the outputs for each set of possible inputs are as shown in table 4-8.

Table 4-8. Decade Adder Truth Table

INPUTS			OUTPUTS		
RDEC 4	RDEC 2	RDEC 1	DEC 4	DEC 2	DEC 1
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	NOT VALID		

4.8.8 Transition Loss Delay Type LDY001

The type LDY001 card (see schematic drawing 460-1085) contains the counter control circuit, the divide-by-eight counter circuit and the loss storage and control circuit. (See figure 4-12). The card also contains an inverter (U3D) which is part of AUTO-CAL section (see figure 4-19). Each input and output terminal of the ICs (U1, U2 and U3) are individually connected to the connectors of the card; interconnection among the various elements of the ICs is accomplished in the library. Schematic drawing 460-1085 not only provides a true representation of the card but also includes a logic diagram showing the library connections. The circuits are explained in the following paragraphs.

During the quiescent state, SPILL is low, X-LOSS is low and DEL8 is high. When SPILL, applied to U3A goes high, CLEAR, the output of U3A, goes low. When low, CLEAR causes the output to the counter, DEL8, to go low and also sets the R-S flip-flop formed by U2C and U2D. The X-LOSS output from this flip-flop goes high indicating a state of transition loss. The circuit remains in this condition until $\overline{\text{LF-XNG}}$ or $\overline{\text{HF-XNG}}$ provides negative-going transitions indicating that data is being received. These transitions are inverted by U2A and become XNG. Because the QD output of the counter (DEL8) is low, the output of U3C, $\overline{\text{DEL8}}$, is high and primes U3B to allow the positive-going transitions of XNG to enable U3B. The resultant negative-going transitions, GATED CLK, from U3B are applied to the C1 input to the counter. When eight of these transitons are counted, DEL8 goes high which causes $\overline{\text{DEL8}}$ to go low thereby inhibiting U3B. Because U3B is inhibited, GATED CLK is a high level and does not affect the clock input of the counter. The high DEL8 from the counter primes U2B and allows the next, the ninth, XNG position transition to enable U2B. The resultant low output pulse, $\overline{\text{DELAYED XNG}}$, resets the R-S flip-flop and causes the X-LOSS signal to go low. The circuit remains in the condition just

described until SPILL level again goes high. Thus, X-LOSS is generated (goes high) immediately after SPILL is received (goes high) and is present until the ninth transition crossing from the low frequency or high frequency AGC and offset control circuit is received. Gate U3D is used as an inverter to provide RESET from EQUAL/RESET. Capacitor C1 is for high frequency bypassing of the +5 volt source. Resistors R1 and R2 are pull-up resistors.

4.8.9 Automatic Calibration Type ACL005/ACL009

The type ACL005/ACL009 card (see schematic drawing 460-1103) contains circuits of the voltage controlled oscillator section (see figure 4-17), circuits of the automatic calibration section (see figure 4-19)) and circuits of the DAC and decade range splitter section (see figure 4-20). Circuits of the voltage controlled oscillator section include gain selectable amplifier, amplitude control circuit, emitter controlled oscillator, current source, current multiplier, the ECO driver and the -6.2 volt reference generator. Circuits of the automatic calibration section include a full AUTO-CAL/2-second pulse generator, partial AUTO-CAL control circuit, 10-millisecond timing start control circuit, 400-nanosecond generator, frequency counter, 4-digit comparator, up/down counter circuit, VA DAC and the timing generator. Circuits of the DAC and decade range splitter section include the 8-bit DAC No. 1 and No. 2, combiner, controlled gain amplifier and the decade range splitter. Each of the previously mentioned circuits is explained in the following paragraphs.

Gain Selectable Amplifier. The gain selectable amplifier includes operational amplifier U1, gain control transistors Q4, Q7 and Q8 and associated parts. The Vx signal from the DAC and decade range splitter section is a voltage between 0.5 and 5 volts depending on the four significant digits of the dialed bit rate as explained in paragraph 4.4.4. This signal is applied to the non-inverting input of U1. The signal applied to the inverting input is a portion of the output voltage developed across R29 which is part of the feedback loop including as a maximum R36, R37 and R38. This portion of the input to U1, and therefore, the gain of U1, depends on which, if any, of the resistors are shorted by the control transistors. When control levels $\overline{D1}$, $\overline{D2}$ and $\overline{D3}$ are high, transistors Q4, Q7 and Q8 are turned off; therefore, the signal is developed through the feedback circuit including R38, R37, R36 and R29. The portion of the output signal developed across R29 is 1/8th, causing a gain of 8 in U1. Thus, as shown in table 4-1 the tuning voltage at the output of U1 is between 4 and 6 volts. When $\overline{D3}$ is low and $\overline{D1}$ and $\overline{D2}$ are high, Q8 is turned on and, in effect, shorts R38. Thus, 1/4th of the output signal is fed back to the input of U1, causing a gain of 4 in U1 and a resultant tuning voltage within the range of 3 to 6 volts. When D2 is low and $\overline{D1}$ and $\overline{D3}$ are high, Q7 is turned on and, in effect, shorts R37 and R38. Thus, one-half of the output signal is fed back to the input of U1, causing a gain of 2 in

U1 and a resultant tuning voltage within the range of 3 to 6 volts. When $\overline{D1}$ is low and $\overline{D2}$ and $\overline{D3}$ are high, Q4 is turned on and, in effect, shorts R36, R37 and R38. Thus, the entire output signal is fed back to the input of U1 and causes unity gain in U1 and a resultant tuning voltage within the range of 3 to 5 volts. The selectable range of tuning voltage is developed across R68 and then applied to the amplitude control circuit and the current multiplier circuit.

Amplitude Control Circuit. The amplitude control circuit includes current control transistor Q5, diode-connected transistor Q6, a linearity correction circuit consisting of Q9 and Q10 and associated parts. The base bias of Q5 is established at approximately 0.7 volt obtained from the network consisting of Q6 and R57. The bias voltage is applied through R47. Thus, the emitter of Q5 is held at a virtual ground, but the current through this transistor is controlled primarily by the -6.2 volts from the -6.2-volt reference generator and the VA signal from the automatic calibration section.

The total current through Q5 is reduced by the current flowing through Q9 of the linearity control circuit. Base bias of Q10 is approximately 3.2 volts obtained from the junction of R44 and R45. This base bias establishes an emitter voltage of approximately 2.5 volts developed across R43. The 2.5 volts is applied through R42 to the base of Q9. Therefore, when the tuning voltage applied through R39 exceeds approximately 3.2 volts, current is diverted from Q5 into Q9. As the tuning voltage increases, the current through Q9 increases. The value of the SBT resistor R39 controls the amount of current through Q9 and thus holds the current through Q5 proportional to the VA signal.

Emitter Coupled Oscillator. The emitter coupled oscillator includes Q11 through Q14, timing capacitor C19 and associated parts. Equal currents flow thrugh R49 and R50 from the current source. Q13 and Q14 alternately turn on and off thus generating a differential square wave voltage at their collectors. These voltages are applied to the ECO driver and also to the bases of Q11 and Q12 which are then also alternately turned on and off. The voltages at the collectors of Q11 and Q12 are therefore equal and opposite square waves whose amplitudes are controlled by the current flowing through Q5 and R48 of the amplitude control circuit. The collector voltages of Q11 and Q12 are capacitively coupled through C16 and C18 to the bases of Q13 and Q14, respectively, to provide the positive feedback for oscillation. The time duration of the cycle and, therefore, the oscillation frequency, is determined by the square wave voltage amplitude at the bases of Q13 and Q14 and the currents through R49 and R50. When Q13 turns on, Q14 turns off. Simultaneously, Q12 turns on and Q11 turns off so the base voltage of Q13 is approximately +0.5 volt and the base voltage of Q14 is approximately -0.5 volt. The emitter of Q14 is approximately 1 volt more positive than the emitter of Q13. Because Q14 is off, the current through R50 flows through C19 which causes the emitter voltage of Q14 to linearly decreawe. When this voltage decreases to 1 volt more negative than the emitter of Q13, Q14 turns

on which reverses the status of Q11, Q12 and Q13. The emitter of Q13 is now at 1 volt more positive than the emitter of Q14 and begins to linearly decrease in the manner just described, until Q13 again turns on.

Current Source. The current source includes U7Q3, U7Q4 and associated parts. This circuit provides equal division of the output current from the current multiplier required by the emitter coupled oscillator. Both transistors have a fixed base bias of approximately -3 volts which is developed by the divider network consisting of R65 and R66 and then applied to both bases through R53. Capacitor C20 ensures that any signal currents on the bases will be bypassed to ground.

Current Multiplier. The currents developed from the tuning voltage and applied through the current source transistors, U7Q3 and U7Q4, are varied over a 2 to 1 range to tune the emitter coupled oscillator in the following manner. The current through Q17 is determined by the tuning voltage and R67 because the emitter of Q17 is maintained at a virtual ground by U5. The current from Q17 generates a voltage across the series network consisting of R71, R73 and diode-connected transistor U7Q5. This voltage is applied to the bases of parallel connected transistors U7Q1 and U7Q2 resulting in a total current which is twice that in Q17 because the total of R71 and R73 is twice the value of R77 and the voltage across U7Q5 is equal to the base-emitter voltage of U7Q1 and U7Q2. This total current is then divided into two equal currents by the current source components.

The phase error signal is supplied in the form of differential currents, $-VCO\Delta I$ and $+VCO\Delta I$, which develop voltages across diode connected transistors U6Q5 and U6Q4. These differential voltages are applied to the bases of the variable gain differential amplifier composed of U6Q1 and U6Q2 whose gain is proportional to the current through R81. The VCO tuning voltage applied through R69 causes a proportionate current to flow through Q18 which, in turn, causes a voltage across R74 which is proportional to the tuning voltage. The collector voltage of Q18, after buffering by emitter followers Q19 and Q20, serves as the bias source for the bases of U6Q1 and U6Q2. The bias voltages are applied through the diode-connected transistors U6Q4 and U6Q5. Thus, the voltage across R81 is precisely equal to the voltage across R74 and the current through R81 is thereby proportional to the tuning voltage.

The phase error signal current from the collector U6Q2 flows through common base stage U6Q3 and is combined with the current in U7Q1 and U7Q2. The phase error signal current in U6Q1, which is equal in amplitude but opposite in phase to that in U6Q2, develops a voltage across R73 and U7Q5 which is applied through R71 to the bases of U7Q1 and U7Q2. The resultant signal current generated in U7Q1 and U7Q2 is now in phase with that in U6Q2 and U6Q3. The currents in the current source transistors, U7Q3 and U7Q4, are thus increased or decreased by the phase error signal from the nominal values established by the tuning voltage.

ECO Driver. The ECO driver is a differential amplifier consisting of Q15, Q16 and associated parts. The differential outputs of the ECO are developed across R56 and R60 and then are applied through R54 and R59 to the bases of Q16 and Q15, respectively. The differential output signals, VCO and $\overline{\text{VCO}}$, are developed in the collector circuits and applied through R62 and R63 to the countdown section. A bias voltage of +6.2 volts is developed at the junction of R61 and CR6 and applied through R56 and R60 to the elements of Q11 through Q16. R64 is the common emitter resistor for the differential amplifier.

The -6.2 Volt Reference Generator. The -6.2 volt reference generator includes operational amplifier U2, emitter follower Q3 and associated parts. The +6.2 volts developed at the junction of R18 and CR5 is applied through R19 and R20 to the inverting input of U2. R19 is used to adjust the -6.2 volt output. The output of the amplifier is applied to the base of Q3 and thus causes the output voltage to be developed across R24. The voltage fed back through R23, in conjunction with the voltage developed across R19 and R20, controls the overall gain of the operational amplifier and the emitter follower and thus stabilizes the output at -6.2 volts. Capacitors C13 and C14 function as filter capacitors while C11 and C12 function as bypass capacitors. R22 is the collector resistor for emitter follower Q3.

Full AUTO-CAL/2-Second Pulse Generator. The full AUTO-CAL/2-second pulse generator includes inverters U25F and U25B, NAND gates U14A and U26D, also a single-shot U13B. Input to U14A, pin 3, is normally high unless either of the two most significant thumbwheels of the bit rate is changed since the last full AUTO-CAL cycle. When RESET pushbutton is depressed, a high level is applied to pin 13 input to inverter U25F. The low level output of U25F provides a positive output level from U14A, pin 6, which triggers U13B and thus provides a negative pulse of 2 seconds duration at its $\overline{\text{Q}}$ output. This negative pulse becomes a positive pulse at the output of U26D; it is then inverted by U25B. If the RESET pushbutton is depressed and held longer than 2 seconds, the 2-second one-shot circuit will be overridden via the low level input to pin 13 of U26D, holding U26D, pin 11, high. The one-shot circuit insures a minimum 2-second full AUTO-CAL cycle.

Partial AUTO-CAL Control Circuit. The partial AUTO-CAL control circuit includes NAND gates U26A, U27C, inverter U25C, and a flip-flop comprising NOR gates U26B and U14B. During normal operation, X-LOSS and $\overline{\text{SYNC}}$ are both low levels. The high level output from U26A-3 is inverted by U25C. This low level will hold the flip-flop with a high at U14B-8 and a low at U26B-6. The partial AUTO-CAL strobe pulse from U16A-6 (see figure 4-30H) will be inhibited by the low level on U27C, pin 9, thus preventing the initiation of a partial AUTO-CAL cycle. Where X-LOSS and $\overline{\text{SYNC}}$ are high, the output of U26A-3 is low inverted by U25C; then pin 6 is high enabling NAND gate U27C. The AUTO-CAL strobe pulse will generate a negative pulse at U27C, pin 8, thus changing the state of the cross-coupled flip-flop, and initiate the partial AUTO-CAL cycle.

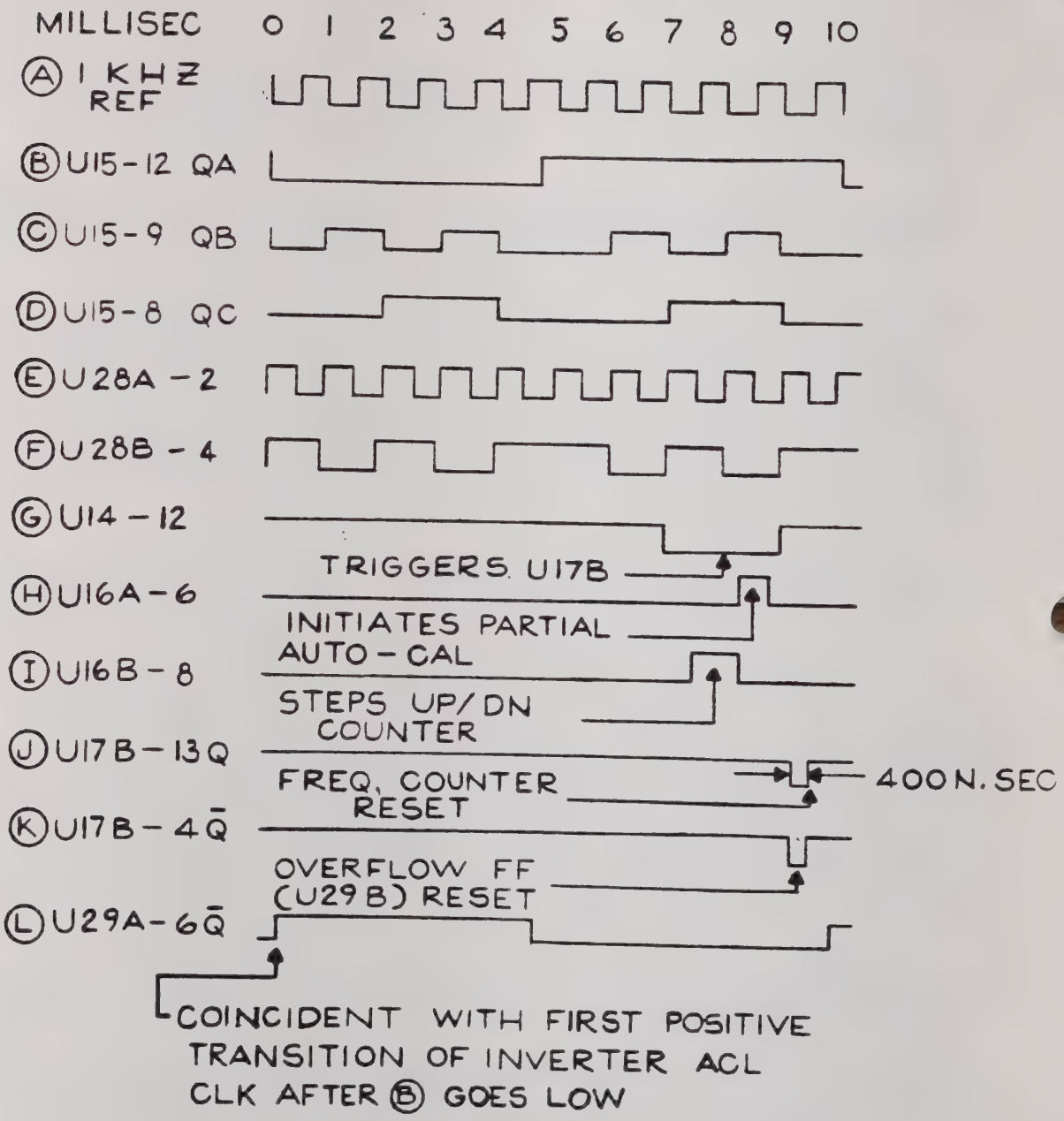


Figure 4-30. Automatic Calibration Section, Typical Waveforms

10-Millisecond Timing Start Circuit. The 10-millisecond timing start circuit includes NAND gate U26C and inverter U25E. When not in AUTO-CAL mode, both inputs to U26C are high and produce a low at U26C-8. This low inhibits the operation of U14C and U16B, both of which are in the timing generator. Thus, the 10-millisecond square wave is not generated within the timing generator. The low output at U26C-8 also is inverted by U25A to a high level which is transferred as EQUAL/RESET. When either full or partial AUTO-CAL mode is initiated, a low level from U25B-4 or U14B-8, respectively, causes a high at U26C-8 which permits the timing generator to provide the 10-millisecond square wave.

400-Nanosecond Generator. The 400-nanosecond generator is single-shot U13A. Normally, the $\overline{Q}$ output is at a high level which does not affect the up/down counter. When full AUTO-CAL mode is initiated, the negative-going leading edge of the two-second pulse from U25B-4 triggers U13A. The resulting negative-going, 400-nanosecond pulse produced at the $\overline{Q}$ output is applied to the load inputs of U20 and U21 of the up/down counters where it presets the counters. The 400-nanosecond generator is used only in the full AUTO-CAL mode; during partial AUTO-CAL mode the counters are updated from the last remaining count of the previous AUTO-CAL cycle.

Frequency Counter. The frequency counter includes count control AND gate U27D, four 4-bit BCD counters, U34 through U37, connected serially, and overflow flip-flop U29B. ACL CLK from countdown section and a 5-millisecond positive pulse from U29A-$\overline{Q}$ are applied to U27D. The output of U27D is applied to the input, pin 14, of the least significant digit of the counter. Each time the input signal (ACL CLK) has a negative transition the counter increases the count by a decimal 1 represented in BCD code at the output lines. At the count of 8 pin 11, 2^3, goes high and remains high for the count of 9. The next input pulse, the 10th, causes the four output lines to go low. The positive-to-negative transition at pin 11 is applied to next most significant counter where the count is increased by a decimal 1. Thus, in this manner the four stage counter can accept 9999 pulses. On the next count, the counter is returned to 0000 and the negative transition at pin 11 of U34, the most significant counter, is applied through inverter U28F and sets the overflow flip-flop U29B. The four output lines of each counter are connected to their associated comparator. The 400-nanosecond reset pulse from the timing generator is applied to pins 2 and 3 of each counter and when this positive pulse is received, all output lines go low.

4-Digit Comparator. The 4-digit comparator includes four 4-bit comparators, U30 through U33, and inverter U28E. Each comparator accepts the four bits of a frequency counter digit at the A inputs and the four bits of a dialed digit from program control at the B inputs. The comparison causes one of three output lines to go high and the other two output lines to go low. If the frequency counter digit is

less than the dialed digit, the A<B output is high. If the frequency counter is larger than the dialed digit, A>B output is high. If both digits are the same, A=B output is high. By cascading each of the first three comparators to its next most significant comparator, the output lines of the most significant comparator, U30, respond in the same manner just described but the comparison considers the four digits of each input as complete numbers rather than individual digits. Thus, when the number in the frequency counter is equal to the dialed bit rate, A=B of U30 is high and A>B is low. The A>B level is inverted by U28E and applied to the up/down counter.

Up/Down Counter Circuit. The up/down counter circuit includes AND gate U27A, U27B, and two inverters U28E and U28D, with two 4-bit up/down counters U20 and U21 connected serially; thus, the maximum count accepted into the counter circuit is 255 (binary 1111 1111). AND gate U27A accepts the OVERFLOW level from the frequency counter and the inverted A>B level from the 4-digit comparator and applies its output to the DOWN/UP input of each counter, U20 and U21. When full or partial AUTO-CAL is initiated, a positive pulse from U16B-8 (see figure 4-30I) will enable U27B to receive A=B positive pulses inverted by U28D. Therefore, the CLK input receives positive transitions. When the level from U27A-3 is low, the counters are incremented by one bit each time the CLK input receives a positive transition; otherwise, the counters are decremented by one bit each time the CLK input receives a positive transition.

When a negative transition is applied to the LOAD input, the levels at the A, B, C and D inputs are preset into each counter and thus appear on the output line at QA, QB, QC and QD, respectively. The most significant bit of the most significant counter (U20-D) is connected to a high level through R83 and the remaining load inputs are connected to ground; therefore, when the negative transition is applied to the LOAD input, at the beginning of the full AUTO-CAL cycle, the counters are preset to 128 (binary 1000 0000), nominally called midscale.

VA DAC. The VA DAC includes eight inverters and a digital-to-analog converter which convert the count in the up/down counter circuit to an analog voltage between 0 and -10 volts. The output of the VA DAC increases or decreases by approximately 0.039 volt as the count to the input is increased or decreased by one bit, respectively. Thus, when the VA DAC receives a full count (all ones), the output is -10 volts; at midscale (a count of 128), the output is -5 volts and when the VA DAC receives no count (all zeros), the output is zero volts.

Timing Generator. The timing generator includes counter U15 which basically is connected as a divide-by-ten counter, NAND gate U14C, 400-nanosecond single-shot U17B, AND gates U16A and U16B, flip-flop U29A, and inverter U25D. The waveforms from each of the previously mentioned elements are shown in figure 4-30. Waveform A is the 1 kHz signal received from the crystal oscillator which is accurate to within ±0.001 percent. From this signal, waveforms B, C, and D are derived and are available at outputs U15-QA, U15-QB and U15-QC, respectively.

During a partial or full AUTO-CAL cycle, the input to U14C-1 and U16B-13 is a high level received from U26C-8 in the 10-millisecond timing start circuit. This high level primes AND gate U14C and U16B and allows the QA, QB and QC outputs from U15 to be gated. U15-9 is inverted by U28B and fed to input U16B-12 (see figure 4-29F). The output of U14C, waveform G, has a positive-going transition occurring 9 milliseconds after the start of the 10-millisecond period. This transition triggers single-shot U17B (see figure 4-30J and K) and resets frequency counter and overflow U29B in preparation for the next 5 milliseconds counting period. R3 and C3 establish the width of the output pulse. The output of U16B (see figure 4-30I) has a positive 1-millisecond pulse occurring 7 milliseconds after the start of the 10-millisecond period. This positive pulse will clock the up/down counter.

Flip-flop U29A is operational only during an AUTO-CAL cycle which is when the PR input is high. If the PR input is low, $\overline{Q}$ output is held low which inhibits U27D. The output from U29A-$\overline{Q}$, during AUTO-CAL mode, is shown in waveform L. The positive portion of this waveform from the flip-flop primes AND gate U27D in the frequency counter and holds the gate open for precisely 5 milliseconds during the ACL CLK counting process. To ensure the gate is opened coincidentally with the start of a clock, so that an accurate count can be obtained, the inverted ACL CLK from U25D clocks U29A and, in effect, causes the flip-flop output signal to be delayed until the start of an ACL CLK pulse.

The 8-Bit DACs. The 8-Bit DAC No. 1 is a digital-to-analog integrated circuit, U11. The four lines identified as MSD 1, MSD 2, MSD 4 and MSD 8 contain the binary coded decimal value of the most significant digit dialed on the bit rate thumbwheels on the front panel (part of program control). The four lines identified as NMSD 1, NMSD 2, NMSD 4 and NMSD 8 contain the binary coded decimal value of the next to the most significant digit dialed on the bit rate thumbwheels. The binary value of each line is applied to its corresponding input of U11. The output of U11 is an analog voltage proportional to the value of the eight input bits. The 8-Bit DAC No. 2, U12, is identical to the 8-Bit DAC No. 1 except the No. 2 DAC processes the two lower order digits of the bit rate thumbwheels.

Combiner. The combiner includes operational amplifier U4 and associated parts. On the ACL005 card, the ouput from U11 is applied to U4 through R6; the output from U12 is applied to U4 through the resistive network including R7, R8, and R10. On the ACL009 card, the output from U11 is applied directly to U4; the output from U12 is applied to U4 through the resistive network including R8 and R10. The resistive network produces a voltage at the input to U4 that is proportional to the total value of the four binary-coded decimal digits. The output of the combiner, Vx, ranges from 0.5 volt, when the significant digits of the bit rate are 1.000, to 5.0 volts, when the significant digits of the bit rate are 9.999. C7 and C8 are bypass capacitors for the +15-volt and -15-volt source lines.

Controlled Gain Amplifier. The controlled gain amplifier includes switch Q1, differential amplifier U3 and buffer Q2. When Q1 is turned off, operational amplifier U3 together with its buffer Q2, operates at unity gain and thus provides an output, VD 1, from the emitter of Q2. This output, like Vx, is between 0.5 and 5 volts. When the two widest bandwidths are used in the tracking loop filter, control level LOOP 3 & 4 goes high and turns Q1 on. Because Q1 is on, R13, in effect, is connected to ground and, because of the relationship between R15 and R13, increases the gain of U3 by 10 percent. Thus, the increased VD 1 improves the jitter response of the bit synchronizer when the wider bandwidths are used. When LOOP 3 & 4 level is low, the junction of CR2 and R11 is approximately 0.7 volt. This voltage prevents current flow through R12, CR3 and CR4. Thus, Q1 is held off. When LOOP 3 & 4 level is high, CR2 is reverse biased and current flow through R12, CR4, CR3 and R11 allows the junction of R12 and CR4 to go positive. The positive base voltage turns Q1 on. C9 operates as a bypass capacitor and C10 operates as a filter capacitor to prevent abrupt changes on VD 1.

Decade Range Splitter. The decade range splitter uses two-input and three-input OR gates and inverters to produce control levels representing segments of the decade range. The true and complement forms of the eight bits representing the two most significant digits are obtained from the input circuit of 8-bit DAC No. 1 and applied to the logic elements where they are combined to provide the control levels indicated in table 4-9. Therefore, a high level D1, D2, D3 or D4 represents its associated segment of decade range and a low level $\overline{D1}$, $\overline{D2}$ or $\overline{D3}$ represents its associated segment of decade range. $\overline{D4}$ could have been provided; however, it is not required.

Table 4-9. Derivation of Decade Control Levels.

DECADE RANGE	CONDITION OF CONTROL LEVELS						
	D1	D2	D3	D4	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$
1.0 to 1.4	L	L	L	H	H	H	H
1.5 to 2.9	L	L	H	L	H	H	L
3.0 to 5.9	L	H	L	L	H	L	H
6.0 to 9.9	H	L	L	L	L	H	H

4.8.10 Countdown Logic and Sync Detector Type CSD002

The type CSD002 card (see schematic drawing 460-1095) contains circuits of the countdown section (see figure 4-18) and circuits of the sync detector section (see figure 4-21). The circuits of the countdown section include the range select prescaler, divide-by-ten divider, decade divider, clock select, divide-by-two and quadrature generator, buffer and multiplexer. The circuits of the sync detector section include main mixer, line drivers, capacitor control circuit, SØ sync matrix, sync switch and sync lamp driver. Each of these circuits is explained in the following paragraphs.

Range Select Prescaler. The range select prescaler includes the VCO amplifier consisting of Q1, Q2, Q3, U23A and associated parts, integrated circuit element U11 which uses 3 stages of a 4-stage counter and integrated circuit U9 which is a 4-input select gate.

VCO and $\overline{\text{VCO}}$ are applied through R17 and R18 to the bases of Q1 and Q2 which are connected as a differential pair. The bases have a dc level of 9.4 volts obtained from Zener diode CR1. Q3 together with its biasing resistors R1 through R4 control the current through the differential pair. Resistors R16, R101, R17 and R18 prevent oscillations from occurring. The output of the differential pair, at the collector of Q2, is applied through U23A which provides TTL levels to drive U9 and U11. IC U11 is a binary counter with the input at pin 8 and outputs at pins 5, 9, and 2. The output at pin 5 is 1/2 the frequency of the input. The output at pin 9 is 1/4 the frequency of the input. The output at pin 2 is 1/8 the frequency of the input. The input frequency (VCO frequency) and the three output frequencies from U11 are applied to the 4-input selection IC U9 where one of the frequencies is selected by D1, D2, D3 or D4, whichever is high. The output of U9 is applied to the divide-by-ten divider and also to the clock select U13.

Divide-by-Ten Divider. The divide-by-ten divider contains four JK flip-flops and AND gate U23C configured so that the Q output of U22A is 1/10th the frequency applied to the clock inputs of U17A, U17B and U22B. The clear input (CL) of each flip-flop is held at a positive voltage applied through R36 from the +5-volt source; thus, the flip-flops are not affected by the clear input. U23B buffers the output from U22A. This output is ACL CLK (auto-cal clock) and is transferred to the automatic-calibration section.

Decade Divider. The decade dividers include five idential ICs, each containing a divide-by-ten divider. The output, pin 12, of the first divider, U12, is applied to the clock select and also to the input, pin 1, of the second divider U18. The output of each succeeding divider, U18, U19, U21, and U20, is applied to the clock select and also to the next lower order divider except for the last divider, U20, which is applied only to the clock select.

Clock Select. The clock select is IC U13 which is a group of selection gates controlled by DEC 1, DEC 2 and DEC 4*. These control levels are decoded to provide enabling signals 0 through 6 which correspond to the bit rate multiplier and select one of the seven inputs 1, 2, 3, 4, 13, 14, or 15, to be transferred to the output, pin 6. The state of the control levels, the decoded value (same as bit rate multiplier) and the selected input are given in table 4-10.

Table 4-10. Clock Select Decode.

STATE OF CONTROL LEVELS			DECODED VALUE	SELECTED INPUT (Pin No.)
DEC 4*	DEC 2	DEC 1		
0	0	0	0	4
0	0	1	1	3
0	1	0	2	2
0	1	1	3	1
1	0	0	4	15
1	0	1	5	14
1	1	0	6	13

Divide-by-Two and Quadrature Generator. The divide-by-two and quadrature generator includes flip-flops U14A and U14B and inverter U10D. The output of clock select is applied to the clock (C) input of U14A which for each positive transition puts a ONE or ZERO into the flip-flop depending on whether the D input is a ONE or ZERO, respectively. The output of this flip-flop is 1/2 the frequency of the clock input; the Q output is Øq and the $\overline{Q}$ output is $\overline{Øq}$. Both outputs are applied to the buffer and the multiplexer. The Q output also is applied to the D input of U14B which is clocked by the complement of the clock to U14A. This complement is obtained from U10D. Thus, the output of U14B is Øn and the $\overline{Q}$ output is $\overline{Øn}$. Both outputs are applied to the buffer and also the multiplexer.

Buffer. The buffer includes four inverters and associated series resistors. The inverters, U10B, U10C, U10E and U10F, provide the complement of its respective input signal. The outputs, respectively, are Øq, $\overline{Øq}$, Øn and $\overline{Øn}$.

Multiplexer. The multiplexer includes two identical multiplexer ICs, U15 and U16 and a differential amplifier composed of Q12, Q13 and associated parts. Each IC contains two sets of selection gates, each set transfers one of four inputs to the output pin depending on the state of the control levels applied to pins 2 and 14. Table 4-11 gives the selected input that is transferred to the output pin for each possible combination of control levels for both sections of each IC.

Table 4-11. Multiplexer Selection Scheme.

CONTROL LEVELS		SELECTED INPUT PIN	OUTPUT PIN
EXT PIN 2	CRZ PIN 14		
	SECTION A OF IC		
H	H	3	7
H	L	4	7
L	H	5	7
L	L	6	7
	SECTION B OF IC		
H	H	13	9
H	L	12	9
L	H	11	9
L	L	10	9

The differential amplifier buffers the Ø2 and Ø4 clocks and applies these outputs as P-CLK and its complement $\overline{\text{P-CLK}}$ to pins 14 and 15 respectively. Resistor R32 and R33 are suppression resistors used to prevent oscillations. Resistor R34 establishes the current through the differential amplifier transistors Q12 and Q13. R19 and R20 prevent excessive collector current.

Main Mixer. The main mixer includes five major functions as follows. A gating circuit including U3B and U6B passes complementary outputs of U when processing NRZ or SØ type PCM or passes Z when processing RZ type PCM. A differential amplifier including Q5 through Q8 and Q14 and Q15 accepts the complementary U or Z pulses, as applicable, and provides single-ended positive pulses to an integrator circuit which basically includes C6. The average voltage across C6 is then applied through two cascaded operational amplifiers U28 and U27. Another gating circuit including U3A and U6C accepts U and CLK when processing NRZ or SØ type PCM or accepts Z and CLK when processing RZ type PCM. When in sync, U or Z, as applicable, is bracketed by negative cycles of CLK; therefore, neither gate is enabled. When an out-of-sync condition occurs, complementary outputs are provided each time the positive cycle of CLK is coincident with the positive U or Z. These complementary outputs are applied to a differential amplifier consisting of Q10, Q11, Q18, Q19, Q21 and Q22. This differential amplifier provides single-ended negative pulses which, like the positive pulses from the other differential amplifier, also are applied to the integrator circuit mentioned previously. Therefore, in-sync, the integrator circuit is charged positively; however, when out-of-sync, the negative pulses overcome the positive pulse and thereby cause a negative charge on the integrator circuit. The voltage across the integrator is applied to two cascaded operational amplifiers U28 and U27 whose outputs are between +10 and -10 volts. If the output voltage is between approximately zero and +10 volts, synchronization is achieved. A non-synchronization condition is achieved when the output voltage is between zero and -10 volts. This voltage is applied to the sync switch.

When processing RZ type PCM, a high CRZ primes AND gate U3C. During normal operation LOSS is low and, when inverted by U8D, also primes U3C. Therefore, the Z output passes through U3C to the inputs of U3B, U6B, U3A and U6C where it is substituted for the U pulses which is held high by the low strobe level applied from U8E to U7. When processing NRZ or SØ type PCM, a low level CRZ inhibits U3C, but the high level output of U3C primes gates U3B, U6B, U3A and U6C. Also the U pulses are received from line receiver U7. The four gates operate in the manner previously described except that the U pulse is substituted for the Z pulse.

The complementary outputs of U3B and U6B are applied through R69 and R70, then developed across R55 and R57. The voltages across these latter resistors are applied through suppression resistors R53 and R56 to the bases of Q14 and Q15. Between pulse times, a high from U3B turns Q14 on and a low from U6B turns Q15 off. Common emitter bias for Q14 and Q15 is established by the conducting transistor causing a voltage drop across R45. When U or Z, as applicable, is applied to the bases of Q14 and Q15, the states of these two transistors change so that Q14 is off and Q15 is on. Collector currents of these two transistors flow through associated 150-ohm resistors, R50 and R51, and then through a common resistor R81. The voltage drop across R81 is relatively constant and, thereby, establishes a positive bias for the bases of Q7 and Q8. Therefore, the voltage variations across R50 and R51 alternately turn Q7 and Q8 on and off. When Q14 is on and Q15 is off, the base voltage of Q7 is less positive than the base voltage of Q8. Therefore transistor Q7 is turned on, Q8 is turned off; and there is no current flowing through C6. During the lower bit rates, the capacitor control circuit parallels C4 and C5 with C6. During pulse time, Q14 is on and Q15 is off causing Q7 to be off and Q8 to be on. Because Q8 is on, the current flowing through Q8 charges C6 positively. Transistor Q6 and its emitter resistor R82 control the amount of charging current. Q6 has a fixed base bias of approximately 4 volts obtained from the divider network composed of R83, and diode-connected Q5 and R86.

When in sync the output of U3A is high and the output of U6C is low. In the manner similar to that described in the preceeding paragraph, the high from U3A holds Q10 off and the low from U6C holds Q11 on. Because Q10 is off and Q11 is on, Q18 is on and Q19 is off. Because Q19 is off, there is no current from the negative source applied to C6. When an out-of-sync condition occurs, that is, the phase of CLK shifts with respect to U or Z pulses as applicable, the resultant complementary pulses from U3A and U6C cause Q10, Q11, Q18 and Q19 to change states. Thus Q19 is on for the width of the pulse and during this time charges C6 negatively.

The voltage across C6 and, when applicable C4 and/or C5, is applied to the non-inverting input of U28 where it is amplified to provide an output within the range of approximately +10 to -10 volts. This voltage is then applied to the inverting input of U27 and the sync lamp driver. Operational amplifier U27 functions as an inverting buffer which drives the sync switch. A slight positive voltage obtained from the junction of R95 and R89 is applied to the non-inverting input of U27.

Line Receivers. Line receivers U4 and U7 are identical dual amplifiers with strobe inputs which, in this application, are used to inhibit the output signal as desired. One set of complementary signals is applied to pins 1 and 2 and another set of complementary signals is applied to pins 11 and 12. A single-ended output from the first set of complememtary signals appears at pin 4 if pin 5 is held high. When the strobe input to pin 5 is low, pin 4 output is held high. A single-ended output from the second set of complementary signals appears at pin 9 if pin 8 (strobe line) is held high. When pin 8 is low, pin 9 is held high. In addition to the strobe input for each line receiver, a low level at pin 6 holds both outputs high. In this application, when loss goes high, it is inverted by U8D and applied as a low level to pin 6 of U4 and U7, and thereby inhibits the four outputs.

The input lines for UR and ZR are terminated in 75 ohm resistors R8, R9, R12 and R13. The input lines for SD-CLK and SD-BD also are terminated in 75 ohm resistors R10, R11, R14 and R15; however, each pair of these resistors is returned to an individual source of -1.4 volts. One source includes R111, CR14 and CR15 and the other source includes R112, CR16 and CR17. The V_{CC} voltage, +5 volts, is applied to pin 14. The V_{ee} voltage, approximately -5.3 volts, is obtained from the network including Q25 and resistors R102 through R105.

Capacitor Control Circuit. The capacitor control circuit includes logic elements U5A, U8C and U8B, control transistors Q4 and Q9 and FETs Q23 and Q24. The purpose of this circuit is to provide a smaller total capacitance in the integrator circuit of the main mixer as the bit rate is increased. Basically, capacitors C4 and C5 are operational in the main mixer circuit only when FETs Q23 and Q24, respectively, are turned on and provide low impedance paths to ground for their respective capacitors; otherwise, the capacitor return paths are open. Each FET is turned on when the emitter voltage of its associated control transistor is the relatively low voltage obtained when the control transistor is on. When the control transistor is off, approximately -15 volts from the emitter turns off the FET. Table 4-12 gives the signal levels at significant locations, conduction states of the FETs, and the total capacitance included in the mixer circuit for each decade of bit rate.

Table 4-12. Capacitor Control Selection

BIT RATE	CONTROL LEVELS DEC 4	CONTROL LEVELS DEC 2	OUTPUT OF U5A	INPUT TO BASE OF Q4	FET Q24	FET Q23	TOTAL CAPACITANCE C4, C5, C6 (uf)
10^0	0	0	L	L	ON	ON	111
10^1	0	0	L	L	ON	ON	111
10^2	0	1	H	L	OFF	ON	11
10^3	0	1	H	L	OFF	ON	11
10^4	1	0	H	H	OFF	OFF	1
10^5	1	0	H	H	OFF	OFF	1
10^6	1	1	H	H	OFF	OFF	1

SØ Sync Matrix. The SØ sync matrix is enabled only when CSØ is high. This high level primes AND gates U6A, U5D and U5. The absence of LOSS also primes U6A. The third input to U6A is connected to a source of +5 volts through R109. Thus, with 3 high inputs to U6A, the high output primes U5C which allows $\overline{Z}$ to be applied through U5C to become Z, and then applied to U2A and U2B. $\overline{Z}$ also is applied directly to U2C and U1A. $\overline{BD}$ is applied through primed gate U5D to become BD and is then applied to U2A and U2C. $\overline{BD}$ also is applied directly to U2B and U1A. $\overline{CLK}$ is applied to gates U2C and U2B; it also passes through primed gate U5 to become CLK and is then applied to gates U2A and U1A. Thus, gates U2A, U2B, U2C and U1A monitor the phase relationships of Z, BD and CLK. The outputs of these four gates are combined in U1B; its output is developed across R94.

The output voltage across R94 is a high level when data and clock are in sync and the input data are all ONEs; it is a low level when data and clock are in sync and the input data are all ZEROs. This voltage is integrated by R93 and C7 and, for the conditions just given, the voltage across C7 is 5 volts or zero volts, respectively. During this time U is not present because the data is consistently ONEs or ZEROs and the main mixer detects this situation as an out-of-sync condition; however, when the voltage across C7 is relatively high (above approximately 2.8 volts) or is relatively low (below approximately 1.2 volts), operational amplifier U26 or U25 detects this situation and provides an in-sync signal which is ORed with the signal from the main mixer to provide an output SYNC signal. As changes occur in the SØ data, the high and low pulses from U1B are averaged across C7; thus, when an occasional ZERO occurs among mostly ONEs, the voltage across C7 decreases from 5 volts and when an occasional ONE occurs among mostly ZEROs, the voltage across C7 increases from zero volts. Also each time the data changes U is generated. Therefore, when SØ data and clock are synchronized and the SØ data is changing between ONEs and ZEROs, the main mixer provides the SYNC signal and when the SØ data contains mostly ONEs or mostly ZEROs, the SØ sync matrix provides the SYNC signal. If SØ data and clock are not synchronized both circuits provide an out-of-sync signal. When out-of-sync, the output of U1B is random pulses which provide an average voltage between 1.2 and 2.8 volts across C7.

The voltage across C7 is applied to the non-inverting input of U24 which is operating as a buffer. The voltage divider consisting of R98, R99 and R100 provides approximately 1.2 volts for the inverting input of U25 and approximately 2.8 volts for the non-inverting input of U26. The output of U24 is applied to the remaining inputs of U25 and U26. When the output of U24 is above 2.8 volts, the output of U26 is a negative voltage which causes CR10 to conduct and thereby causes the sync switch to generate SYNC. When the output of U24 is below 1.2 volts, the output of U25 is a negative voltage which causes CR11 to conduct and thereby causes the sync switch to generate SYNC. When the output of U24 is between 1.2 and 2.8 volts the outputs of U25 and U26 are positive voltages which reverse bias their associated diodes.

SYNC Switch. The sync switch includes switch Q20, inverter U8A, three input diodes forming a negative input OR gate and associated parts. When the inputs to CR8, CR10 and CR11 are high, the diodes are reversed biased by the approximate 3.5 volts obtained from the junction of R39 and R97. Also the approximate 0.7 volt developed across CR7 holds Q20 on and thus pulls the output SYNC line, pin 27, to ground. This low level is inverted by U8A whose output is a high level $\overline{\text{SYNC}}$ at pin 28. The output of U8A also is applied to the sync lamp driver. When the input to CR8, CR10 or CR11 is low, the junction of R39 and R97 also is low. This low level turns Q20 off and thus provides a high level through R40 to pin 27. This high is inverted by U8A and thus provides a low level to pin 28.

Sync Lamp Driver. The sync lamp driver includes inverter U8F and switch Q17 and their associated parts. This portion of the driver provides or does not provide the ground return circuit for the SYNC lamp during a sync condition or non-sync condition, respectively. The sync lamp driver also includes Q16, Zener diode CR13 and associated parts. This portion of the driver functions as a dimmer. Therefore, to light the SYNC lamp, a low level must be applied to U8F, whose output, a high, is applied to the base of Q17 and turns Q17 on to provide the ground return. When the +15 volt source is applied through R88, SYNC lamp, connected between pins 37 and 40, lights dimly. When Q16 is turned on, the source voltage is applied through parallel resistors R87 and R88 and thus causes SYNC lamp to light at full brilliance. Q16 is turned on only when the output of U28 exceeds approximately 5 volts which indicates a high degree of synchronization. Diode CR4 and Zener diode CR13 establish the threshold voltage that will turn Q16 on. Diode CR5 prevents Q16 from going too far into cutoff during an out-of-sync condition.

4.8.11 Phase Detector Type PDT020

The type PDT020 card (see schematic drawing 460-1058) contains circuits of the phase detector section (see figure 4-14) and includes the following: BD, U, Z, Øn and Øq line receivers, bit detector, SD-BD line

driver, primary phase detector, Δ current generator, loop bandwidth tracking control circuit, frequency range decoder, SØ adjunctive phase detector, SØ adjunctive Δ current generator, routing switch, SD-CLK line driver and -5 volt source. Each of these circuits is explained in the following paragraphs.

The BD Line Receiver. The BD line receiver includes differential amplifier composed of Q2 and Q3, current control transistor Q1 and associated parts. The base voltage of Q1 is held at approximately +12 volts by a voltage divider composed of R2 and R4. This voltage is applied to the base through R3, an oscillation suppressor resistor. Emitter resistor R1 establishes the proper emitter voltage for conduction through Q1. Zener diode CR1 provides approximately 10 volts through R5 and R8 to the collector circuits of the differential driver circuit located on the threshold detector card. Thus R5 and R8 function as collector load resistors for the driver circuit. C1 is a bypass capacitor.

The BD signal and its complement are applied through R6 and R7 to the bases of the differential amplifier; therefore, the transistors alternately turn on and off. The BD signal is developed across collector load resistor R10 from where it is applied to the bit detector. Resistor R11, which is returned to -15 volts, is included to ensure that the BD output goes to a low level (just below zero volts) when Q3 is turned off. R9 is the collector load resistor for Q2.

The U Line Receiver. The U line receiver is practically identical to the BD line receiver described in the preceding paragraph. The only difference is in the collector circuits of the differential amplifier composed of Q28 and Q29. The output of each transistor is developed across two series connected resistors. The total voltage developed across both resistors is the U and $\overline{U}$ signals. The voltages developed across R109 and R108 are the UR and $\overline{UR}$ signal.

The Z Line Receiver. The Z line receiver is identical to the U line receiver described in the preceding paragraph. The Z output signal is developed across the series connected resistors R42 and R44; the $\overline{Z}$ which otherwise would be developed across R41 and R43 is not required. ZR and $\overline{ZR}$ are developed across R44 and R43, respectively.

The Øn Line Receiver. The Øn line receiver is integrated circuit (IC) U8 and associated parts. The differential input is applied to pins 1 and 2. The differential output is obtained from pins 4 and 9. Bias voltages are applied to the remaining pins for the proper operation of the IC.

The Øq Line Receiver. The Øq line receiver is integrated circuit (IC) U9 and associated parts. The differential input is applied to pins 1 and 2. The differential output is obtained from pins 4 and 9. Bias voltages are applied to the remaining pins for the proper operation of the IC.

Bit Detector. The bit detector includes clock selection logic elements U1D and U2, BD flip-flop U4B, Z flip-flop U4A, output signal selection NOR gates U5A and U5B and logic elements U3A, U1A and U1B. The circuit is controlled by control levels CRZ and EXT. When processing RZ type PCM signals, CRZ is high. The low level from U1A inhibits BD flip-flop U4B because the low levels at the P and R inputs hold the Q and $\overline{Q}$ outputs high; this configuration of the Q and $\overline{Q}$ outputs is non-stable, that is, it will not persist when the P and R inputs return to their inactive level. The resultant high level at the output of U1B does not affect the Z flip-flop U4A, this allows the C input to clock the D input through to the outputs of the flip-flop. The D input is the Z pulse. The C input is obtained from U2F and depends on whether or not external clock is used. If external clock is used, EXT is high and primes U2A which passes $\overline{Øq}$ through U2A and U2F to the C input of U4A. If external clock is not used, EXT is low. EXT is inverted by U1D and primes U2B which passes $\overline{Øn}$ through U2B and U2F to the C input of U4A. Thus, the selected clock strobes the Z pulses to the outputs of U4A with the true pulse at the Q output and the complement pulse at the $\overline{Q}$ output. The true output is applied through NOR gate U5B and the complement output. These pulses are inverted in U5A and U5B, then applied through R15 and R18 to become BD-NRZ and $\overline{\text{BD-NRZ}}$. The output of the bit detector is PCM data in NRZ form regardless of the PCM form applied to the bit detector.

When processing NRZ, DM or SØ type PCM signals, CRZ is low. The low level from U1B inhibits Z flip-flop U4A because the low levels at the P and R inputs hold the Q and $\overline{Q}$ outputs high. The high level at the output of U1A does not affect the BD flip-flop U4B; the C input is thus allowed to clock the D input through to the outputs of the flip-flop. The D input is the BD pulse. The C input is obtained from U2E and depends on whether or not external clock is used. If external clock is used, EXT is high and primes U2C which passes $\overline{Øq}$ through U2C and U2E to the C input of U4B. If external clock is not used EXT is low. EXT is inverted by U1D and primes U2D which passes $\overline{Øn}$ through U2D and U2E to the C input of U4B. Thus, the selected clock strobes the BD pulses to the output of U4B with the true pulse at the Q output and the complement pulse at the $\overline{Q}$ output. The true output is applied through NOR gate U5B and the complement output is applied through U5A. These pulses, inverted in U5A and U5B, are applied through R15 and R18 to become BD-NRZ and $\overline{\text{BD-NRZ}}$.

In summation, the bit detector provides PCM in NRZ code regardless of the type of PCM being processed. Either BD or Z pulses will be processed. The BD pulses are processed through the upper half of U2 and the BD flip-flop; the Z pulses are processed through the lower half of U2 and the Z flip-flop. The outputs of the active flip-flop are applied through NOR gates U5A and U5B to the BD-NRZ and $\overline{\text{BD-NRZ}}$ output pins and also to the inputs of the SD-BD line driver.

The SD-BD Line Driver. The SD-BD line driver includes a differential amplifier consisting of Q4 and Q5 and associated parts. The input signals, BD-NRZ and $\overline{\text{BD-NRZ}}$ are applied through R13 and R17 to the bases of Q4 and Q5, respectively. These input signals alternately turn the two transistors on and off. The output signals, $\overline{\text{SD-BD}}$ and SD-BD, are developed across their respective collector load resistors. R12 and R16 are part of the collector load for its associated transistor; the remaining parts of the collector load are included in the companion line receiver circuit on the countdown and sync detector card. The common emitter circuit is retained to +15 volts through R14.

Primary Phase Detector. The primary phase detector has two portions; one portion, Q30 through Q34, processes the $\overline{U}$ pulse and Øn and the other portion, Q45 through Q48, processes the U pulse and Øn. The first portion NANDs the $\overline{U}$ pulse and Øn to form the X pulse. The other portion ANDs the U pulse and Øn to form the Y pulse. The U pulse is in phase with the generated clock when the transition of Øn occurs in the middle of the U pulse. If the frequency of the clock is other than that of the incoming PCM, the transitions of Øn occur before or after the center of the U pulse. Therefore, when the frequency and phase of the generated clock are correct, the X and Y pulses have equal widths. Otherwise, one of the pulses X or Y is wider than the normal width (1/2 width of U pulse) and the other is narrower than the normal width.

The NAND function is performed by transistors Q30 through Q34 and associated parts. Øn from the Øn line receiver is applied through R110 to the base of Q30 which is one input to the NAND function. When Øn is high, Q30 is turned on and causes a voltage drop across R114 and a high level at the emitters of Q31 and Q32. This high level holds Q32 off. Q31 can be on or off depending on its base voltage; however, because Q30 is on, the Q31 collector voltage (common with Q30 collector voltage) remains at a low level. The collector voltage of Q32 is high. These differential signals are applied to the differential amplifier formed by Q33 and Q34 and causes Q33 to be off and Q34 to be on. The resultant low level at the collector of Q34 (the X signal) is applied to the X switch circuit. Its companion differential signal, $\overline{X}$, from the collector of Q33, a high level, also is applied to the X switch. The circuit remains in this condition until Øn goes low and turns Q30 off. Because Q30 is off, the differential pair, Q31 and Q32, operates in a conventional manner and causes Q34 to go off when $\overline{U}$ pulse is low. When Q34 goes off, a high level X pulse from the collector of Q34 and a low level $\overline{X}$ pulse from the collector of Q33 are applied to the X switch.

The AND function is performed by transistors Q45 through Q48 and associated parts. Øn from the Øn line receiver is applied through R178 to the base of Q45 and U pulse from the U line receiver is applied through R179 to the base of Q46. When either of these inputs are low its associated transistor is turned on. The current flow through R181 and

CR24 causes the common emitter voltage to be one diode drop (approximately 0.7 volt) above the lower base voltage. Because at least one of the inputs is near ground, the common emitter voltage is approximately +0.7 volt. This low level is applied through R182 to the base of Q47 which together with Q48 forms a differential amplifier. Because the base of Q48 is clamped at approximately 3 volts by the voltage divider network composed of R184 and R187, the low level applied to the base of Q47, turns Q47 on and Q48 off. Therefore, the collector voltage of Q47, the $\overline{Y}$ signal, is a high level and the collector voltage of Q48, the Y signal, is a low level. The circuit remains in this condition until both inputs are high, which causes the common emitter voltage to be one diode drop above the lower base voltage. The lower base voltage is in excess of +3.5 volts; therefore, the common emitter voltage is in the vicinity of 4.2 volts. This high level holds Q47 off and allows Q48 to conduct. Therefore, the collector voltage of Q47, the $\overline{Y}$ signal, is a low level and the collector voltage of Q48, the Y signal, is a high level.

Capacitors C29 and C30 bypass to ground any signal currents on the +15 volt lines. Resistor R183 is the common emitter resistor for the differential amplifier composed of Q47 and Q48. Diode CR24 is included to establish the proper voltage level at the base of Q47. R182 is included to prevent oscillation. R185 and R186 are the collector load resistors for Q47 and Q48, respectively. R177 and R180 limit the current through Q45 and Q46, respectively.

The Δ Current Generator. The Δ current generator includes three current adjust circuits, the X switch and the Y switch. The No. 1 current adjust circuit includes Q20, Q21A, Q21B and associated parts. The No. 2 current adjust circuit includes Q18, Q19A, Q19B and associated parts. The No. 3 current adjust circuit includes Q16, Q17A, Q17B and associated parts. The X switch is a differential amplifier composed of Q22, Q23 and associated parts. The Y switch, is a differential amplifier composed of U15Q1, U15Q2 and associated parts. The three current adjust circuits are identical except for the emitter resistors R67 and R68 which have greater ohmic value than their counterparts. The increased resistance allows circuit No. 2 to operate with less current.

Only one current adjust circuit is enabled at any one time. No. 1 is enabled by level C when the bit rate is between 1.000×10^0 and 1.499×10^6 bps. No. 2 is enabled by level B when the bit rate is between 1.500×10^6 and 2.999×10^6 bps. No. 3 is enabled by level A when the bit rate is between 3.000×10^6 and 5.000×10^6 bps. Because the three circuits are identical only No. 3 is explained.

Transistor Q16 functions as a switch. A high control level applied through R58 holds Q16 off and thus inhibits any current flow through Q17A and Q17B. A low control level applied through R58 turns Q16 on to enable the circuit. Q17A, Q17B and associated parts form a current mirror. The current flowing through Q17B is the output current from the loop bandwidth tracking control which provides a current whose value is related to the operating bit rate. Because Q17A and Q17B form a current mirror the current flowing through Q17A is identical to that flowing through Q17B. Diodes CR4 and CR5 establish a larger base-collector voltage for improved control of the current in the slave leg (Q17) of the mirror circuit. Potentiometer R60 compensates for any unbalance between R62 and R63.

The current flowing through Q17A also flows through the X switch to either ground or the ΔI line. The complete circuit for the current in the ΔI line is through the routing switch and the input circuit of the applicable tracking loop filter. Because this current flows to +15 volts from the tracking loop filter, it is called the up current. A down current supplied and controlled by the loop bandwidth tracking control circuit has the same value as the up current and flows through the Y switch to ground from the ΔI line.

The X switch accepts X and $\overline{X}$ from the primary phase detector. During X time, the low level at the base of Q23 turns Q23 on and thus allows the up current to flow for the duration of the X pulse. Immediately before or immediately after the X pulse, depending on whether the U transistion was positive or negative, the Y pulse causes a high level at the base of U15Q1 and turns U15Q1 on. This allows the down current to flow for the duration of the Y pulse. When the X and Y pulses have the same width, the up and down currents are equal and opposite, therefore, no correction signal ΔI is generated. When the pulse widths are not the same, the up or down current predominates and thus establishes a correction signal which causes an appropriate correction in the generated clock frequency.

When Q23 of the X switch is turned off, Q22 is turned on and directs the up current through R79 and R78 to ground. The bases of Q22 and Q23 have a fixed base bias of +10.7 volts obtained from the junction of Zener diode CR3 and R61. This bias is applied through suppressor resistors R75 and R76 to their respective bases. When U15Q1 of the Y switch is turned off, U15Q2 is turned on and directs the down current through R96, R95 and R94 to the +15 source. The junction of R94 and R95 is clamped to +6.2 volts by Zener diode CR12. Resistors R125 and R128 are suppressors.

Loop Bandwidth Tracking Control Circuit. The loop bandwidth tracking control circuit controls the amount of current flowing through the X switch, the Y switch, the SØ-X switch and the SØ-Y switch. The overall function of the circuit is to provide equal currents through matched transistors U15Q3 and U15Q4 and also to provide equal currents

through matched transistors U16Q3 and U16Q4. The currents through U16Q3 and U16Q4 are one-half the value of the currents through U15Q3 and U15Q4. The value of the currents is dependent on the VD1-ΔI signal which is the signal applied to the bases of both sets of matched transistors.

Signal VD1-ΔI is derived in the circuit composed of operational amplifiers U13 and U14, buffer Q26, switches Q24 and Q25 and associated parts. The purpose of the circuit is to change VD1-ΔI when the bit rate is changed and also to double VD1-ΔI if loop bandwidth 4, the widest bandwidth, rather than bandwidths 1, 2 or 3, is used to process the correction signals from the primary phase detector and the SØ adjunctive phase detector.

When LBW4 is high, bandwidth 4 is being used, Q24 is turned on and, because of the voltage drop across R82, has a high voltage level at its emitter. This high level is applied through R83 to the base of Q25 and turns Q25 on, which in effect connects R86 to ground and causes operational amplifier U13 to have a gain of 2. When LBW4 is low, Q24 and Q25 are turned off. Diode CR11 limits the negative base voltage of Q25 to -0.7 volt. Because Q25 is off, operational amplifier U13 has a gain of unity.

For bit rates below 10^4 bps, a fixed voltage of approximately 0.5 volt obtained from the voltage divider consisting of R84, R87 and R88, is applied through R85 to the non-inverting input of operational amplifier U13. The output of U13 is applied to the non-inverting input of operational amplifier U14 where it is compared to a voltage level obtained from the emitter of U15Q4. Both inputs to U14 are approximately -7.5 volts and the output is the amplified difference which is applied through R92, emitter follower Q26, and R126 to the base of U15Q4 and thus controls the current through U15Q4 as well as the current through U15Q3, U16Q3 and U16Q4. Because the U15Q4 emitter voltage is applied to the U14 inverting input, this feedback circuit functions like a servo system to stabilize the value of VD1-ΔI. When the bit rate is 10^4 bps or greater, DEC 4* is high. The high level is inverted by U12C. The resultant low level from U12C energizes relay K1. The closed contact of K1 applies VD1 through R85 to the U13 non-inverting input where it is added to the fixed bias.

The current flowing through U15Q3 is the current flowing through either U15Q1 or U15Q2 depending on whether Y is high or low respectively. The current flowing through U15Q4 is the current which flows through the master leg of current mirror transistor Q17B, Q19B or Q21B, whichever is enabled; it is then reflected through Q17A, Q19A, or Q21A, whichever is enabled, to one or the other of the transistors of the X switch (Q22 and Q23). The currents flowing through U16Q3 and U16Q4 are similarly distributed to transistors Q41 and Q42 of the SØ-X switch and transistors U16Q1 and U16Q2 of the SØ-Y switch.

Frequency Range Decoder. The frequency range decoder decodes levels DEC 4*, DEC 2, D4 and D3 to provide three levels identified as A, B and C. Level A is low only when the bit rate is between 3 and 5 MHz. Level B is low only when the bit rate is between 1.50 and 2.999 MHz. Level C is low only when the bit rate is between 1 Hz and 1.499 MHz. Level A, B or C, when low, turns on its associated current range select circuit in the primary phase detector and an identical current range select circuit in the SØ adjunctive phase detector. The decoding is performed by NAND gates U11A and U11B, NOR gates U10A, U10B, U10C, and U10D and inverters U12D, U12E and U12F.

The SØ Adjunctive Phase Detector. The SØ adjunctive phase detector is operational only when CSØ is high; thus, the detector is operational only when processing SØ type PCM signals. This detector, which includes flip-flops U6A, U6B, U7A and U7B and NOR gates U3B, U5C and U5D, compares the transitions of clock with the Z pulse. The generated clock is in phase with the Z pulse when the transitions of Øn occur in the middle of the Z pulse. If the frequency of the clock is other than that of the incoming PCM, the transitions of Øn occur before or after the center of the Z pulse. Therefore, when the frequency and phase of the generated clock are correct, the SØ-X and SØ-Y pulses have equal width; otherwise, one of the pulses, SØ-X or SØ-Y, is wider than the normal width (1/2 width of Z pulse) and the other is narrower than normal width.

When CSØ is high, a ONE is clocked into U6A and U7A for each positive transition of the Z pulse. The contents of U6A and U7A are transferred to U6B and U7B by the positive going transitions of $\overline{Øn}$ and Øn, respectively. The $\overline{Q}$ outputs of the four flip-flops are ORed in U5D, U5C and U3B to provide outputs of SØ-X, SØ-Y and SØ-$\overline{Y}$, respectively.

SØ Adjunctive Δ Current Generator. The SO adjunctive Δ current generator includes three current adjust circuits, the SØ-X switch and the SØ-Y switch. The No. 1 current adjust circuit includes Q35, Q36A, Q36B, and associated parts. The No. 2 current adjust circuit includes Q37, Q38A, Q38B and associated parts. The No. 3 current adjust circuit includes Q39, Q40A, Q40B and associated parts. The SØ-X switch is a differential amplifier composed of Q41, Q42 and associated parts and a differential driver composed of Q43, Q44 and associated parts. The SØ-Y switch is a differential amplifier composed of U16Q1, U16Q2 and associated parts. The three current range select circuits are identical to each other and also identical to the current range select circuits that are part of the phase detector explained previously.

The SØ-X switch is practically identical to the X switch of the primary phase detector explained previously. The difference is that the SØ-X switch uses a differential buffer (Q43 and Q44) to convert the single-ended SØ-X signal to differential signals. Q44 base voltage is fixed at approximately +1.5 volts. Therefore, when SØ-X exceeds 1.5 volts, Q43 turns on and forces Q44 off, and when SØ-X is less than 1.5 volts, Q43 is cut off and allows Q44 to conduct. Thus, the differential signals developed in the collector circuit are applied to the differential amplifier Q41 and Q42. Capacitors C26 and C27 bypass to ground

any signal currents on the -15 volt line. The SØ-Y switch is identical to the Y switch which is part of the SØ adjunctive phase detector explained earlier.

Routing Switch. The routing switch essentially is two relays, K2 and K3, that direct the ΔI signal to the high frequency or low frequency tracking filter. Relay K2 directs ΔI signal, as HF-IØ, when DEC4 is low, that is, when the bit synchronizer is processing PCM signals with a bit rate of 10^4 bps or greater. Relay K3 directs ΔI signal, as LF-IØ, when DEC 4* is low. DEC 4* is inverted twice by U12A and U12B before being applied to the coil of K3. Thus, when DEC 4* is low, the bit synchronizer is processing PCM signals with a bit rate less than 10^4 bps. Diodes CR21 and CR22 dampen the reverse voltage generated when the relays are deenergized. Resistor R188 is a pull-up resistor for U12A.

The SD-CLK Line Driver. The SD-CLK line driver is a differential amplifier composed of Q13, Q14 and associated parts. Operation of this line driver is identical to the SD-BD line driver explained earlier.

The -5-Volt Source. The -5-volt source uses Q15 and R57 to drop 10 volts from the -15 volt source. Conduction, and thus the voltage drop across Q15, is controlled by the fixed base bias established by the voltage divider consisting of R51 and R56. C4 is a bypass capacitor for the -5 volt source.

4.8.12 High Frequency Tracking Loop Filter Type HLF001

The type HLF001 card (see schematic drawing 460-1065) contains circuits of the high frequency tracking loop filter section (see figure 4-15) and includes the following: loop bandwidth decoder, decade decoder, loop filter, HF-IØ buffer, feedback network, HF/LF select circuit, meter driver, reset switch and +5.5 volt reference generator. This card also contains the EQUAL LT and LOSS LT buffers both of which are part of program and operational status displays. Each of these circuits is explained in the following paragraphs.

Loop Bandwidth (LBW) Decoder. The loop bandwidth decoder includes NAND gates U9A, U9B, U9D, NOR gate U9C and inverters U10A, U10C and U10F. These elements convert input levels of LBW 4, LBW 2 and LBW 1 which represent the binary coded value for the position of the LOOP BAND switch to output levels of LOOP 2 and LOOP 3 &4. The complements of these two signals are also provided. The relationships among the selected loop band, the input control levels and the output control levels are given in table 4-13.

Table 4-13. Loop Bandwidth Decoder Truth Table.

SELECTED LOOP BAND	CONTROL LEVELS			OUTPUT LEVELS	
	LBW 4	LBW 2	LBW 1	LOOP 2	LOOP 3 & 4
1	0	0	1	0	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	0	1

Decade Decoder. The decade decoder includes integrated circuits U11 and U12. U11 is a 4-bit full adder; however, not all inputs are used; instead, they are connected to ground. This element adds the value of DEC 4*, DEC 2 and DEC 1 which are applied to the A inputs, to the value of LOOP 3 & 4 and LOOP 2 which are applied to the B inputs. The sum of these two quantities is a BCD value appearing at pins 15, 2, 6 and 9; having a decimal value between 4 and 7. The output is equal to 4 when LOOP BAND switch is at position 1 and the bit rate multiplier is 10^4 (the lowest bit rate when processing high frequency PCM signals) and is equal to 7 when LOOP BAND switch is at position 3 or 4 and the bit rate multiplier is 10^6. The BCD code for 4, 5, 6 or 7 is applied to U12 which is a BCD-to-decimal converter and causes one of the output lines, pins 5, 6, 7 or 9, to go low. Each output line is applied through a non-inverting amplifier to an associated relay coil. These relays K5 through K8 are also identified as 4, 5, 6 and 7, respectively. The conditions that energize each relay is given by:

$\Sigma = N + (L-1)$; where

Σ = number of energized relay

N = exponent of bit rate multiplier

L = position of LOOP BAND switch.

As an example, a bit rate multiplier of 10^5 with the LOOP BAND switch in position 2 would give:

$\Sigma = 5 + (2-1)$

$\Sigma = 5 + 1$

$\Sigma = 6$

Therefore: K7, which is identified as $\Sigma 6$, would be energized.

Loop Filter. The loop filter includes all parts that comprise a variable RC network that affects the HF-I/O signal at the junction of R6 and R7 before the signal is applied to the HF-I/O buffer. In simplified form, the RC network includes, from the junction of R6 and R7, a main capacitor connected in series with a bump capacitor to ground. A variable impedance provided by Q10 is in parallel with the bump capacitor. The total value of the main capacitor is the value of C35 and the value of C24 and C25, C31 or C34, whichever is connected in parallel wth C35 by the associated summing relay. The value of the

bump capacitor is the value of C23, C26, C29 or C32 whichever is connected to ground by the associated summing relay. The impedance of Q10 is controlled by the current flow through Q8 and the resultant voltage drop across R50 which is the base voltage of Q10.

The signal current developed across the bump capacitor tends to increase as the bit rate increases. To compensate, the resistance between pin 1 and 6 of Z2 decreases as VD1 increases. Thus, the signal current through Q8 and the voltage across R50 also increases which, in turn, increases current flow through Q10 and decreases the impedance across Q10. Because the impedance of Q10 is changed, the frequency response of the filter is changed, and thus provides the proper characteristics within each decade. In addition, the base voltage of Q10 is changed by shunting R50 with a series circuit consisting of parallel-connected capacitors C13-C14 and R53 when LOOP 2 is selected; and by shunting R50 with the two parallel-connected capacitors when LOOP 3 & 4 are selected. Thus, the characteristics of the loop filter are changed between decades by proper selection of main and bump capacitors and are changed within the decade by VD1 which changes the shunt impedance. The shunt impedance also is affected by the selected loop bandwidth.

VD1 is applied to a series circuit consisting of R37 and the resistive element between pins 3 and 4 of Z2; pin 4 of Z2 is connected to a constant source of -1 volt obtained from U8 and its associated parts. As VD1 is increased from 0.5 to 5 volts, the input to U6 is changed to provide a linear relationship between the resistive elements of Z2 and VD1. The non-inverting input to U6 is connected to ground; therefore, as VD1 increases, the output of U6 increases negatively which increases the conduction through Q7 and the bulb element of Z2. The increasing brillance of the bulb decreases the resistance across the resistive elements until the junction of R37 and pin 3 of Z2 is equal to 0 volts, at which time the circuit stabilizes until VD1 is again changed. Thus, when VD1 is 0.5 volt, the resistance of each of the Z2 resistive elements is 6k ohms and when VD1 is 5 volts, the resistance of each of the Z2 resistive elements is 600 ohms.

HF-IØ Buffer. The HF-IØ buffer consists of operational amplifier U1 and the resistive element between pins 1 and 6 of Raysistor element Z1. The non-inverting input accepts the HF-IØ signal which varies about a dc reference of 5.5 volts. It also accepts a small amount of feedback current through R10. The amount of feedback current is controlled by the output signal from U1 and the resistance value between pins 1 and 6 of Z1 which, in turn, is controlled by the feedback network. The output of the buffer, which has unity gain, is developed across R12 and then applied to the HF/LF select circuit.

Feedback Network. The feedback network includes operational amplifier U5, lamp driver Q6, Raysistor Z1, operational amplifier U2 and associated parts. VD1 is applied to a series circuit consisting of R32 and the resistive element between pins 3 and 4 of Z1. The junction of these resistances is connected to the inverting input of U5. The non-inverting input to U5 is referenced to 0.5 volt obtained from the junction of R33 and R34. Therefore, as VD1, which is between 0.5 and 5 volts, increases above 0.5 volt, the output of U5 increases negatively which increases the conduction through Q6 and the bulb element of Z1. The increasing brilliance of the bulb decreases the resistance of the resistive elements of Z1 until the voltage at the junction of R32 and pin 4 is equal to the voltage applied to the non-inverting input of U5, at which time the circuit stabilizes until VD1 is again changed. When VD1 is at 0.5 volt, the resistive elements have 5k ohms and when VD1 is at 5 volts, the resistive elements have 500 ohms.

The output signal from buffer U1, which tends to increase as the bit rate is increased, is applied through the variable resistive element between pins 6 and 1 of Z1 to the inverting input of operational amplifier U2. The positive input of this amplifier is referenced to +5.5 volts which also is the dc level at the output of U1. Therefore, the input signal to U2, and thus the feedback voltage from the output of U2, tends to remain constant at 5.5 volts and thus holds the input of U1 constant as the bit rate is changed.

HF/LF Select Circuit. The HF/LF select circuit includes HF relay K1, LF relay K2, a differential amplifier consisting of Q4A and Q4B, current control transistors Q5A and Q5B, inverters U10E and U10D and associated parts. DEC 4* is applied to the two series connected inverters to provide true and complement levels which are applied to the coils of relays K1 and K2. The polarities are such to energize only K1 when processing high frequency PCM signals and to energize only K2 when processing low frequency PCM signals. The selected signal is applied through the contacts of its associated relay to the differential amplifier and also through R14 to the meter driver.

The selected signal is also applied through R23 to the base of Q4A. The other input to the differential amplifier, at the base of Q4B, is referenced to +5.5 volts through R26. The complementary output signals, -VCOΔI are developed in the collector circuits of Q4A and Q4B. The emitter resistors of Q4A and Q4B, R27 and R28, are returned to +15 volts through the current controlled transistor Q5A and R29. Diode-connected transistor Q5B, R30 and R31 form a voltage divider to provide the proper base bias for Q5A.

Meter Driver. The meter driver includes operational amplifier U3 and U4 and associated parts. The inverting input of U3 is operated at zero volts dc because +5.5 volts is applied from the output of U1 through R14 to the input and -5.5 volts is applied from the output of

U4 to the input through R18. Both resistors, R14 and R18, are of equal value. Potentiometer R20, which controls the output of U4, compensates for any unbalance between the positive and negative voltages and thus is used to provide zero volts at the input of U3 which, at the output of U3, zeros the LOOP DEVIATION meter. The diodes, CR4 through CR7, limit the error signal deviation to ±1.4 volts.

Reset Switch. The reset switch includes inverter U10B, switch Q1, FETs Q2 and Q3 and associated parts. Normally, the -6 volts developed at the junction of R3 and R4 is applied through CR1 and holds Q2 and Q3 off. Therefore, the FETs do not affect the input signal. When a positive going RESET pulse is received, it is inverted by U10B and turns on Q1. The collector of Q1 approaches +15 volts which reverse biases CR1 and allows both FETs to turn on. Q2 clamps the input signal line at the junction of R7 and R8 to +5.5 volts which is supplied through Q2 and thus returns the input signal to the reference level (+5.5 volts). Q3 clamps the input signal line at the location where the feedback voltage is applied and thus returns the feedback voltage to the reference level.

The +5.5-Volt Reference Generator. The +5.5 volt reference generator includes operational amplifier U7 and emitter followers Q11 through Q14. The operational amplifier accepts 5.5 volts at its non-inverting input, from the voltage divider consisting of R54, R55 and R56. The inverting input which is slightly below 5.5 volts is obtained from the junction of R59 and R60. The ratio of these two resistors establishes the gain of the operational amplifier U7. The gain is such to amplify the slight differential voltage at the input to produce an output voltage of approximately 5.5 volts. This voltage is applied through R61 and R62 to the bases of Q11 and Q12, respectively, and causes both transistors to conduct such that 9.5 volts is dropped across Q13 and R67. The voltage dropped across R66 causes Q14 to conduct such that 5.5 volts is dropped across Q14 and R68. Thus, the junction of R67 and R68 is at 5.5 volts.

When the output voltage of the generator tends to increase, the output of the operational amplifier increases and causes the current through Q12 to decrease and the current through Q11 to increase. The resultant increased current through Q14 and decreased current through Q13 maintains the output of the generator at 5.5 volts. When the output voltage of the generator tends to decrease, a similar but opposite process occurs to maintain the output voltage at 5.5 volts. C22 is a filter capacitor which eliminates any ripple voltage. C21 bypasses to ground any ripple voltage from the +5.5 volt source line.

$\overline{\text{EQUAL LT}}$ and $\overline{\text{LOSS LT}}$ Buffers. The $\overline{\text{EQUAL LT}}$ buffer includes buffer U13A and pull-up resistor R79. The $\overline{\text{LOSS LT}}$ buffer includes buffer U13B and pull-up resistor R80.

4.8.13 Low Frequency Phase-Locked Loop Filter Type PLL102

The type PLL102 card (see schematic drawing 460-1059) contains circuits of the low frequency tracking loop filter section (see figure 4-16), two inverters used in the program control functional area, another inverter used in the program and operational status display functional area, and the lamp test circuit also used in the program and operational status display functional area. The circuits of the low frequency tracking loop filter section include the loop filter, decade decode circuit, DEC 1 driver, raysistor control circuit, the RESET switch and the capacitor discharge circuit. Each of these circuits is explained in the following paragraphs. The lamp test circuit also is explained. Because of their simplicity, no detailed explanantion is required for the three inverter circuits.

Loop Filter. The loop filter includes operational amplifiers U1 through U4, FETs Q1 and Q2, relays K1, K2, K5, K6, and associated parts. Signal paths of the loop filter are referenced to 5.5 volts, rather than to ground so that the output signal, LFΔV, varies above and below 5.5 volts as the width relationship of the positive and negative input pulses changes from an equal-width status when the VCO frequency is correct. Essentially, the loop filter is differential amplifier U3 whose input signal is conditioned by an RC network. A simplified version of the RC network would be two resistors, R_L and R_S, and a capacitor C_L, all connected in series between the signal input and signal return (+5.5 volts). The junction of the two resistors would be connected through capacitor C_S to signal return. For a bit rate of 10^0 or 10^1 bps and when LOOP 1 is selected, resistors R7 and R8 would be considered as one resistance, R_L, and R9 would be R_S. Further, C15 would be C_L and C14 would be C_S. The effective capacitance of C_S is determined by the gain of U4 which, in turn, is controlled by the resistive element of Raysistor Z2. Therefore, as the bit rate within a decade increases, VD1 increases, the resistance of Z2 increases, the gain of U4 decreases and the effective capacitance of C_S decreases.

The gain of U4, in addition to being controlled by VD1, is also controlled by FET Q1 which, in turn, is controlled by DEC 1. When the bit rate is 10^0, Q1 is off, leaving only R49 in the feedback circuit for U4 rather than the parallel combination of R29 and R31. Thus, when the bit rate is increased from the 10^0 decade to the 10^1 decade, the gain of U4 decreases and the effective capacitance of C_S decreases. Therefore, the effective capacitance of C14 decreases linearly as the bit rate increases from 1.000×10^0 to 9.999×10^1.

In a manner similar to that just described, the effective capacitance of C_L is controlled by the gain of U2, which in turn is controlled by the resistance of Z1 within the decades and by the state of Q2 between decades. Thus, the effective capacitance of C15 decreases linearly as the bit rate increases from 1.000×10^0 to 9.999×10^1.

When the bit rate increases to the 10^2 or 10^3 decade, relay K1 is deenergized and relay K2 is energized. This reduces, by a factor of 100, the values of C_L and C_S. The VD1 controlled circuit and the DEC 1 controlled circuits continue to operate in the same manner as that described for decades 10^0 and 10^1. Thus, the effective capacitances of C_L and C_S are linearily reduced as the bit rate increases from 1.000×10^2 to 9.999×10^3.

When LOOP 2 is selected, relay K5 is energized and causes R2 and R3 to parallel R_S and R_L, respectively. This reduces the RC time constant of the filter and, in effect, causes a reduction in bandwidth. In a similar manner, when LOOP 3 or LOOP 4 is selected, relay K6 is energized and causes R4 and R5 to parallel R_S and R_L, respectively. Because the values of R4 and R5 are less than the values of R2 and R3, the bandwidth of the filter is further reduced.

Decade Decode Circuit. The decade decode circuit includes inverters U10F and U10E, NAND gates U9A, U9B and U9D and associated parts. These logic elements combine DEC 2 and DEC 4* to provide a low level at the output of U9A when the bit rate is 10^0 or 10^1; or to provide a low level at the output of U9B when the bit rate is 10^2 or 10^3. A low level at either output energizes its associated relay in the loop filter. The decade decode circuit is capable of decoding bit rates of 10^4 and 10^5 which energize K3 in the loop filter; however, this circuitry is for further expansion and presently is not used. Bit rates of 10^4 and 10^5 as well as 10^6 are processed in the high frequency phase-locked loop filter section.

The DEC 1 Driver. The DEC 1 driver includes inverter U8A, emitter follower Q10 and associated parts. DEC 1 is high when processing bit rates of 10^1, 10^3 and 10^5, and low when processing bit rates of 10^0, 10^2, 10^4 and 10^6; however, because this section is operational only for bit rates of 10^3 and lower, the higher bit rates can be disregarded. When DEC 1 is high, the output of U8A is low, which turns on Q10. The resultant voltage drop across R60 causes a high level at the collector of Q10 which reverse biases diodes CR11, CR7 and CR8. When the diodes are reversed biased, their associated FETs are allowed to conduct. When DEC 1 is low, the high level from U8A-2 turns off Q10. The low level at the collector of Q10, which approaches -15 volts, causes diodes CR11, CR7 and CR8 to conduct. The resultant negative voltage applied to the gate element of the three associated FETs causes these FETs to be cut off. Resistors R57, R58 and R59 provide biasing for Q10. Capacitor C32 bypasses to ground any transients occurring across R60 when DEC 1 is changing levels.

Raysistor Control Circuit. The Raysistor control circuit includes operational amplifier U5, FET Q7 and associated parts. These provide during the 10^1 and 10^3 decade ranges a voltage proportional to VD1 that opposes the VD1 signal applied to U6 and U7. This circuit limits the effect of VD1 upon the Raysistor elements, to improve the linearity in the loop filter. The Raysistor control circuit also includes two

identical drivers. The driver associated with Raysistor Z1 includes operational amplifier U6, emitter follower Q8 and associated parts. The driver associated with Raysistor Z2 includes operational amplifier U7, emitter follower Q9 and associated parts. Because the two drivers are identical, only the one associated with Z1 is explained.

Operational amplifier U5 is operated as a unity gain amplifier. When the bit rate is in 10^0 or 10^2 decade range, a low level from DEC 1 driver holds Q7 off. The input to operational amplifier is approximately -4 volts obtained from the junction of R48 and R49, thus, the output of U5 is a -4 volts dc level applied through R53 to the input of U6. VD1 also is applied to the input of U6 through the resistive element, Z1. VD1, which varies from 0.5 to 5 volts as the bit rate is changed from 1.000 to 9.999 in conjunction with the -4 volt level, causes the output of U6 and also the emitter current of Q8 to change until the current through R53 is equal to the current through the resistive element of Z1. When equal currents are obtained, the voltage across the bulb element is within the range of 2 volts, when the bit rate is 1.000, to 1 volt, when the bit rate is 9.999. Thus, as the bit rate increases, the brilliance of the bulb decreases and the resistance of the resistive elements of Q1 increases. Thus, resistance between pins 3 and 4 of Z1, which is in the loop filter, varies over a 2-to-1 range as VD1 changes to provide linear tracking.

When the bit rate is in 10^1 or 10^3 decade range, a high level from DEC 1 driver holds Q7 on, which thereby applies VD1 through R52 to the input of U5. The resultant input voltage to U5, and also the output voltage of U5, varies from 12 volts when the bit rate is 1.000, to ground when the bit rate is 9.999. Under these conditions the voltage across the bulb element of Z1 varies from 1.5 volts when the bit rate is 1.000 to zero volts when the bit rate is 9.999. This increased range provides the tracking necessary when the decade range is 10^1 or 10^3.

The feedback circuit, including C34 and R66, stabilizes the gain through U6 and Q8. Diode CR12 limits any negative excursion to -0.7 volt. Capacitors C26 through C29 bypass to ground any signal currents from the +15 and -15 volt lines.

The RESET Switch. The RESET switch includes FETs Q3 and Q4, a differential amplifier consisting of transistors Q5 and Q6, inverter U8B and associated parts. The output signal from the loop filter normally is applied through Q4, which is conducting to the high frequency tracking loop filter section. During this time, Q3 is held off by the -15 volts applied through R42 and CR9. These conditions are achieved because RESET is low and the output of U8B is high; this high approaches +15 volts because the inverter has an open collector circuit. Therefore, the base of Q5 is more positive than the fixed bias of approximately +14 volts obtained from the junction of R46 and R47. Thus, Q5 is off and Q6 is on. Because Q6 is on, the voltage drop across R41 causes CR10 to be reverse biased and permits Q4 to conduct.

Because Q5 is off, the negative voltage applied through R42 and CR9 holds Q3 off. When RESET is present, U8B-2 is held low, to approximately zero volts; therefore, the junction of R43 and R44 is negative with respect to the Q6 base voltage which changes the state of each transistor and each FET. Thus, in the reset condition, Q4 is off and thereby disconnects the signal from the output line, and Q3 is on and thereby connects 5.5 volts to the output line.

Capacitor Discharge Circuit. The capacitor discharge circuit includes inverter U10C, relay K4 and associated parts. Normally, the relay is deenergized and the loop filter is not affected. When RESET is present, the high level causes U10C-6 to go low and thus energizes K4. The closed contacts of the relay apply 5.5 volts through current limiter R10 to one side of capacitors C14 and C15 or C16 and C17, whichever pair is connected through their associated relay. Because the other end of these capacitors also is at 5.5 volts, the capacitors are discharged. Capacitors C18 and C19 and relay K3 are included for future expansion.

Lamp Test Circuit. The lamp test circuit includes inverters U12A through U12F and U11B through U11F and pull-up resistor R65. During the quiescent condition, the 5 volts applied through R65 holds these open collector inverters off. Because these inverters are ORed with their associated driving element, the lamp is either on or off, depending on the state of the driving element. When LAMP TEST pushbutton is depressed, ground, applied to the input of each inverter, turns the inverters on and thereby provides a ground return for each of the lamps. The other end of each lamp is connected to the +5 volt source.

4.8.14 Line Drivers Type LDR023

The type LDR023 card (see schematic drawing 460-0949) contains the circuits of the line drivers section (see figure 4-22). These circuits include eight identical 50 ohm, 0 to 4 volt output line drivers and one 50 ohm, 0 to -6 volt output line driver. One of the eight 0 to 4 volt drivers and the 0 to -6 volt driver are described in the following paragraphs. The 0 to -6 volt driver is not used in this bit synchronizer.

Zero to 4 Volt Line Driver. Input 7 (see schematic drawing) feeds U2B and U6A. U2B is a standard gate used as an inverter which feeds U10C and U10D. These are open collector gates used as inverters to supply the large amount of current required to drive a long 50 ohm terminated coaxial cable down to zero volts (from +4 volts) within a fall time of less than 15 nanoseconds. Network U6A, which accepts the input signal at pins 5 and 6, has its output paralleled with the output of NAND gates U10C and U10D. This network supplies the current required to ensure the positive-going transition change from zero volts to +4 volts within 15 nanoseconds. Isolation resistor R1 is connected to a test point and allows monitoring of the output signal without affecting circuit operation.

Zero to -6 Volt Line Driver. This line driver, identified as driver 1, includes two differential amplifiers; one contains transistors Q6 and Q7. Transistors Q3 and Q4 are the switches that switch the output line between ground and -6 volts, respectively. Transistor Q5 provides current limiting. Transistors Q8 through Q11 form a regulator circuit to provide -6.5 volts. Details of this circuit are explained in the following paragraphs.

The input to the -6 volt driver is applied through base-damping resistor R9 to the base of Q1. The base of Q2 is clamped to +1.4 volts by the divider formed by R11, CR1 and CR2. The common emitter resistor R10 sets the current through the differential amplifier Q1, Q2. The inverting output, from the collector of Q1, and developed across collector load resistor R19, is fed to the base of Q7, one-half of the other differential amplifier. The other side (Q6) of this differential amplifier has its base clamped at -10 volts by divider CR8 and R17. Diodes CR6 and CR7 clamp the voltage swing to 0.7 volt above and below the base voltage (-10 volts) of Q6. Resistor R18 sets the current through the differential amplifier. The output signal from Q6 (inverted from input 1) is developed across collector load resistor R12 and is fed to the base of emitter follower Q3. The collector of Q7 feeds the base of common emitter Q4. Transistor Q2 collector also feeds the base of Q4 through diode CR4. Resistor R16 is the current sense resistor and Q5 is the current limit amplifier. Diodes CR3 and CR5 prevent excessive reverse bias at the base to emitter junctions of Q3 and Q4, respectively, and thus minimizes the turn-on time.

When the input signal at the base of Q1 is high, transistors Q1 and Q7 are off and Q2 and Q6 are on, which causes Q3 to be off and Q4 to be on; therefore, output 1 (at pin 28) is -6 volts. When the input is low, Q1 and Q7 are on and Q2 and Q6 are off, which causes Q3 to be on and Q4 to be off; therefore, output 1 is excessive emitter-to-collector current when driving the output to -6 volts. R14 feeds the current sense back to the base of Q5 and R15 feeds the output voltage back to the base of Q5. The net effect of these two signals turns Q5 on. When Q5 turns on, the collector of Q2 is driven to -6.5 volts which back biases CR4 to remove the base drive to Q4 until Q4 collector current is reduced.

The junction of resistors R20 and R21 provides -6.5 volts that is applied to the base of Q8. This voltage causes the emitter current to develop approximately -5.8 volts across R22, the emitter resistor for Q8. This voltage is applied through resistor R23 to the emitter of Q9. The output of Q9 across collector load resistor R24 feeds the base of Q10 which, together with Q11, forms cascaded emitter followers which serve as the pass transistors for the regulator. Resistors R29 and R27 limit the collector current through Q10 and Q11. Resistor R26 is the base damping resistor and R25 is the emitter load resistor for Q10.

If the regulated output voltage (-6.5 volts) tends to become less negative because of high current flow through the pass transistors, Q9 collector current decreases and allows the collector voltage to become more negative. This voltage, applied to the base of Q10, causes the voltage drop across the pass transistors to decrease and thereby restores the regulated output voltage to -6.5 volts. If the regulated output voltage tends to become more negative than -6.5 volts, a similar but opposite process occurs through Q9, Q10 and Q11. The net effect of this process is to increase the voltage drop across the pass transistors which restores the regulated output voltage to -6.5 volts.

4.8.15 Line Drivers Type LDR024

The type LDR024 card (see schematic drawing (460-0980) contains two tape recorder line drivers used in the line driver section (see figure 4-22). These line drivers accept two independent signals and provide, for each input, bipolar signals that can be set from ±1 to ±3 volts to drive 50 ohm lines and terminations. The card contains individual but identical circuitry to process the two input signals. These two areas are identified as driver 1 and driver 2 in the schematic drawing. Also identified are the positive voltage regulator and the negative voltage regulator which establish the high and low levels for the outputs of both driver 1 and driver 2. The negative voltage regulator is adjustable and provides a voltage between -1 and -3 volts. The positive voltage regulator accepts this negative voltage and provides a positive voltage with the same absolute value as the negative voltage from which it was derived. The output stages of both drivers use these plus and minus voltages to produce their outputs; thus, the amplitudes (between 1 and 3 volts peak) of the bipolar output are set within the negative voltage regulator.

Negative Voltage Regulator. The absolute peak value of the bipolar signal is set by potentiometer R32 which, in conjunction with R23 and R37, applies between -0.7 and -3.6 volts to the base of Q16. Transistor Q16 and Q17 form a differential amplifier. Resistor R24 sets the current within the amplifier, R26 sets the stage gain, R38 limits the collector current of Q16 and R39 is the collector load for Q17. The collector voltage of Q17 is applied to the base of Q18 which is an emitter follower cascaded with pass transistor Q19. The negative voltage that is used for the low level of the output signals is obtained from the emitter of Q19. Resistor R25 is the emitter load resistor for Q18, R40 limits the Q18 collector current, R33 is the base damping resistor for Q19, and R35 and R41 limit the Q19 collector current. The Q19 emitter voltage also is fed back to the base of Q17 as a sense voltage for regulation. As the Q19 emitter voltage tends to go less negative, the forward base bias of Q17 is decreased and causes the Q17 collector current to decrease and the collector voltage to go more negative. This more negative voltage, applied to the base of Q18, reduces the collector-to-emitter resistance to the cascaded pair (Q18 and Q19) and thereby restores the Q19 emitter voltage back to its regulated value. As the Q17 emitter voltage tends to go more negative, a similar but opposite process to that just described will occur to restore the regulated voltage.

Positive Voltage Regulator. The positive voltage regulator can be considered an inverting operational amplifier with a gain of unity. Transistors U1Q3 and U1Q4 form a differential amplifier with the base of U1Q3 clamped to ground through R14. When the positive voltage output (at the Q1 emitter) is of the same absolute value as the negative voltage output, the voltage at the junction of R5 and R17 (resistors have equal value) is zero volts. As the U1Q4 base voltage tends to deviate from zero volts, the U1Q4 collector voltage developed across R2 drives cascaded emitter followers U1Q2 and U1Q1. These transistors operate in the same manner as transistors Q18 and Q19 described in the previous paragraph, to maintain the plus voltage output at the same absolute value as the negative voltage output. Resistor R1 limits the collector current of U1Q3. Resistors R15, R16 and R18 set the currents through the differential amplifiers. Resistor R3 limits the U1Q2 collector current and R4 is the emitter resistor for U1Q1. Resistor R6 is the base damping resistor for Q1.

Drivers. Because both drivers are practically identical, only driver 1, including a threshold circuit that is common to both drivers, is explained. Input 1 (pin 5) is applied through damping resistor R13 to the base of Q3 which, together with Q2, forms a differential comparator. A threshold voltage (1.4 volts) which is applied to Q2's base is obtained from the voltage divider consisting of R11, CR1 and CR2. This threshold voltage which is common to both drivers also is applied to Q14 base. Resistor R12 sets the comparator current. The inverted output signal from Q3 which is developed across R22 is applied to the base of Q9. Transistors Q8 and Q9 form another differential comparator with the base of Q8 clamped to -8.8 volts by R29 and CR9. Diodes CR5 and CR6 limit the signal at the base of Q9 to ±0.7 volt with respect to the base of Q8. The Q9 collector output signal, developed across CR3 and R7 is the same polarity as the input signal and is applied to the base of pull-up transistor Q4. The Q8 collector output signal, developed across CR10 and R8, is inverted with respect to the input signal and is applied to the base of pull-down transistor Q10. Resistors R19 and R27 are current sampling resistors for Q4 and Q10, respectively. When excessive current is sensed in either resistor, the increased voltage drop across R19 or R27 forward biases its associated transistor (Q5 and Q11, respectively). This in turn, reduces the forward bias and the collector-emitter current in its associated pull-up or pull-down transistor as applicable. Diodes CR7 and CR12 prevent Q4 and Q10 from being driven too far into cutoff and enhance the turn-on time of these transistors. When input 1 (pin 5) is low, Q2, Q8 and Q4 are off and Q3, Q9 and Q10 are on, causing output 1 (pin 27) to be pulled to the negative regulated voltage (as set between -1 and -3 volts). If the output load draws excessive current, the voltage across R27 turns on Q11 which, through its collector current, pulls the base of Q10 towards the negative regulated voltage. With increased negative voltage on the base, Q10 limits the collector-emitter current to an acceptable value. When input 1 (pin 5) is high, Q2, Q8 and Q4 are on and Q3, Q9 and Q10 are off, causing output 1 (pin 27) to be pulled to the positive regulated voltage. Transistor Q4 has the same type of current sensing circuitry as Q10 which was just described.

4.8.16 Program Decoding Type PDC001

The type PDC001 card (see schematic drawing 460-0985) contains the amplitude detector and offset detector circuits which are part of the operational status display section (see figure 4-28). The card also contains the program decoder, circuit loop bandwidth adder and the source select adder which are part of the program decoding section (see figure 4-26). Each circuit is explained in the following paragraphs.

Amplitude Detector. The amplitude detector (see schematic drawing 460-0985) consists of meter driver U1B and U1D, comparator U1A, $\overline{\text{LOSS}}$ drivers Q1 and Q2 and X LOSS switch U1C. This circuit accepts the AGC/V signal whose normal range is -0.5 to -4 volts and cause a meter deflection in accordance with the amplitude of the AGC/V. In addition, when the AGC/V approaches +0.7 volt, which occurs during spill condition, the comparator turns on the $\overline{\text{LOSS}}$ drivers which, in turn, light the front panel LOSS lamp. The circuit also accepts X LOSS which is normally a low level. When this level goes high, U1C is turned on and causes Q2 to be turned on. Transistor Q2, when conducting, provides the ground return to light the LOSS lamp. Thus, the LOSS lamp is turned on by either a positive AGC/V or X LOSS. Transistor U1D compensates for the base-to-emitter drop of U1B. Because the base of U1D is grounded, the emitter is clamped at -0.7 volt. This voltage is applied to the plus side of the meter. The voltage on the emitter of U1B rides 0.7 volt more negative than the base and it is this voltage that is applied to the meter; therefore, the meter indication reflects the true value of AGC/V. These two voltages from the emitters of U1B and U1D are also applied to the bases of comparator U1A. The reference voltage, -0.7 volt, from U1D is applied to the pin 2 base of U1A and the AGC voltage is applied to the pin 4 base of U1A. As long as the AGC voltage remains more negative than the reference voltage, the right hand side transistor (pins 3, 4, 5) remains off, which in turn holds $\overline{\text{LOSS}}$ driver transistors Q1 and Q2 in the off state. However, when AGC/V goes positive, the positive voltage (any voltage more positive than -0.7 volt) applied to the pin 4 base of U1A turns that transistor on, which then turns on Q1 and Q2. Transistor Q2, when conducting, lights the LOSS lamp. Resistor R1 and Zener diode CR1 provide +5.1 volts for operation of the detector circuit.

Offset Detector. The offset detector (see schematic drawing 460-0985) consists of the positive threshold detector, Q4 and Q5, negative threshold detector Q7 and Q8, and lamp drivers Q3 and Q6. When OFST/V is between -2 and +2 volts, Q5 and Q7 are conducting; thus, the other transistors (Q4 and Q8) in each comparator are turned off. Because both Q4 and Q8 are off, Q3 and Q6 are off. Thus, the OFFSET lamp is not lit. When OFST/V is more negative than the reference voltage (-2 volts) established by R25 and R26, and is applied to the base of Q8, Q7 is turned off and Q8 is turned on. The larger voltage drop across R17 turns Q3 on. Transistor Q3, being on, raises the base voltage of Q6 and turns it on. Transistor Q6 provides the ground

return to light the OFFSET lamp. When OFST/V is more positive than the reference voltage (+2 volts) established by R19 and R22, and is applied to the base of Q5, Q4 is turned on and Q5 is turned off. When Q5 is turned on, it causes the same process as described when Q8 is turned on.

Loop Bandwidth Adder. The loop bandwidth adder (see schematic drawing 460-0985) is composed of NAND, NOR and inverter logic elements that change the two-line signal inputs representing digital values of 0, 1, 2 and 3, to three-line signal outputs representing digital values of 1, 2, 3 and 4, respectively. The truth table for the loop bandwidth adder is shown in table 4-14.

Table 4-14. Loop Bandwidth Adder Truth Table

INPUTS		OUTPUTS		
LB2	LB1	LBW 4	LBW 2	LBW1
0	0	0	0	1
0	1	0	1	0
1	0	0	1	1
1	1	1	0	0

Source Select Adder. The source select adder (see schematic drawing 460-0985) is composed of NAND, NOR and inverter logic elements that change the two-line signal inputs representing digital values of 0, 1, 2 and 3 to three-line signal outputs representing digital values of 1, 2, 3 and 4, respectively. The truth table for the source select adder is shown in table 4-15.

Table 4-15. Source Select Adder Truth Table.

INPUTS		OUTPUTS		
IB2	IB1	S3	S2	S1
0	0	0	0	1
0	1	0	1	0
1	0	0	1	1
1	1	1	0	0

Program Decoder. The program decode logic (see schematic drawing 460-1096) is composed of a BCD-to-decimal converter U5 and other logic elements (NAND and NOR gates and inverters). The BCD-to-decimal converter U5 converts XB1, XB2 and XB4 BCD inputs to 0 through 7 decimal outputs. The decimal output lines, together with CODE, DM-M, are decoded by the logic elements as shown in table 4-16.

Table 4-16. Program Decoder Truth Table

CODE SELECTED	INPUT SIGNALS				OUTPUT SIGNALS												
	CODE DM-M	XB4	XB2	XB1	CNRZ	CRZ	CSØ	RZ+L	SØ+SØ-M	DM	L-LT	M-LT	S-LT	NRZ-LT	RZ-LT	SØ-LT	DM-LT
NRZ-S	0	0	0	0	1	0	0	0	1		1	1	0	0	1	1	1
NRZ-M	0	0	0	1	1	0	0	0	0	0	1	0	1	0	1	1	1
NRZ-L	0	0	1	0	1	0	0	1	0	0	0	1	1	0	1	1	1
RZ	0	0	1	1	0	1	0	1	0	0	1	1	1	1	0	1	1
BIØ-L	0	1	0	0	0	0	1	1	0	0	0	1	1	1	1	0	1
BIØ-M	0	1	0	1	0	0	1	0	1	0	1	0	1	1	1	0	1
BIØ-S	0	1	1	0	0	0	1	0	0	0	1	1	0	1	1	0	1
DM-S	0	1	1	1	1	0	0	0	1	1	1	1	0	1	1	1	0
DM-M	1	1	1	1	1	0	0	0	0	1	1	0	1	1	1	1	0

4.8.17 Decode Driver Type DDR022

The type DDR022 card (see schematic drawing 460-0836) contains the circuitry for the unit address decode, write decode and the data word buffers which are used in the data distributor section (see figure 4-24). Each of these circuits is described in the following paragraphs.

Unit Address Decode Circuit. The unit address decode circuit has its jumpers wired for option number 1 as shown in schematic drawing 460-0836. The circuit accepts the computer address code (bits CB15 through CB12); the signal WRITE REQUEST from the computer; and the enabling pulse, TRANS STROBE, also from the computer. Computer bits CB12 through CB15 are accepted directly from the computer via the interface connector. This circuit is explained in the following paragraphs.

When the proper unit address is high, NAND gate U5B is primed, that is, the computer bit lines have levels of 0001; gate U5A is then enabled when TRANS strobe is received from the computer and WRITE REQUEST. The output from the enabled NAND gate (a low level) is inverted by U12D to become WRITE EN which is then applied to the write decode circuit.

The transfer strobe receiver consists of a differential amplifier Q1, Q3 and a common emitter amplifier Q3. A jumper is connected between pins T and U. In the quiescent state, the base of Q1 is held at a high level by the input signal or, in the absence of an input signal, by pull-up resistor R7. A level, approximately 2.5 volts, is applied to the base of Q2 from the voltage divider consisting of R11 and R12; therefore, Q1 is off and Q2 is on. The positive voltage developed across collector resistor R10 is applied to the base of Q3 and turns Q3 on. Because of the voltage drop across collector resistor R13, a low level from the collector of Q3 is applied to pin 2 of U5A where it inhibits the gate. When a low level is received at the base of Q1, it turns Q1 on and Q2 off. The low level at the emitter of Q3 is applied to the base of Q3 to turn Q3 off. The resultant high on the collector of Q3 enables U5A when the correct address is decoded on the remaining inputs of U5A.

The WRITE REQ circuit (pin 7) is the master control for the PROGRAM WRITE circuit. A high input, provided by pull-up resistor R6 or a high from the computer, which is twice inverted by U13C and U13D, is required to hold a priming level at pin 1 of U5A. A low level from the computer will inhibit this circuit. A jumper is connected between L and M. The PRO EN circuit (pin 13) is not used; however, the high input, provided by the pull-up resistor R8, which is twice inverted by U12F and U12E, is required to hold a priming level at pin 5 of U5A. The PROGRAM CONTROL circuit (pin 40) is not used; however, the high input provided by the pull-up resistor R4 is required to hold a primary level at pin 1 of U1A.

Write Decode Circuit. The write decode circuit accepts computer bits CB8, CB9, CB10 and decodes these bits to become DECODE 000, DECODE 001, DECODE 010 and DECODE 011, which are used in the program verify section of the bit synchronizer. The write bits are strobed to the output of the write decode circuit by WRITE EN from the unit address decode circuit. The write bits are used in the display section. Signal WRITE 100 also is decoded; however, this signal is not used. A truth table showing which computer bits are required to provide the various WRITE and DECODE signals is given in table 4-17.

Table 4-17. Write Decode Circuit Truth Table

COMPUTER BITS			WRITE SIGNALS				DECODE SIGNALS			
CB10 (pin 28)	CB9 (pin 26)	CB8 (pin 27)	WRITE 000 (pin 39)	WRITE 001 (pin 36)	WRITE 010 (pin 34)	WRITE 011 (pin 32)	DECODE 000 (pin 38)	DECODE 001 (pin 37)	DECODE 010 (pin 35)	DECODE 011 (pin 33)
0	0	0	1	0	0	0	1	0	0	0
0	0	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	0	1	0
0	1	1	0	0	0	1	0	0	0	1

Data Word Buffers. The data word buffers accept computer bits CB0 through CB7. These signals are twice inverted and become BCB0 through BCB7 (buffered computer bits 0 through 7).

4.8.18 Program Storage Register Type PSR021

The type PSR021 card (see schematic drawing 460-1096) stores and distributes eight data bits from the computer, or stores and distributes eight locally generated data bits. In addition, the circuitry allows locally generated data bits to change the stored data bits. The card contains an 8-bit storage register; there are four such cards in the program storage registers section (see figure 4-25). The card accepts eight data bits (BCB0 through BCB7 via pins 36, 37, 25, 26, 16, 18, 6 and 8, respectively) and a write signal (a unique signal for each of the four cards). The write signal (WRITE 000 through WRITE 011) is applied to its respective card through pins 35, 29, 15 and 9. The eight locally generated data bits are applied to the card through pins 31, 41, 22, 21, 12, 19, 4 and 7. The locally generated data bits are uniquely identified on each of the four cards used in the program storage registers section. Control levels also applied to the card include PROG at pin 39, MANUAL at pin 38, OVERRIDE at pin 28 and OVRD at pins 34, 30, 14 and 10. Eight output lines for the stored data or the locally generated data are provided at pins 32, 40, 23, 27, 13, 20, 5 and 11.

Because the eight data bits obtained from the computer and the eight locally generated data bits are identically processed on each of the four type PSR021 cards, only the logic elements that process signal BCB0 (applied to pin 36) and signal NMSD-1 MANUAL SET (locally generated data bit applied to pin 31 of the PSR021 card in slot A3A1) is described. When MANUAL/PROGRAM switch S1 is in the MANUAL position, signal MANUAL (at pin 38) is a high level and primes gate U2C which allows the locally generated data bit (NMSD-1 MANUAL SET) to be applied to the output line (pin 32). The output of U2A, which also feeds the output line is inhibited by PROG which is a low level at pin 39.

When the bit synchronizer is in the program mode of operation, BCB0 is applied through pin 36 to the data (D) input of flip-flop U9A. Signal WRITE 000 provides a positive-going transition through pin 35 to the clock (C) input of U9A which strobes BCB0 into U9A. The output of the flip-flop, from the complement side ($\overline{Q}$) passes through primed AND gate U2A to the output line at pin 32. Gate U2A is primed because, in the program mode of operation, PROG, at pin 39, is a high level obtained from the MANUAL/PROGRAM switch. The locally-generated data bit at gate U2C is inhibited by signal MANUAL which at this time is a low level.

The programmed bit stored in the flip-flop can be replaced with the manually selected bit available at pin 31. The manually selected bit is applied to pin 13 of U2D; however, to provide an output, this gate must be primed simultaneously by two signals. The first signal, obtained from OVERRIDE switch S3, applies a low level through pin 34 to inverter U10E; the second signal, obtained from OVERRIDE pushbutton S2, applies a low level through pin 28 to inverter U10D. If the input to either inverter (U10D or U10E) is high, gate U2D will not be primed. The output of U2D is applied to the clear input of the flip-flop and, through gate U2B (used as an inverter) to the preset side of the flip-flop. Gate U2B is considered to be an inverter because U2B is primed each time U2D is primed. Thus, the locally generated data bit replaces the program specified data bit in the flip-flop. The output of the flip-flop, now with the locally generated data bit, is applied to the output line as previously described in the program mode of operation.

4.8.19 Program Verify Type DDR030

The type DDR030 card (see schematic drawing 460-1097) contains the circuitry for the 16-bit program verify. The circuitry consists of a decode address circuit and verify line drivers. Decode Address Circuit is used to select the proper 8-bit program instruction which is sent to the computer via J17/J18 on the rear panel of the bit synchronizer. The Decode Command signal from the decoder driver inputs on pins 14 and 15 of Program Verify card. The Decode Command signals will prime only one of the Decode Address NAND gates: either U10B or U10C. Once the proper NAND is prime, the Verify Transition signal via decoder driver by way of the computer will enable the Decoder Address to select the proper verify line drivers. READ REQ'D (pin 11) of Decoder Address is received from the computer through J17/J18; this logic command must be enabled with a high level in order to prime the Decode Address Circuit. A low level on READ REQUEST command will inhibit the Decode Address.

Verify Line Driver consists of 16 open collector NAND gates. The circuit configuration is such that two of the NAND gates' outputs are tied together forming a collector ORing circuit. The collector ORing circuit configuration then forms the 8-bit instruction format that is sent to the computer. The DECODE-EN from the Decode Address circuit will select the proper 8-bit instruction. The other input to the NAND gate, which is the 8-bit instruction from the program registers via card pins and an inverter, is then selected and sent back to the computer as the verify 8-bits. Spare NAND gates U6 and buffer U9A are not used for program verify.

The Read Decode Circuit consists of 4 open-collector NAND gates. Here, again, the circuit configuration is such that all four of the NAND gates' outputs are tied together forming a collector ORing circuit. The DECODE-EN from the Decode Address primes all four NAND gates, but only one is enabled. The other input to the NAND gates receives the WRITE DECODES for the Decode Driver Card (A3A5). The output of the collector ORing is called INPUT ACKNOWLEDGE and sent back to the computer via J17/J18. This circuit is used only on card A4A7 of the bit synchronizer.

4.8.20 Binary Coded Decimal Multiplier Type BCD001

The type BDC001 card (see schematic drawing 460-0981) contains the circuits used in the bit rate multiplier as shown in figure 4-26. The card contains logic elements for conversion of BCD data to decimal data, select gates which select one set of four inputs or another set of four inputs, and standard NAND and NOR gates. The purpose of the circuitry is to provide an output representing a bit rate value that is twice the bit rate received from the program storage registers when processing DM type PCM signals; and to provide an output representing a bit rate value that is the same as that received from the program storage registers when processing other types of PCM signals. The input signals are four digits in BCD code identified as rate lowest significant digit (RLSD), rate next to lowest significant digit (RNLSD), rate next to most significant digit (RNMSD) and rate most significant digit (RMSD). The output signals, also in BCD code, are similarly identified except the R is deleted from the mnemonic. Before explaining the overall operation of the circuit, a brief explanation of the integrated circuit elements that perform the BCD to decimal conversion and input selection is given.

Operation of Integrated Circuits. Elements U13, U15, U17 and U19 perform the BCD to decimal conversion. These elements cause one of the output lines from 0 through 9 to go low and all other lines to remain high whenever a valid BCD code is applied to the input. Valid inputs applied to input lines A through D are binary coded decimal equivalents for digits 0 through 9. The output line that goes low is the decimal equivalent of the BCD input. Elements U6, U8, U10, U14, U16, U18 and U20 select one set of four inputs (the A inputs) and apply them to the output or select the other set of four inputs (the B inputs) and apply them to the outputs. The level at the SEL input (pin 1) determines which set of inputs is transferred to the output. When the select level is low, the A inputs are transferred and when the select level is high, the B inputs are transferred. In addition, there is an ENBL input (pin 15). The level applied to this pin must be low for the element to operate as described above. When a high level is applied to the ENBL input, the four output lines remain low.

Operation When Processing NRZ, RZ or BiØ Signals. When processing NRZ, RZ or BiØ type PCM signals, signal DM is low and is applied to pin 1 (SEL) of U14, U16, U18 and U20. These elements transfer the A inputs (1A through 4A) to the output lines (1Y through 4Y), respectively. Thus, the BCD information on the input lines is transferred directly to the output lines. The two gates, U12C and U12B, in the output line for bit 1 of the MSD, operate as inverters. Thus, they do not affect the output of this line because pin 4 of U12B is held high by the DM signal (a low level) which is applied through gate U12A to U12B.

Operation When Processing DM Signals. DM type PCM signals are processed using two different schemes which provide output signals that represent values twice that of the input signals. The first scheme is used when the significant digits of the bit rate are 4.999 or less. The second scheme is used when the significant digits of the bit rate are 5.000 or greater. During the first scheme, a low control level is generated at U11 because outputs 5 through 9 of U19 are all high. RMSD inputs to U19 are holding all of the other output lines (0 through 4) low. The low level from U11 is applied to the SEL input of U6, U8 and U10 which causes these elements to transfer the A inputs to the output terminals. The following paragraphs explain how the four input digits are doubled.

1. Gates U5A, U5B and U1A generate the three most significant bits of BCD whose value is equivalent to twice the decimal value of RLSD. The least significant bit does not have to be decoded because any digit multiplied by two is an even digit and when converted to BCD has a zero as the least significant bit. Thus, the input to pin 11 of U6 is always zero (ground). When RLSD is 5 or greater, a carry is generated at U1B and added to the NLSD. Table 4-18 gives, for each possible output of U13: the BCD levels obtained from gates U1A, U5B and U5A; which digits generate a carry; and the decimal equivalent of the BCD output which, in conjunction with the carry, is twice the value of the decoded digit obtained from U13. The elements that provide these signals within the RLSD circuitry are given in parentheses in the column headings of the table.

Table 4-18. Doubling Process

DECODED DIGIT (U13)	BCD OUTPUTS				CARRY (U1B)	DECIMAL EQUIVALENT OF BCD
	2^3 (U1A)	2^2 (U5B)	2^1 (U5A)	2^0 (GND)		
0	0	0	0	0	0	0
1	0	0	1	0	0	2
2	0	1	0	0	0	4
3	0	1	1	0	0	6
4	1	0	0	0	0	8
5	0	0	0	0	1	0
6	0	0	1	0	1	2
7	0	1	0	0	1	4
8	0	1	1	0	1	6
9	1	0	0	0	1	8

2. Gates U7A, U7B and U2B generate the three most significant bits of BCD whose value is equivalent to twice the decimal value of RNLSD. As explained in the preceding paragraph, the doubling process results in a predictable least significant bit; however, if a carry is generated when the next lower

significant digit is doubled, that carry becomes the least significant bit of RNLSD. Thus, when a carry is generated at U1B, the NLSD value is increased by 1. When RNLSD is 5 or greater, the doubling process causes a carry to be generated at U2B. This carry is added to NMSD.

3. The NMSD is processed identically to that of the NLSD explained in the preceding paragraphs except that gates U9A, U9B and U3A generate the three most significant bits of BCD and the carry is generated at U3D.

4. The value of the MSD is always 4 or less in this scheme; therefore, the most significant bit in the RMSD is always zero. Thus, by shifting the RMSD bits left one position and adding the carry from the NMSD, the BCD output of U20 is twice the value of the RMSD or one digit higher if there was a carry from NMSD. Shifting is accomplished by transferring RMSD 1 through U20 to MSD 2, by transferring RMSD 2 through U20 to MSD 4, or by transferring RMSD 4 through U20 to MSD 8. The carry from NMSD is applied through U20 to MSD 1. The non-significant RMSD 8 is not used.

During the second scheme when the significant digits of the bit rate are 5.000 or greater, a high control level is generated at U11 because one of the outputs 5 through 9 is low. The high level from U11 is applied to the SEL inputs of U6, U8 and U10 which cause these elements to transfer the B inputs to the output terminals. The following paragraph explains how the four input digits are doubled by shifting the double value BCD to the next lower digit circuitry and, if necessary, generating a DEC ADD signal which increases the multiplier of the complete bit rate value by a factor of 10.

1. In this scheme, only the carry output from the LSD is used; the three most significant bits from LSD are not required. The three most significant bits of NLSD are transferred through gates U7A, U7B and U2A to the B inputs of U6; therefore, these bits become the three most significant bits of LSD. The least significant bit of LSD is obtained from U1B. Thus, LSD represents twice the value of the RNLSD digit plus one if a carry was generated in the LSD.

2. In a manner similar to that just described, the three most significant bits of NMSD are transferred through gates U9A, U9B and U3A to the B inputs of U8 and, therefore, become the three most significant bits of NLSD. The least significant bits of NLSD is obtained from U2B. Thus, NLSD represents twice the value of the RNMSD digit plus one if a carry was generated in the NLSD.

3. The input bits to RMSD must represent a digit between 5 and 9. Thus, double this value is between 10 and 18. The digit in the tens position, which is always a one, is placed as a carry in the MSD output which, as will be explained in the

following paragraph, is always 0001. The digit in the units position, which is always even and between 0 and 8, has the 3 most significant bits of its equivalent BCD decoded by U4. The least significant bit is obtained from the carry of NMSD at U3A. Thus, NMSD represents twice the value of RMSD digit plus one if a carry was generated in NLSD.

4. In this second scheme of operation, the MSD is always 1 (BCD equals 0001). This is accomplished because signal DM is high and applied to pin 1 of U12A and the output of U11 is high and applied to pin 2 of U12A. The resultant low level is inverted by U12C and applied as a high to ENBL input (pin 15) of U20. This causes all outputs of U20 to go low. The low level from U12A also is applied to pin 4 of U12B. Therefore, the output of U12B is high and thus provides a 1 bit for the least significant bit of MSD. The MSD has a BCD output of 0001. Because the bit rate digits were shifted right during the doubling process, the output value represented by LSD, NLSD, NMSD and MSD must be raised by the power of 10 to reflect a true doubled value. This is accomplished by the DEC ADD signal obtained from U12D. When this signal is high, the exponent generated in the decade adder circuit (see schematic drawing 460-0982) is increased by one.

5. As an example of how the second scheme processes the digits, assume that an input bit rate of 6.155×10^2 (615.5 bps) is received and doubled to 1.231×10^3 (1231 bps). The least significant digit (5) of the input bit rate becomes the least significant digit of the doubled value and the 1 in the tens column of the 11 becomes the carry. The next digit (1) of the input bit rate is doubled to 2 and the carry added to make 3 which becomes the NLSD of the doubled value. The last digit of the input rate (6) is doubled to 12 and becomes the MSD and NMSD digits of the doubled value. The resultant value of 1.231 is then multiplied by 10 by increasing the multiplier from 10^2 to 10^3 via DEC ADD signal. The resultant value of 1231 bps is twice the value of the input rate of 615.5 bps.

4.8.21 Crystal Oscillator Type XTL028

The type XTL028 card (see schematic drawing 460-1105) contains the circuits of the automatic calibration section (see figure 4-19). These circuits include the 1 kHz reference generator, program status circuit, and the 2-digit storage and comparator. This card also contains two pull-up resistors that are connected to the X10 display DS5 of the BIT RATE display and four isolation diodes used in the program and operational status displays functional area (see figure 4-28). The 1 kHz reference generator and the 2-digit storage and comparator are explained in the following paragraphs.

The 1 kHz Reference Generator. The 1 kHz reference generator includes the 4 MHz crystal oscillator Y1 and its associated on-off switch S1, two flip-flops U8A and U8B, which are used as divide-by-two dividers and three identical divide-by-ten dividers. Switch S1 is normally in the ON position; it is provided for maintenance purposes. The 4 MHz output from the oscillator is applied through the two flip-flops U8A and U8B. The Q output of U8B is 1 MHz and is applied to output pin 24 which is then connected via library wiring to input pin 22. This 1 MHz reference signal is then applied serially through the three divide-by-ten dividers, U5, U6 and U7. The output of U7, at pin 12, is the 1 kHz reference signal. The remaining signals, 100 kHz, 10 kHz and 2 kHz, are not used.

The Program Status Circuit. This circuit is not used in the operation of the bit synchronizer.

The Two-Digit Storage and Comparator. The two-digit storage and comparator includes U1, which stores the four bits of the next to the most significant digit of bit rate; U2, which stores the four bits of the most significant digit of bit rate; U3, which compares the digit stored in U1 with the most current next to the most significant digit; and U4, which compares the digit stored in U2 with the most current most significant digit.

When $\overline{EQ}$ goes low, the eight incoming bits representing the two digits are stored in U1 and U2. These bits are then available at outputs A, B, C, and D of U1 and U2 and applied to the A inputs of U3 and U4 respectively. Immediately after the two digits are stored, the A=B output of U4 goes high because the B inputs of U3 and U4 are the same as the A inputs of U3 and U4. If, after the two digits are stored in U1 and U2, either of the two digits is changed, the A=B output of U4 goes low and generates a full AUTO-CAL cycle. The A>B and A<B outputs are not used.

SECTION V

MAINTENANCE

5.1 GENERAL

This section provides preventive and corrective maintenance information and procedures and also includes, as a separate grouping, maintenance data which is supplemental information used primarily when isolating a defective part within a malfunctioning circuit or a printed-circuit card. Schematic/logic diagrams, wiring diagrams and assembly drawings of the pc cards are available in Section VI.

The basic philosophy incorporated into the maintenance section is to use the preventive maintenance procedures to minimize possible failures and, if repairs are necessary, to effect them during scheduled downtime rather than operational time. If the equipment should malfunction during operational time, the technician uses the corrective maintenance information and the maintenance data to restore the equipment to operational status as quickly as possible. The importance of a scheduled and thorough preventive maintenance program cannot be over-emphasized, so that cleaning, adjusting and repairing can be completed without compromising the overall mission of the system in which the bit synchronizer is used.

Corrective maintenance procedures include minimum performance standards, test and adjustment procedures, troubleshooting information, and repair and replacement procedures. The minimum performance standards which are referenced in the preventive maintenance schedule also can be used at any time to determine whether or not the bit synchronizer is operating properly and, if not operating properly, to indicate which function or circuit of the equipment is malfunctioning. Using the test and adjustment procedures and the troubleshooting information, the technician can isolate the malfunctioning circuit to a pc card or to a portion thereof. The technician then isolates the defective part on the malfunctioning pc card by using the information contained in the theory of operation discussions in Section IV and the maintenance data contained in this section. This data includes terminal voltages and references to waveforms, schematic and wiring diagrams and other related maintenance aids.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance includes prescribed cleaning, repairing and testing procedures that must be performed periodically to keep the bit synchronizer at its maximum operating efficiency. These procedures are included in the preventive maintenance schedule. Additionally, lubrication and minor repair instructions are given. See table 5-1 for the preventive maintenance schedule.

Table 5-1. Preventive Maintenance Schedule

ITEM	FREQUENCY	PROCEDURE
Indicators	Daily	Depress LAMP TEST pushbutton. All indicator lamp and display segments light. Replace defective lamps in accordance with instructions given in paragraph 5.2.3.
Front and rear panels	Weekly	Dust with clean, lint-free cloth, with vacuum cleaner using soft brush attachment or with low pressure (10 to 15 psi) compressed air. For stubborn dirt on metal surfaces use a clean, lint-free cloth dampened with cleaning solvent per Federal Specification P-S-61, Type II. For stubborn dirt on meter or display faces use a clean, lint-free cloth and a mild soap and water solution to remove the dirt and then rinse and wipe dry.
Cooling fans	Weekly	Visually observe that both cooling fans are operational and, if necessary, clean. If fans must be cleaned more often than once a month, external air supply is not being adequately filtered.
Operational check	Monthly	Perform minimum performance standards (table 5-2).
Interior surfaces	Semiannual	Loosen knurled locking screws at the two upper corners of the front panel and pull bit synchronizer to its completely extended position. Remove top and bottom covers. Using low pressure (10-15 psi) compressed air or a vacuum cleaner, carefully remove all dust from the interior of the unit. Check for visibly damaged or loose parts. Repair or replace, as necessary. Ensure all printed circuit cards are seated properly. Clean top and bottom covers and then replace. Release the latches on the side of the slides and then push the bit synchronizer into a closed position. If slides do not operate smoothly, lubricate in accordance with instructions given in paragraph 5.2.1, otherwise repair or replace, as necessary.

5.2.1 Lubrication

The only part of the bit synchronizer that requires lubrication is the rack slides. Annually, apply MIL-L-15016 lubricant to the bearing surfaces of the slides that attach to each side of the equipment rack. Use a nozzle type applicator to apply the lubricant.

5.2.2 Fuse Replacement

Fuse F1 is a 3AG, slo-blo type rated at 2.5 amperes. To remove the fuse, press the cap of fuseholder XF1 towards the rear panel and simultaneously rotate the cap counterclockwise. Spring tension forces the cap and fuse from the fuseholder. Pull the defective fuse from the cap and then replace it with a new fuse. Insert the cap and new fuse into the fuseholder with a clockwise twisting motion.

5.2.3 Lamp Replacement

Lamps for POWER, OFFSET, LOSS, and SYNC have polarized pin contacts and are mounted in lamp holders. To replace any of these lamps except POWER, pull the defective lamp from the lamp holder and then insert the new lamp, being careful that the lamp pins align with the lamp holder contacts before pushing the new lamp completely into the socket. Replace the POWER lamp in the manner just described with the following exceptions: first unscrew the plastic cap that secures the lamp into the lamp holder and then, after the new lamp is replaced, replace the plastic cap. Lamps for NRZ, BiØ, DM, RZ, L, M and S are mounted in the front panel without a lamp holder. To remove any of these lamps, pull the socket from the rear of the lamp and then, with a pair of long nose pliers, squeeze and remove the retaining clamp from the lamp. Pull the lamp through the front of the panel. Insert the new lamp through the panel. Install the retaining clamp to secure the lamp to the panel and then replace the lamp socket, being careful that the lamp pins align with the socket contacts before pushing the socket completely onto the lamp.

5.3 CORRECTIVE MAINTENANCE

Corrective maintenance includes the minimum performance standards, the test and adjustment procedures, troubleshooting information, and repair instructions. The minimum performance standards are used periodically as specified in the preventive maintenance schedule, table 5-1, and also whenever it is suspected that the bit synchronizer is not operating within specifications. If the bit synchronizer does not provide the minimum performance standards, use, as required, the test and adjustment procedures, troubleshooting information and repair instructions to correct the malfunction. After correcting the discrepancy, repeat the procedure for the minimum performance standards. Table 5-2 provides a complete operational check for the bit synchronizer.

Table 5-2. Minimum Performance Standards

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
1	Digital Multimeter, Fluke Model 8050A, or equivalent	Power Supply tests: a. Connect multimeter across terminals labeled + and C on power supply PS1 ±15 volt terminal strip. NOTE Refer to Appendix A for power supply adjustments and troubleshooting procedures.	+15 ±0.1 vdc. If necessary, adjust power (See Note).
		b. Connect multimeter across terminals labeled - and C on power supply PS1 ±15 volt terminal strip.	-15 ±0.1 vdc. If necessary, adjust power supply (see Note).
		c. Connect multimeter across terminals labeled +5V and 5V Return on power supply PS1 5 Volt terminal strip.	5 ±0.05 vdc. If necessary adjust 5 VOLT potentiometer on PS1 labeled +5 Adj. (see Note).
2	Frequency Counter, General Radio Model 1191, or equivalent.	Bit rate selector test: a. Connect frequency counter between 0° test point GND test point, both of which are on front panel.	
		b. Set BIT RATE multiplier thumbwheel to 10^6 and then, in turn, set first four BIT RATE thumbwheels to 1.000, 2.222, 4.444, 7.777 and 9.999. For each setting, observe frequency counter.	Frequency counter indicates within 0.1% of dialed bit rate.
		c. Set first four BIT RATE thumbwheels to 1.000 and then, in turn, set BIT RATE multiplier thumbwheel to 10^6 through 10^0. For each setting, observe frequency counter.	Same as above.

Table 5-2. Minimum Performance Standards (cont.)

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
3	Oscilloscope, Tektronix Model 547 & Type 1A2 Preamp; MONITOR Bit Error Rate Test Set Model 852B, or equivalent.	Code Conversion Checkout a. Connect as shown in figure 5-1. b. Set Model 852B as follows: (1) PATTERN to PRN-N. (2) NOR/INV to NOR. (3) BIT RATE to 5.000 x 10^5 (4) DATA CODE to NRZL (5) BLANK to OFF. (6) CLOCK to NORM. (7) BIT ERRORS to A (Accumulate). (8) INS ERR to OFF. (9) LOOP to OFF. (10) OFFSET to OFF. (11) NOISE to OFF. (12) DATA to HI. (Set output for 2 volts p-p of output data test point.) c. Set bit synchronizer controls as follows: (1) BIT RATE to 5.000 x 10^5 (2) CODE to NRZ-L. (3) SOURCE to position 1. (4) LOOP BAND to position 1. (5) POLARITY to +. (6) MANUAL/PROGRAM to MANUAL. d. Repeat steps b and c for each of the standard IRIG codes.	Observe that Model 852B SYNC indicator is lit. Depress Model 852B RESET switch and verify that no bit errors are displayed. The bit synchronizer shall convert all input codes to NRZ-L code without error.

Table 5-2. Minimum Performance Standards (cont.)

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
4	Oscilloscope, Tektronix Model 547 & Type 1A2 Preamp; MONITOR Bit Error Rate Test Set Model 852B, or equivalent.	AGC and offset correction circuits checkout a. Connect as shown in figure 5-1. b. Set Model 852B as follows: (1) 48 BIT PATTERN: word 1 to 10111011 word 2 to 00011111 word 3 to 00110100 word 4 to 10001001 word 5 to 11110101 word 6 to 00011110 (2) NOR/INV to NOR. (3) BIT RATE to 5.000 x 10^5. (4) DATA CODE to NRZL. (5) BLANK to OFF. (6) CLOCK to NORM. (7) BIT ERRORS to A (accumulate). (8) INS ERR to OFF. (9) LOOP to OFF. (10) OFFSET to OFF. (11) NOISE to OFF. (12) DATA to HI. c. Set bit synchronizer as follows: (1) BIT RATE to 5.000 x 10^5. (2) CODE to NRZ-L. (3) SOURCE to position 1. (4) LOOP to position 3. (5) POLARITY to +. (6) MANUAL/PROGRAM to MANUAL. d. Set oscilloscope sync to trigger from Model 852B SYNC test point.	

Table 5-2. Minimum Performance Standards (cont.)

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
4 (cont.)		e. Observe the Model 852B DATA OUTPUT test point on oscilloscope trace #1, and the bit synchronizer AGC'ed signal at card location A1A3TP1 on oscilloscope trace #2 while varying the Model 852B output between 0.5 V and 10 V p-p.	#2 channel shall remain at a constant 1.0V p-p, centered about ground, throughout the entire test.
		f. Turn Model 852B OFFSET control on.	
		g. Adjust Model 852B OFFSET and DATA level controls as follows, while observing signal on oscilloscope trace #1: (1) Set output level for 1.0V p-p centered about ground. (2) Adjust dc offset for +1.0V (signal varies from +0.5 to 1.5V). (3) Adjust dc offset for -1.0V (signal varies from -0.5 to -1.5V).	#2 channel shall remain at a constant 1.0V p-p, centered about ground. throughout the entire test.
		h. Reduce the bit synchronizer BIT RATE to 5.000×10^3. Repeat steps d, e, f, and g, observing the bit synchronizer's AGC'ed signal at card A1A1TPZ. (Note that pc card VAF027 must be placed on an extender. TPZ is a turret lug located between IC U1 and IC U8 on the lower left of the card.)	#2 channel shall remain at approx. 1.0V p-p centered about ground, throughout the entire test.

Table 5-2. Minimum Performance Standards (cont.)

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
5	Oscilloscope, Tektronix Model 547, MONITOR Bit Error Rate Test Set 852B; Noise Generator Elgenco Model 610A; Reference Filter Krohn-Hite Model 3202R; Frequency Counter Hewlett Packard Model 5245L; RMS Voltmeter Hewlett Packard Model 3400A; or equivalent.	Jitter Performance test a. Connect as shown in figure 5-1. b. With Model 852B controls set as described in step 4-b, make the following changes: (1) BIT RATE to 1.000×10^5. (2) CLOCK to JITTER. c. Set bit synchronizer as follows: (1) BIT RATE TO 1.000×10^5. (2) CODE to NRZ-L. (3) SOURCE to position 1. (4) LOOP to position 3. d. With scope trace #1 connected to the Model 852B at J10, set oscilloscope as follows: (1) TRIGGER on channel #1. (2) Calibrate for one full cycle of clock per 10 cm. or full scale. NOTE Each centimeter is equal to 10% peak jitter when measured from center of trace; left edge of trace remains steady. e. Using the frequency counter, make the following connections: from the bit synchronizer clock output to the counter input; and from the Model 852B clock output to the external standard frequency on the counter's rear panel.	

Table 5-2. Minimum Performance Standards (cont.)

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
5 (cont.)		f. Set the frequency counter controls as follows: (1) FUNCTION to FREQUENCY. (2) TIME BASE to .1 sec. (3) MODE TO EXT STD FREQ. g. Observe that the frequency counter displays 1000.000 when no jitter is present. h. Set function generator to sine wave. Slowly increase the amplitude of the sine wave at various frequency rates (generally 0.1%, 0.2%, 0.5%, 1%, 2%, 5% and 10% of the operating bit rate). Observe the frequency counter display at the point where it no longer displays 1000.000. Note the magnitude of the jitter displayed on the oscilloscope. i. Compare each reading with the Nominal Jitter Performance Curve (figure 5-2).	Jitter performance should not be worse than that plotted in figure 5-2.
6	Oscilloscope, Tektronix Model 547; MONITOR Bit Rate Test Set 852B; Noise Generator Elgenco Model 610A; Reference Filter Krohn-Hite Model 3202R; Frequency Counter Hewlett Packard Model 5245L; RMS Voltmeter Hewlett Packard Model 3400A; or equivalent.	Bit Error Probability (BEP) performance check a. Connect as shown in figure 5-1. b. Set Model 852B as follows: (1) PATTERN to PRN-N. (2) NOR/INV to NOR. (3) BIT RATE to 5.000×10^5.* (4) DATA CODE to NRZ-L.* (5) BLANK to OFF. (6) CLOCK to NORM.	

Table 5-2. Minimum Performance Standards (cont.)

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
6 (cont.)		(7) BIT ERRORS to A (accumulate).* (8) INS ERR to OFF. (9) LOOP to OFF. (10) OFFSET to OFF. (11) NOISE to ON. (12) DATA to HI. Set output at DATA test point for 1.0V p-p. c. Set bit synchronizer as follows: (1) BIT RATE to 5.000 x 10^5.* (2) CODE to NRZ-L.* (3) SOURCE to position 1. (4) LOOP to position 3. (5) POLARITY to +. *These settings are for reference only. Parameters may be varied as desired when checking BEP. d. Signal-to-noise (S/N) ratio calibration is made as follows: (1) Set the reference filter to low pass mode and adjust the frequency response to read one-half the bit synchronizer operating rate (in this case, 250 kHz). (2) Set the noise generator to maximum; set the bandwidth "Range" adjustment so that sufficient band noise is applied to the bit synchronizer, generally five times the bit rate. (3) Make the following changes on the Model 852B. (3.1) Turn NOISE switch to OFF.	

Table 5-2. Minimum Performance Standards (cont.)

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
6 (cont.)		(3.2) Turn the BIT RATE down by one decade, and note the amplitude reading on the RMS meter. Adjust the Model 852B DATA LEVEL control slightly so that a good db reference point can be used. (3.3) Return the BIT RATE decade switch to the original rate. (Note that the meter reading is slightly less. This is normal.) Turn off data by switching the Model 852B CLOCK switch to EXT, if no external clock is applied to the unit. (3.4) Turn NOISE to ON. Adjust the NOISE LEVEL control until the RMS meter reading is exactly 12 db below the reference point taken in step 3.2. The S/N ratio is now 12 db.	
		e. To measure BEP, switch the Model 852B CLOCK to NORM. Note that the bit synchronizer and Model 852B show sync lock. (1) Set Model 852B BIT ERRORS x 10 switch to "5". (2) Depress RESET switch. CIP lamp will light for the duration of the test. The BEP reading should be no greater than 18×10^{-5}.	BEP shall be within 1 db of ideal performance. Refer to figure 5-3. (See Note).
		f. Repeat BEP performance check for various bit rates, codes and S/N ratios.	BEP shall be within 1 db of ideal performance. Refer to figure 5-3. (See Note).

Table 5-2. Minimum Performance Standards (cont.)

STEP	TEST EQUIPMENT	PROCEDURE	MINIMUM ACCEPTABLE PERFORMANCE
		NOTE Following are examples of BEP for various S/N ratios. Use in conjunction with figure 5-3.	

S/N	THEORETICAL	S/N TOLERANCE
12 db	3.0×10^{5}	1.8×10^{4}
9 db	2.7×10^{3}	6.0×10^{3}
6 db	2.0×10^{-2}	3.25×10^{-2}
3 db	7.0×10^{-2}	9.4×10^{-2}
0 db	1.6×10^{-1}	1.9×10^{-1}

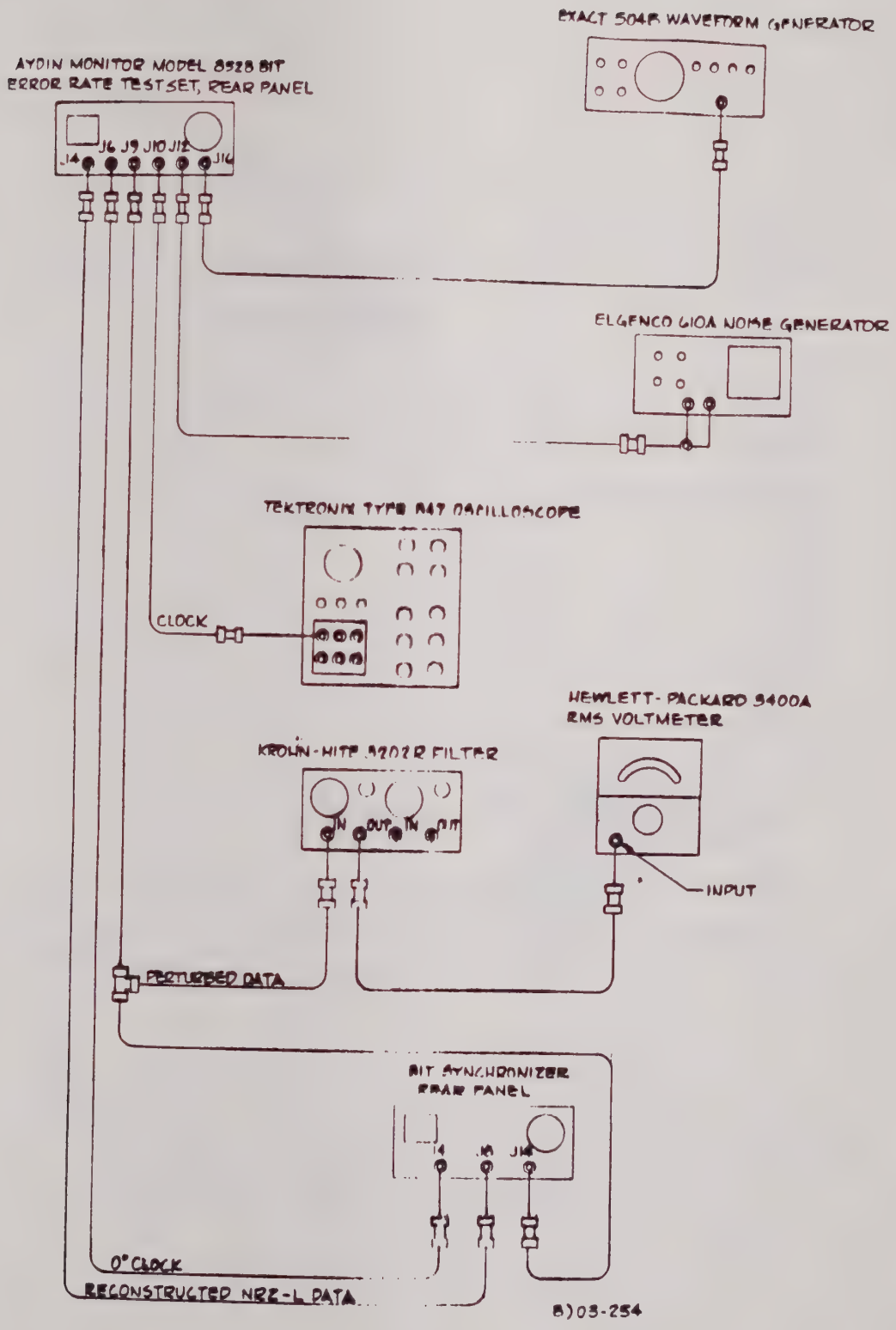


Figure 5-1. Bit Synchronizer, Test Setup Interconnection Diagram

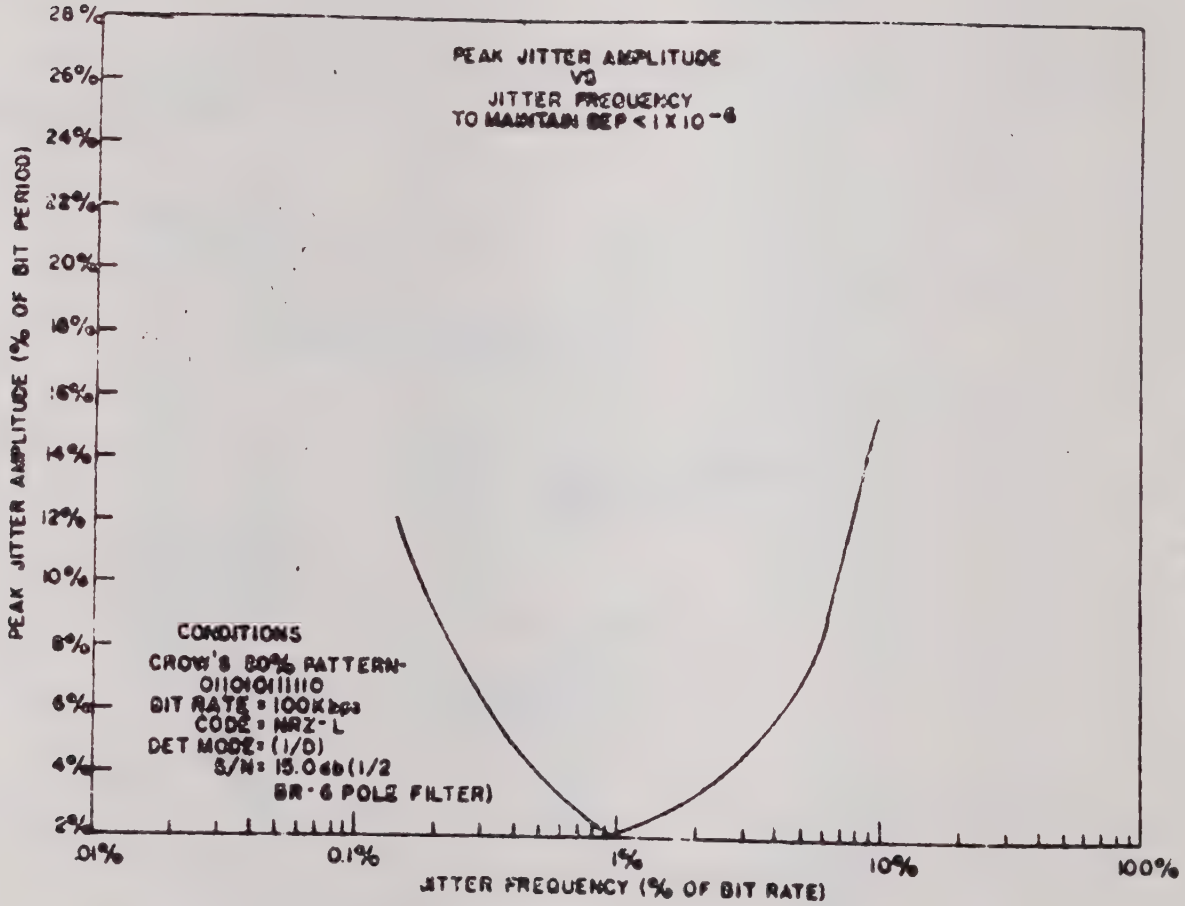


Figure 5-2. Nominal Jitter Performance Curve

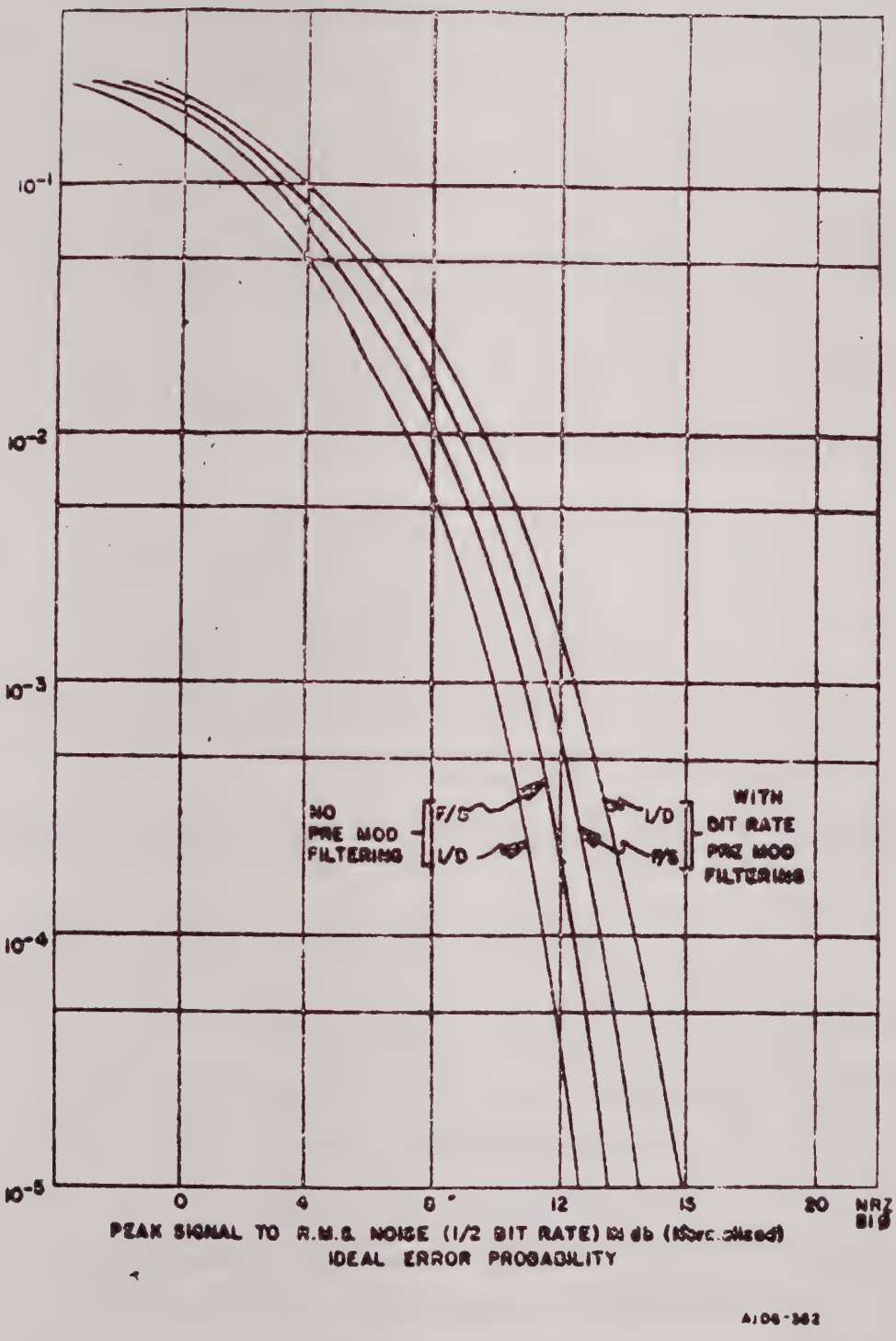


Figure 5-3. Error Probability Curves

5.4 TEST AND ADJUSTMENT PROCEDURES

Test and adjustment procedures are given in the following paragraphs for each circuit that contains an adjustable part (potentiometer or variable capacitor) or a select-by-test (SBT) resistor. These circuits include the test point driver, variable gain amplifier, low frequency matched filter, low frequency tracking loop filter, loop deviation meter driver circuit, delta current generator and tape records output circuits. Both the adjustments and selection of SBT resistors are factory set and normally do not require subsequent adjustment or change unless the adjustable or selectable part or a part closely associated with the adjustable or selectable part is replaced. Further, properly adjusted pc cards either from spares or from another bit synchronizer can be interchanged with identical type pc cards of the bit synchronizer without additional adjustment or selection of SBT resistors. Therefore, do not change a preset adjustment or select a new SBT resistor unless the observed indication given in the test portion of each adjustment procedure is not within the specified tolerance.

CAUTION

All internal adjustments are factory preset. Adjust only after replacing defective electrical component on printed circuit card and then adjust only the card involved.

5.4.1 Preliminary Procedures

Before performing any of the following test and adjustment procedures, prepare the bit synchronizer as follows:

a. Remove top cover to gain access to pc cards.

b. Ensure power cable is connected between bit synchronizer and ac source.

c. Set POWER switch to ON position.

d. Set POLARITY switch to + position.

e. Set INPUT CODE switch to NRZ-L.

f. Set LOOP BAND switch to 1 position.

g. Set MANUAL/PROGRAM switch to MANUAL position.

h. Set BIT RATE thumbwheels to 1.000×10^3.

i. Set OUTPUT DATA switch to NRZ-L position.

j. Set SOURCE switch to 1.

k. Unless otherwise specified, do not connect an input signal to the bit synchronizer.

5.4.2 Adjustment of Test Point Driver

To adjust the test point driver, perform the preliminary procedures given in paragraph 5.4.1, and then proceed as follows:

a. Place type SLC029 pc card, A1A2, on card extender and then connect two jumpers. Connect one between pin 27 and ground and the other between pin 28 and ground. Also, jumper a short across resistors R218 and R219 for this procedure.

b. Connect cable between high impedance output of square wave generator and input source no. 1 connector, J14, of bit synchronizer.

c. Connect oscilloscope probe (1 to 1 and dc coupled) to pin 35 of SLC029.

d. Set oscilloscope for time base of 5 microseconds/cm and amplitude of 1 volt/cm.

e. Adjust square wave generator for an output of 100 kHz at 3 volts p-p as observed on oscilloscope.

f. Change oscilloscope probe to pin 37. Waveform should be a true rectangular wave. If waveform has overshoots or rounding, adjust C3 to obtain true rectangular wave.

g. Waveform must be 1 volt p-p and symmetrical about zero volts (zero offset). If necessary, adjust R13 to obtain zero offset.

5.4.3 Adjustment of Variable Gain Amplifier

To adjust the variable gain amplifier, perform the preliminary procedures given in paragraph 5.4.1 and then proceed as follows:

a. Place type SLC029 pc card A1A2 on card extender and then connect two jumpers. Connect one between pin 27 and ground and the other between pin 28 and ground. Also jumper a short across resistors R218 and R219.

b. Set BIT RATE thumbwheels to 1.000×10^4.

c. Connect cable between high impedance output of square wave generator and input source no. 1 connector, J14, of the bit synchronizer.

d. Connect oscilloscope channel A probe (1 to 1 and dc coupled) to pin 35 of SLC029.

e. Connect oscilloscope channel B probe (1 to 1 and dc coupled) to TP1 of VAF026, A1A3.

f. For channel A of the oscilloscope, set time base to 0.2 millisecond/cm and amplitude to 0.5 volt/cm. For channel B, set time base to 0.2 millisecond/cm and amplitude of 1 volt/cm.

g. Set square wave generator to 5 kHz and then adjust its amplitude to provide a 0.5 volt p-p signal, centered about ground on channel A of the oscilloscope.

h. The waveform on channel B of the oscilloscope should be identical to that on channel A. If it is not, use the following steps to select a new value for R60.

i. Remove R60. Obtain a 100k potentiometer and adjust the wiper arm so that it is in the approximate center of its range.

j. Connect the potentiometer (center and one end) across terminals from which R60 was removed.

k. Adjust the potentiometer until waveforms on channel A and B of oscilloscope are identical.

l. Without disturbing the setting of the potentiometer, remove the potentiometer and then measure the resistance that was between the terminals of the card.

m. Select a resistor whose value is the same as, or slightly less than, the value of the measured resistance. A typical value for the selected resistor is 68k ohms.

n. Install the selected resistor and then ensure that channel B waveform has the same amplitude or slightly greater than the channel A waveform.

o. Disconnect cable between square wave generator and bit synchronizer.

p. Connect digital voltmeter between right side of R29 and top of R30.

q. Adjust R21 for minimum voltage as indicated on voltmeter. As voltage decreases towards zero, progressively change to lower voltage ranges to ensure R21 is set for absolute minimum offset, but equal offset between positive polarity and negative polarity.

r. Remove jumpers and replace pc cards.

5.4.4 Adjustment of Voltage Controlled Oscillator

To adjust the VCO, perform the preliminary procedures given in paragraph 5.4.1, and then proceed as follows:

a. Set switch S1 on type XTL028 pc card A2A2 to the OFF position.

b. Connect frequency counter to clock output connector J1.

c. Set BIT RATE thumbwheels to 6.000×10^4.

d. Place type ACL009 pc card, A1A11, on card extender.

e. Using a digital voltmeter, measure voltage between pin 32 and ground. Voltage must be -6.2 volts. If it is not, adjust R19 to obtain the proper voltage.

f. Observe frequency counter for an indicator of 60.000 kHz. If it does not so indicate, adjust R27 to obtain proper frequency.

g. Change BIT RATE thumbwheels to 5.999×10^4. Frequency counter should indicate between 61.800 and 58.200 kHz. If it does not, change SBT resistor R39 and repeat steps f and g. If the indicated frequency is above the specified range, increase the value of R39. If the indicated frequency is below the specified range, decrease the value of R39. Usually R39 is 2.7k ohms; occasionally, a 2.4k ohm or a 3.3k ohm resistor is required.

h. Return switch S1 on XTL028 pc card to the ON position.

5.4.5 Alignment of Low Frequency Matched Filter.

To align the low frequency matched filter, perform the preliminary procedures given in paragraph 5.4.1, and then proceed as follows:

a. Place type SLC029 pc card, A1A2, on card extender and then connect two jumpers. Connect one between pin 27 and ground and the other between pin 28 and ground. Also jumper a short across resistors R218 and R219.

b. Place type VAF027 pc card, A1A1, on card extender and then connect a jumper between TP-Z and ground.

c. On type VAF027 pc card (see schematic/assembly drawing 460-0908 for location of following potentiometers), set R31, R40 and R86 to their maximum counterclockwise position and set R77 to its maximum clockwise position.

d. Using a digital voltmeter, check for -4 ±1 vdc at pin 10 of U2, U4, U13 and U15. If proper voltage is not obtained, troubleshooting is necessary.

e. Set BIT RATE multiplier thumbwheel to 10^3.

f. Connect oscilloscope probe (dc coupled) to R bus (left side of C19). Oscilloscope should display a dc level. While observing oscilloscope, change BIT RATE thumbwheels between 9.999 and 1.000. If the dc level changes, proceed to the next step; otherwise, proceed to step h.

g. Adjust potentiometer R9 for minimum change of the dc level for bit rates of 9.999 and 1.000. R9 is properly adjusted when the dc level is 0 ±0.2 vdc for bit rates of 9.999 and 1.000.

h. Change oscilloscope probe to T bus (right side of C40). Oscilloscope should display a dc level. While observing oscilloscope, change BIT RATE thumbwheels between 9.999 and 1.000. If the dc level changes, proceed to the next step; otherwise, proceed to step j.

i. Adjust potentiometer R242 for minimum change of dc level for bit rates of 9.999 and 1.000. R242 is properly adjusted when both dc levels are between -2 and +2 vdc and the difference voltage between the two dc levels is no greater than 0.2 vdc.

j. If the dc level on T bus is other than zero volts, adjust R88 until zero volts is obtained.

k. Remove jumper that was installed for step b (between TP-Z and ground).

l. Connect cable between high impedance output of square wave generator and input source no. 1 connector, J14, of bit synchronizer.

m. Change oscilloscope probe to TP-Z and then set oscilloscope for time base of 0.2 millisecond/cm and amplitude of 0.5 volt/cm.

n. Adjust square wave generator for a frequency of 500 Hz. Adjust amplitude for 1 volt p-p as viewed on oscilloscope. Do not change generator amplitude control until alignment procedure is completed.

o. Connect oscilloscope channel A probe to TP2 and channel B probe to TP1. Set channels A and B oscilloscope for a time base of 0.2 milliseconds/cm and an amplitude of 1 volt/cm.

p. On bit synchronizer, set BIT RATE thumbwheels to 1.000 x 10^3.

q. Channels A and B waveforms should be identical and as shown in figure 5-4A; otherwise, adjust R31 until waveforms are identical.

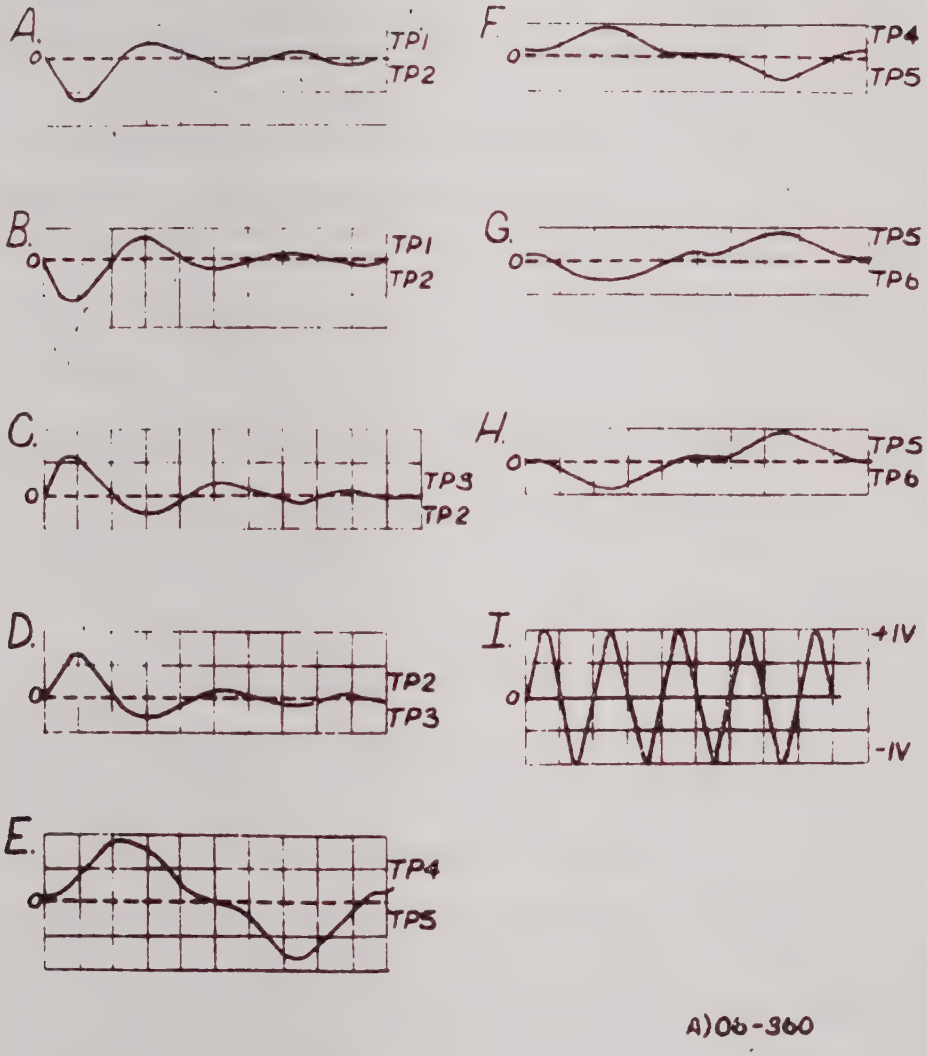


Figure 5-4. Alignment Waveforms for Low Frequency Matched Filter

r. On oscilloscope, change time base for channels A and B to 20 microseconds/cm and amplitude of channe B to 0.1 volt/cm.

s. Set square wave generator to 5000 Hz.

t. On bit synchronizer, set BIT RATE thumbwheels to 9.999×10^3.

u. Channels A and B waveforms should be identical and as shown in figure 5-4B; otherwise, adjust R36 until waveforms are identical.

v. Change channel B probe from TP1 to TP3.

w. On oscilloscope, change time base for channels A and B to 0.2 milliseconds/cm and change polarity of channel B from normal to inverted.

x. Set square wave generator to 500 Hz.

y. On bit synchronizer, set BIT RATE thumbwheels to 1.000×10^3.

z. Channels A and B waveforms should be identical and as shown in figure 5-4C; otherwise, adjust R40 until waveforms are identical

aa. On oscilloscope, change time base for channels A and B to 20 microseconds/cm and amplitude of channels A and B to 1 volt/cm. Also, leave polarity of channel B inverted.

ab. Set square wave generator to 5000 Hz.

ac. On bit synchronizer, set BIT RATE thumbwheels to 9.999×10^3.

ad. Channels A and B waveforms should be identical and as shown in figure 5-4D; otherwise, adjust R47 until waveforms are identical.

ae. Change channel B probe to TP4 and channel A probe to TP5.

af. On oscilloscope, change time base for channels A and B to 0.2 microseconds/cm and amplitude for channels A and B to 0.2 volt/cm. Return channel B to normal polarity.

ag. On bit synchronizer, set BIT RATE thumbwheels to 1.000×10^3; also change square wave generator to 500 Hz.

ah. Channels A and B waveforms should be identical and as shown in figure 5-4E; otherwise, adjust R77 until waveforms are identical.

ai. On oscilloscope, change time base for channels A and B to 20 microseconds/cm, change amplitude of channel A to 0.5 volt/cm and change amplitude of channel B to 0.05 volt/cm.

aj. Set square wave generator to 5 kHz.

ak. On bit synchronizer, set BIT RATE thumbwheels to 9.999×10^3.

al. Channel A and B waveforms should be identical and as shown in figure 5-4F; otherwise, adjust R82 until waveforms are identical.

am. Change channel B probe from TP4 to TP6.

an. On oscilloscope, change time base of channels A and B to 0.2 millisecond/cm. Also, change polarity on channel B to invert.

ao. Set square wave generator to 500 Hz.

ap. On bit synchronizer, change BIT RATE thumbwheels to 1.000×10^3.

aq. Channels A and B waveforms should be identical and as shown in figure 5-4G; otherwise, adjust R86 until waveforms are identical.

ar. On oscilloscope, change time base of channels A and B to 20 microseconds/cm and amplitude of channels A and B to 0.5 volts/cm.

as. Set square wave generator to 5 kHz.

at. On bit synchronizer, change BIT RATE thumbwheels to 9.999×10^3.

au. Channels A and B waveforms should be identical and as shown in figure 5-4H; otherwise, adjust R93 until waveforms are identical.

av. Connect oscilloscope probe to positive side of C46. Waveform should be as shown in figure 5-4I; if it is otherwise, repeat alignment procedure.

5.4.6 Adjustment of Low Frequency Tracking Loop Filter

To adjust the low frequency tracking loop filter, perform the preliminary procedures given in paragraph 5.4.1, and then proceed as follows:

a. Place type PLL102 pc card, A1A8, on card extender and then connect a jumper between terminals E1 and E2.

b. Set BIT RATE thumbwheels to 5×10^3.

c. Ensure AUTO-CAL lamp is lit; otherwise, troubleshooting is necessary.

d. Connect digital voltmeter between pin 14 and TP11 of A1A8.

e. Digital voltmeter should indicate 0 ±0.05 vdc. If it does not, adjust R19 until meter indicates zero volts.

f. Connect digital voltmeter between pin 14 and TP7 of A1A8.

g. Digital voltmeter should indicate 0 ±0.05 vdc. If it does not, adjust R18 until meter indicates zero volts.

h. Repeat steps d through g until no further adjustments of R18 and R19 are required.

5.4.7 Adjustment of Loop Deviation Meter Driver Circuit

To adjust the loop deviation meter driver circuit, perform the preliminary procedures given in paragraph 5.4.1, and then proceed as follows:

a. Set BIT RATE thumbwheels to 5.000×10^4.

b. LOOP DEVIATION meter should indicate exactly at 0 (null point). If it does not, proceed to next step.

c. On type HLF001 pc card, A1A7, adjust R20 until LOOP DEVIATION meter indicates 0 (null point).

5.4.8 Adjustment of Delta Current Generator

To adjust the delta current generator, perform the preliminary procedure given in paragraph 5.4.1, and then proceed as follows:

NOTE

Before adjusting the delta current generator, ensure the loop deviation meter driver circuit is properly adjusted. See paragraph 5.4.7.

a. Connect a noise generator adjusted to provide a 20 MHz bandwidth of noise to J14 (input source no. 1).

b. Set BIT RATE thumbwheels to 3.000×10^5.

c. Increase amplitude of input noise until AUTO-CAL indicator goes out.

NOTE

All potentiometers mentioned in the following steps are located on type PDT020 pc card, A1A6. (See schematic drawing 460-1058.)

d. LOOP DEVIATION meter should indicate 0 ±10. If it does not, adjust R71 until the meter indicates 0 (null point).

e. Change CODE switch to BiØ-L position.

f. LOOP DEVIATION meter should indicate 0 ±10. If it does not, adjust R144 until the meter indicates 0 (null point).

g. Change CODE switch to NRZ-L position and change BIT RATE thumbwheels to 2.000×10^6.

h. LOOP DEVIATION meter should indicate 0 ±10. If it does not, adjust R66 until the meter indicates 0 (null point).

i. Change CODE switch to BiØ-L position.

j. LOOP DEVIATION meter should indicate 0 ±10. If it does not, adjust R139 until meter indicates 0 (null point).

k. Change CODE switch to NRZ-L position and change BIT RATE thumbwheels to 4.000×10^6.

l. LOOP DEVIATION meter should indicate 0 ±10. If it does not, adjust R60 until the meter indicates 0 (null point).

m. Change CODE switch to BiØ-L position.

n. LOOP DEVIATION meter should indicate 0 ±10. If it does not, adjust R134 until meter indicates 0 (null point).

5.4.9 Adjustment of Tape Recorder Output Circuits

The NRZ and BiØ output circuits can be adjusted to provide PCM data with levels between 2 volts p-p and 6 volts p-p (all levels centered around zero volts) as required by the receiving equipment. To preset the output levels, perform the preliminary procedures given in paragraph 5.4.1, and then proceed as follows:

a. Connect a cable between the high impedance output of square wave generator and J14 (input source no. 1).

b. Adjust the square wave generator to provide a 25 kHz signal at 1 volt p-p.

c. Set BIT RATE thumbwheels to 5×10^4.

d. Connect oscilloscope to J9 (TR NRZ) output connector.

e. If output levels as viewed on oscilloscope are not as required, adjust R3 on type LDR024 pc card, A4A11.

f. Connect oscilloscope to J10 (TR BiØ) output connector. Output levels should be the same as those obtained in step e; if they are not, troubleshooting is required.

5.5 TROUBLESHOOTING INFORMATION

Troubleshooting information is presented in tabular form and provides a systematic procedure to locate a defective pc card when an abnormal indicator or symptom is known. The symptom usually is observed from malfunctions occurring during operation or when using the minimum performance standards. To use the troubleshooting procedures, preset the bit synchronizer as specified in the following instructions and then perform the applicable steps of the troubleshooting procedures given in table 5-3.

a. Set POWER switch to ON.

b. From a PCM simulator, connect a 10-bit frame sync pattern operating at frequencies specified in table 5-3 in NRZ-L code to SOURCE 1 input, J14. Set the pattern to 0010100101.

c. Set mode switch to MANUAL position.

d. Set POLARITY switch to + position.

e. Set SOURCE switch to 1 position.

f. Set BIT RATE switches to those frequencies specified in table 5-3.

g. Set LOOP BAND switch to 3 position.

5.6 REPAIR AND REPLACEMENT PROCEDURES

Procedures for the repair of pc cards and the removal and replacement of Varilok connector contacts are given in the following paragraphs.

5.6.1 Printed Circuit Card Repairs

PC card repairs, including the replacement of parts, are accomplished as follows:

a. To remove solder from a connection, dip a length of wire braid in liquid flux and place the braid over the solder joint; apply the soldering iron to the braid until it has soaked up the melted solder. Do this quickly and with a minimum of heating of the card pads.

b. After the solder has been removed from all of the connections, straighten the crimped ends of the leads on the back side of the card. Then, using a pair of suitable pliers, grasp the leads where they enter the holes on the component side of the card and slowly withdraw both ends at the same time to avoid bending the leads where they enter the part. If the part has several leads, first gently loosen each lead and then carefully pry the part from the card with a suitable tool such as a thin blade screwdriver. Be careful to avoid applying bending stresses to the part.

Table 5-3. Troubleshooting Procedures

STEP	SYMPTOM	PROBABLE CAUSE	TEST	NORMAL INDICATION	CORRECTIVE ACTION
1	No clock outputs	A. VCO inoperative.	Connect oscilloscope to A1A9 U23A pin 6.	Presence of high frequency VCO clock.	If clock is not present at A1A9 U23A-6, replace card A1A11 (ACL009); if clock is still not present, replace A1A9 (CSD002).
		B. Clock countdown logic/four phase generator defective.	Progressively connect oscilloscope to A1A9, pin 7, A1A9 pin 13, A1A9 pin 6, and A1A9 pin 12.	Presence of clock at each pin measured.	If clock is missing at any of the pins, replace card A1A9 (CSD002).
		C. Defective ϕ clock to degree clock conversion logic.	Progressively connect oscilloscope to A1A10 TP7 pin 15, pin 11, pin 13. Observe waveforms.	Presence of clock at each test point.	If clock is missing at any of the test points, replace card A1A10 (CCR056).
2	Output clock rate doesn't correspond to BIT RATE dial settings.	A. Malfunction in VCO.	Connect frequency counter to A1A9 U23A pin 6, measure frequency with BIT RATE set at 5.000 x 10^5 and SOURCE set to unused input.	Frequency of the clock at A1A9 U23A pin 6 should be 20 MHz $\pm$0.1%.	If frequency of clock is not correct within $\pm$0.1%, replace A1A11 (ACL009) and A2A2 (XTL028).

Table 5-3. Troubleshooting Procedures (cont.)

STEP	SYMPTOM	PROBABLE CAUSE	TEST	NORMAL INDICATION	CORRECTIVE ACTION
2 (cont.)		B. Malfunction in divide logic.	(1) Connect frequency counter to A1A9 pin 7 with BIT RATE set at 5.000×10^6, CODE set to NRZ-L, and SOURCE set to unused input.	Frequency of clock should be equal to dial setting.	If frequency of clock is not correct, replace A1A9 (CSD002).
			(2) Set MULTIPLIER to: 10^5 10^4 10^3 10^2 10^1 10^0	The frequency of clock should divide by ten from previous setting of multiplier.	
		C. Malfunction in Ø to degree clock conversion.	Connect oscilloscope to card A1A10 pin 15, with BIT RATE set at 5.000×10^5 and SOURCE set to unused input.	Frequency of clock at A1A10 pin 5, should be 500 kHz.	If frequency of clock is incorrect, replace A1A10 (CCR036).
3	No sync lock; sync lamp not lit.	A. Malfunction in phase lock loop circuitry.	(1) Connect oscilloscope to card A1A6 pin 26 and observe waveform with BIT RATE set at 5.000×10^5.	Signal at A1A6 pin 26 is as shown in figure 5-5A.	If signal is incorrect, replace card A1A6 (PDT020) and/or A1A7 (HLF001).

Table 5-3. Troubleshooting Procedures (cont.)

STEP	SYMPTOM	PROBABLE CAUSE	TEST	NORMAL INDICATION	CORRECTIVE ACTION
3 (cont.)			(2) Connect oscilloscope to card A1A6 pin 27 with BIT RATE set at 5.000 x 10^3.	Signal at A1A6 pin 27 is as shown in figure 5-5B.	
			(3) Connect oscilloscope to card A1A5 pin 11 and observe waveform. Set BIT RATE at 5.000 x 10^4.	Signal at A1A5 pin 11 is as shown in figure 5-5C.	
		B. Malfunction in AGC circuitry.	(1) Connect oscilloscope to card A1A3 TP1 and observe waveform (AGC and offset corrected signal).	Signal at A1A3 TP1 is as shown in figure 5-5D.	If signal is incorrect at A1A5 pin 11 and correct at A1A3 TP1, replace card A1A5 (THD001). If signal is incorrect at A1A3 TP1, proceed to troubleshooting AGC circuits.
			(2) Connect oscilloscope to card A1A5 pin 11 and observe waveform. Change BIT RATE to 5.000 x 10^3.	Signal at A1A5 pin 11 is as shown in figure 5-5E.	

Table 5-3. Troubleshooting Procedures (cont.)

STEP	SYMPTOM	PROBABLE CAUSE	TEST	NORMAL INDICATION	CORRECTIVE ACTION
3 (cont.)		C. Malfunction in AGC circuitry.	Connect oscilloscope to card A1A1 TERM Z and observe waveform (AGC and offset corrected signal).	Signal at A1A1 TERM Z is as shown in figure 5-5F.	If signal is incorrect at A1A5, pin 11 and correct at A1A1 TERM Z replace A1A5 (THD001). If signal is not correct at A1A1 TERM Z. proceed to trouble-shooting AGC circuits.
4	No data output. SYNC lamp off. LOSS lamp on.	A. Input signal level below minimum.	Connect oscilloscope to card A4A1 TP1 and observe waveform.	Signal amplitude must be greater then 0.5 volt p-p but less than 30 volt p-p.	Source of input signal must be adjusted until level falls within range of bit synchronizer.
		B. Defective level control circuitry.	(1) Connect oscilloscope to card A1A3 TP1 and observe waveform with BIT RATE set 5.000 x 10^4.	Signal at A1A3 TP1 is as shown in figure 5-5D.	Proceed to trouble shoot AGC circuits or replace cards A1A4 (SLC030), A1A2 (SLC029), A1A3 (VAF026), A1A5 (THD001), A1A10 (CCR036).
			(2) Connect oscilloscope to card A1A1 TERM Z and observe waveform. Change BIT RATE 5.000 x 10^3.	Signal at A1A1 TERM Z is as shown in figure 5-5F.	Proceed to trouble shoot AGC circuits or replace cards A1A2 (SLC029), A1A1 (VAF027), A1A10 (CCR036).

Table 5-3. Troubleshooting Procedures (cont.)

STEP	SYMPTOM	PROBABLE CAUSE	TEST	NORMAL INDICATION	CORRECTIVE ACTION
5	No Data output, SYNC lamp on, LOSS lamp off.	A. Defective bit detector circuitry.	(1) Connect oscilloscope to card A1A6 pin 8 and observe waveform with BIT RATE at 5.000 x 10^4.	Signal at A1A6 pin 8 is as shown in figure 5-5G.	If signal is incorrect replace card A1A5 (THD001).
			(2) Connect oscilloscope to card A1A6 pin 11 and observe waveform with BIT RATE at 5.000 x 10^4.	Signal at A1A6 pin 11 is as shown in figure 5-5H.	If signal is incorrect replace card A1A6 (PDT020).
			(3) Connect oscilloscope to card A1A6 pin 8 and observe waveform with BIT RATE at 5.000 x 10^3.	Signal at A1A6 pin 8 is as shown in figure 5-5I.	If signal is incorrect replace card A1A5 (THD001).
			(4) Connect oscilloscope to card A1A6 pin 11 and observe waveform with BIT RATE at 5.000 x 10^3.	Signal at A1A6 pin 11 is as shown in figure 5-5J.	If signal is incorrect replace card A1A6 (PDT020).

Table 5-3. Troubleshooting Procedures (cont.)

STEP	SYMPTOM	PROBABLE CAUSE	TEST	NORMAL INDICATION	CORRECTIVE ACTION
5 (cont.)		B. Defective code converter circuitry.	(1) Connect oscilloscope to card A1A10 TP6 and observe waveform with BIT RATE at 5.000 x 10^4.	Signal at A1A10 TP6 is as shown in figure 5-5K.	If signal is incorrect replace card A1A10 (CCR036).
			(2) Connect oscilloscope to card A1A10 pin 9.	Signal at A1A10 pin 9 is as shown in figure 5-5L.	If signal is incorrect replace card A1A10 (CCR036).
6	Bit sync fails to track input frequency changes (fails to handle jitter).	Malfunction in phase lock loop circuitry.	None	For multiplier settings of 10 and above, the bit synchronizer should track frequency changes.	In sequence, replace A1A7 (HLF001), A1A6 (PDT020), A1A11 (ACL009).
				For multiplier settings of 10^3 and below, the bit synchronizer should track frequency changes.	In sequence, replace A1A8 (PLL102), A1A7 (HLF001), A1A11 (ACL009).
7	Program set-up displays not lighted.	Malfunction in decoder/driver circuitry.	None	Display should light and indicate selected operating parameter.	If display fails to light, replace defective pc cards A2A3, (BCD001), A2A4, (PDC001), A3A3, (PSR021).

Table 5-3. Troubleshooting Procedures (cont.)

STEP	SYMPTOM	PROBABLE CAUSE	TEST	NORMAL INDICATION	CORRECTIVE ACTION
8	Remote program cannot be entered into bit synchronizer when in program mode	Malfunction in format decoder card.	(1) Connect VOM to card A3A5 U4 pin 12. Observe level . (Program correct unit address in program input lines).	Level present must be high (+5 volt) when proper unit address is applied to bit synchronizer program inputs.	If signal level at A3A5 TP7 is not as specified replace card A3A5 (DDR022).
			(2) Connect oscilloscope to card A3A5 U1 pin 10. Observe waveform. (Program in correct unit address plus a transfer pulse into program input lines).	A transfer pulse should be present going from a low to a high and back to a low.	If transfer pulse is not present, replace card A3A5 (DDR022).
9	Individual words cannot be entered into bit synchronizer when in program mode	A. Malfunction in format decoder card Word #1.	Connect VOM to card A3A5 pin 39 and observe signal level.	Level should be high (+5 volts) only when function address is XX00.	If level at A3A5, pin 39 is not high when function address is programmed into unit replace card A3A5 (DDR022).
		B. Malfunction in format decoder Card Word #2.	Connect VOM card A3A5, pin 31, and observe signal level.	Level should be high (+5 volts) only when function address is XX01.	If level at A3A5, pin 31 is not high when function address is programmed into unit replace card A3A5 (DDR022).

Table 5-3. Troubleshooting Procedures (cont.)

STEP	SYMPTOM	PROBABLE CAUSE	TEST	NORMAL INDICATION	CORRECTIVE ACTION
9 (cont.)		C. Malfunction in format decoder Card Word #3.	Connect VOM to card A3A5, pin 36 and observe signal level.	Level should be high (+5 volts) only when function address is XX10.	If level at A3A5, pin 36 is not a high when function address is programmed into unit replace A3A5 (DDR022).
		D. Malfunction in format decoder Card Word #4.	Connect VOM to card A3A5, pin 38 and observe signal level.	Level should be high (+5 volts) only when function address is XX11.	If level at A3A5, pin 38 is not a high when function address is programmed into unit replace A3A5. (DDR022)

TITLE LOOP ERROR PULSE

UPPER LOCATION A1A13 PIN 26

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 1 MICROSECOND /DIV.

UPPER VER. 0.1 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

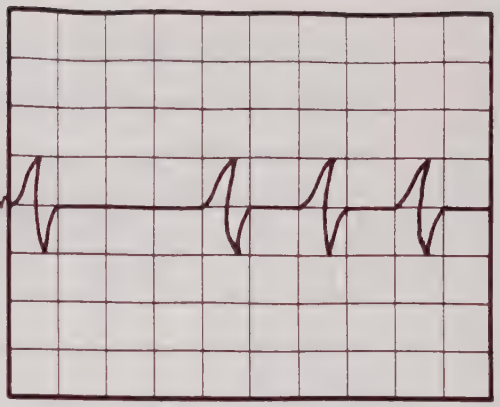


FIGURE A

TITLE LOOP ERROR PULSE

UPPER LOCATION A1A13 PIN 27

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 10 MICROSECONDS /DIV.

UPPER VER. 0.1 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

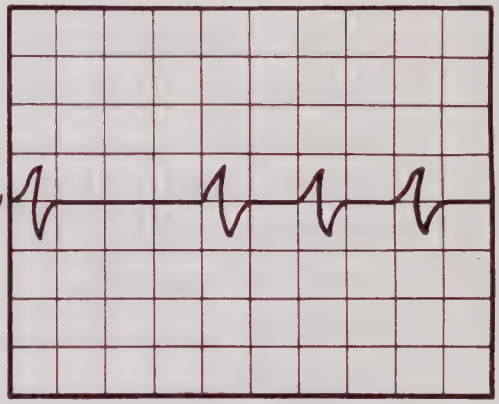


FIGURE B

TITLE U PULSE

UPPER LOCATION A1A12 PIN 11

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC PCM SIMULATOR

UPPER HOR. 10 MICROSECONDS /DIV.

UPPER VER. 0.5 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

800-0385

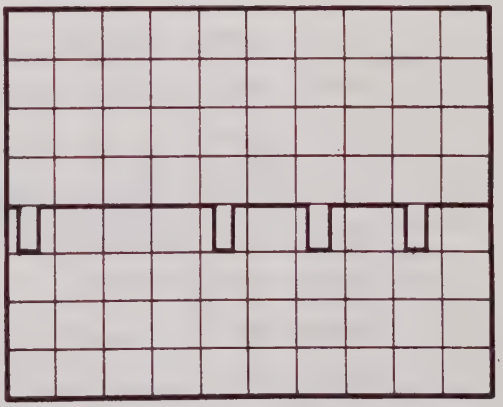


FIGURE C

Figure 5-5. Typical Waveforms for Troubleshooting Procedures (Sheet 1 of 4)

TITLE LEVEL CORRECTED SIGNAL

UPPER LOCATION A1A10 TP1

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 10 MICROSECONDS /DIV.

UPPER VER. 0.5 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

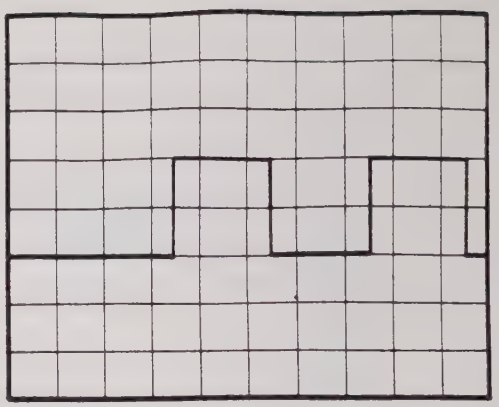


FIGURE D

TITLE U PULSE

UPPER LOCATION A1A12 PIN 11

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 100 MICROSECONDS /DIV.

UPPER VER. 0.5 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

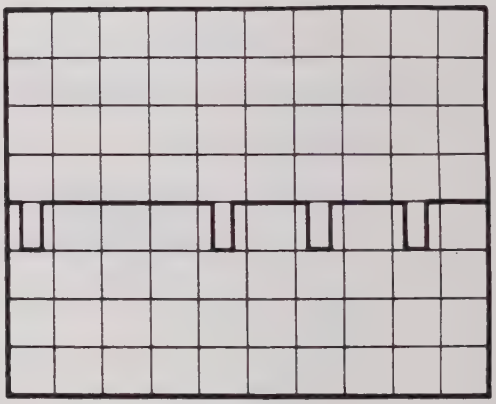


FIGURE E

TITLE LEVEL CORRECTED SIGNAL

UPPER LOCATION A1A8 TERM 8

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 100 MICROSECONDS /DIV.

UPPER VER. 0.5 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

800-0383

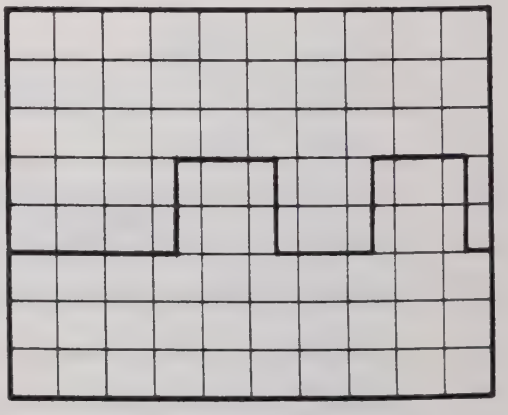


FIGURE F

Figure 5-5. Typical Waveforms for Troubleshooting Procedures (Sheet 2 of 4)

TITLE BIT DETECTOR

UPPER LOCATION A1A13 PIN 8

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 20 MICROSECONDS /DIV.

UPPER VER. 0.5 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

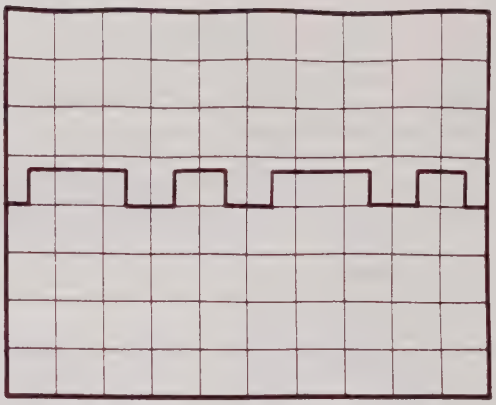


FIGURE G

TITLE BIT DETECTOR NRZ

UPPER LOCATION A1A13 PIN 11

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 20 MICROSECONDS /DIV.

UPPER VER. 0.5 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

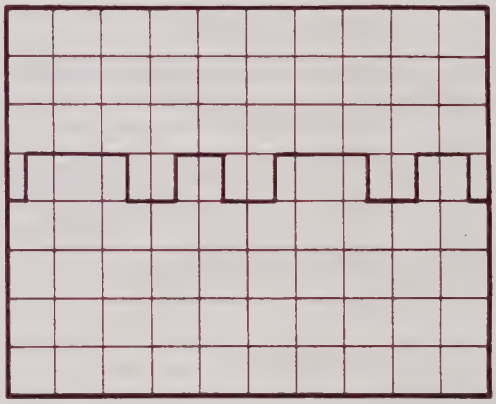


FIGURE H

TITLE BIT DETECTOR

UPPER LOCATION A1A13 PIN 8

LOWER LOCATION

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 200 MICROSECONDS /DIV.

UPPER VER. 0.5 VOLT /DIV.

LOWER HOR. /DIV.

LOWER VER. /DIV.

800-0385

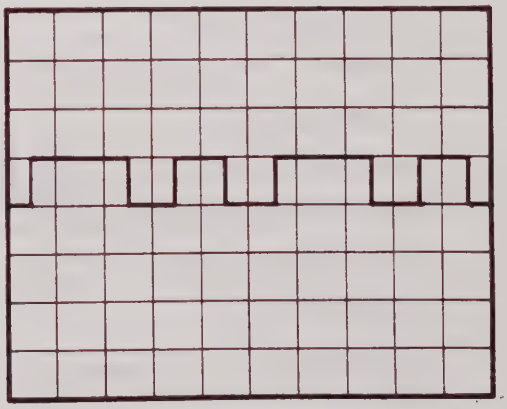


FIGURE I

Figure 5-5. Typical Waveforms for Troubleshooting Procedures (Sheet 3 of 4)

TITLE BIT DETECTOR NRZ

UPPER LOCATION A1A13 PIN 11

LOWER LOCATION _____

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 200 MICROSECONDS /DIV.

UPPER VER. 0.5 VOLT /DIV.

LOWER HOR. _____ /DIV.

LOWER VER. _____ /DIV.

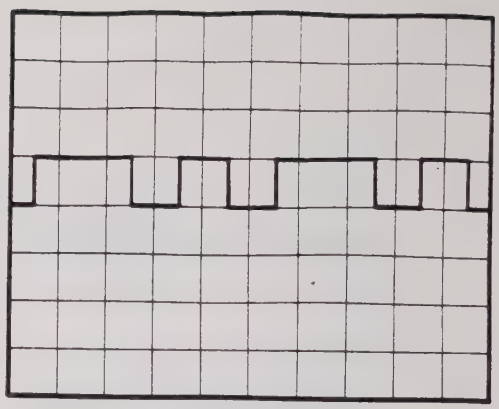


FIGURE J

TITLE BD NRZ

UPPER LOCATION A1A17 TRA

LOWER LOCATION _____

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 20 MICROSECONDS /DIV.

UPPER VER. 2 VOLTS /DIV.

LOWER HOR. _____ /DIV.

LOWER VER. _____ /DIV.

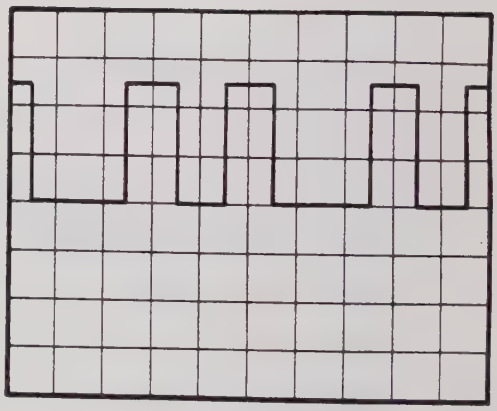


FIGURE K

TITLE NRZ-L DATA

UPPER LOCATION A1A17 PIN 9

LOWER LOCATION _____

EXTERNAL SYNC MAIN FRAME SYNC OF PCM SIMULATOR

UPPER HOR. 20 MICROSECONDS /DIV.

UPPER VER. 2 VOLTS /DIV.

LOWER HOR. _____ /DIV.

LOWER VER. _____ /DIV.

800-0385

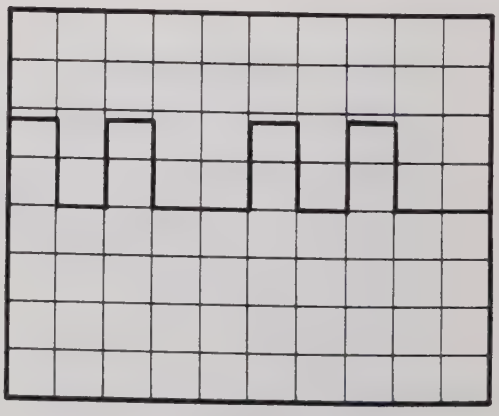


FIGURE L

Figure 5-5. Typical Waveforms for Troubleshooting Procedures (Sheet 4 of 4)

c. When replacing parts, if the leads must be bent, it is best to use bending jigs. Avoid bending radii less than twice the lead diameter. The bend must be at least 1/8 inch from the component end seal, or from the weld. Do not apply any bending stress to the part. The body of the part must contact the card. Whenever possible, the part lead must be bent flush against the metal on the circuit side of the card.

d. Apply the soldering iron to the junction of lead and base metal, contacting both. Use thermal shunts on the leads next to the part to protect it from thermal damage. Heat the connection quickly but thoroughly so that solder wets the metal and flows. Avoid overheating the card.

5.6.2 Removal and Replacement of Varilok Connector Contacts

All of the printed circuit connectors are Varilok, which have replaceable contacts. The removal and replacement procedure for these contacts are as follows:

a. Extraction of Varilok Contacts.

1. From top (card) side of connector, insert Varilok extraction tool so that its two prongs are on either side of contact to be removed.

2. Depress plunger of extraction tool as far as it will go.

3. From underside of connector, grasp protruding contact with long-nose pliers and remove it.

b. Crimping Wire in Varilok Contact.

1. Insert replacement contact in crimping pliers no. 067515-01 with open side of contact to the right.

2. Strip wire to expose 1/8 inch of bare conductor.

3. Insert wire into contact so that bare conductor is even with front edge of squared contact section.

4. Squeeze handles of crimping tool together until stop is reached and ratchet releases.

5. Release squeeze pressure on handles and remove wire and contact.

c. Insertion of Varilok Contacts.

1. Insert Varilok into polarized slot in connector.

2. Using long-nose pliers, place tips of pliers on either side of wire, against protruding crimped edge of contact.

3. Press contact firmly into connector until contact snaps into place.

5.7 MAINTENANCE DATA

Maintenance data contains the terminal voltages for each transistor, field effect transistor and integrated circuit used in the bit synchronizer. It also contains references to typical waveforms and diagrams which are required for maintenance of the bit synchronizer.

5.7.1 Terminal Voltages

Tables 5-4 through 5-19 give the voltage measurement of each transistor, field effect transistor (FET) and integrated circuit containing a transistor array used in the bit synchronizer. A separate table is provided for each pc card. For each transistor and FET, the voltage at each of its three elements is contained in the appropriate column opposite the reference designation of the transistor or FET, as applicable. Unless otherwise specified, all voltages are ±5 percent measured between specified terminal and digital ground and obtained under the following conditions:

a. All measurements are made with a Fluke Digital Voltmeter, Model 8100A or equivalent.

b. POWER switch set to ON position.

c. No signal input (LOSS lamp is lit and SYNC lamp is not lit).

d. POLARITY switch set to + position.

e. SOURCE switch set to 1 position.

f. CODE switch set to NRZ-L position.

g. LOOP BAND switch set to 1 position.

h. BIT RATE thumbwheels set to 1.000×10^5.

i. Mode switch set to MANUAL position.

j. Manual override selection switch set to OFF position.

5.7.2 Waveforms

The waveform tables contained in section IV and V can be used as maintenance data, particularly when isolating defective parts on pc cards. The tables are as follows:

a. Figure 4-8. Typical Waveforms Produced by Amplitude-and-Offset-Normalized NRZ type PCM.

b. Figure 4-29. Typical Waveforms of Code Converter when Processing NRZ-L type PCM.

c. Figure 4-30. Automatic Calibration Section, Typical Waveforms.

d. Figure 5-4. Alignment Waveforms for Low Frequency Matched Filter.

e. Figure 5-5. Typical Waveforms for Troubleshooting Procedures.

Table 5-4. Type VAF027 A1A1 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	3.83	2.08	0.00
Q2	1.40	2.07	0.53
Q3	0.40	1.09	1.00
Q4	1.40	1.09	0.00
Q5	5.87	0.23	6.23
Q6	5.87	0.07	0.00
FET Q7	0.00	0.00	0.00
FET Q8	0.00	0.00	0.00
FET Q9	0.00	0.00	0.00
FET Q10	0.00	0.00	0.00
FET Q11	0.00	0.00	0.00
FET Q12	0.00	0.00	0.00
FET Q13	0.00	0.00	0.00
FET Q14	0.00	0.00	0.00
FET Q15	0.00	0.00	0.00
FET Q16	0.00	0.00	0.00
FET Q17	0.00	0.00	0.00
FET Q18	1.55	1.55	1.55
FET Q19	-15.00	1.78	1.55
Q20	-15.00	-15.00	1.55
Q21	-14.3	-15.00	-15.00
Q22	1.55	0.71	-15.00
Q23	0.08	0.71	-14.3
Q24	-4.8	-5.4	-1.4
Q25	-0.33	-0.93	15.00
Q26	-0.39	-1.00	15.00
Q27	-0.37	-1.00	15.00
Q28	-0.47	-1.00	15.00
Q29	-0.49	-0.98	15.00
Q30	6.18	0.30	0.00
Q31	5.64	0.30	1.53
Q32	15.00	14.75	0.30
Q33	-0.37	-0.95	15.00
Q34	0.00	0.67	-4.30
Q35	1.13	0.67	-5.68
FET Q36	0.00	0.00	0.00
U7 - Q1	-7.28	-7.28	-7.28
U7 - Q2	-6.76	-7.28	-6.76
U7 - Q3	-6.23	-6.76	0.00
U7 - Q4	-7.28	-7.78	-6.23
U7 - Q5	-7.28	-7.78	-7.28

Table 5-4. Type VAF027 A1A1 PC Card, Voltage Measurements (cont)

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
U21-Q1	-0.43	IC	10.07
U21-Q2	-5.74	-6.49	IC
U21-Q3	-0.45	IC	10.07
U21-Q4	1.24	IC	9.47
U21-Q5	-5.73	-6.48	IC
U21-Q6	1.24	IC	9.47
U22-Q1	-7.96	-8.67	-2.81
U22-Q2	-8.67	-9.10	-3.25
U22-Q3	0.00	-0.71	7.34
U22-Q4	-0.12	-0.80	7.54
U22-Q5	-7.96	-8.67	-7.96
U32-Q1	-0.42	IC	10.07
U32-Q2	-5.87	-6.63	IC
U32-Q3	-0.49	IC	6.10
U32-Q4	1.24	IC	5.50
U32-Q5	-5.87	-6.63	IC
U32-Q6	1.24	IC	9.49
U33-Q1	-1.07	IC	+6.20
U33-Q2	-4.95	-5.72	IC
U33-Q3	-0.18	IC	6.20
U33-Q4	-0.20	IC	5.61
U33-Q5	-6.40	-5.72	IC
U33-Q6	0.61	IC	5.61
U34-Q1	-0.42	IC	6.16
U34-Q2	-5.74	-6.49	IC
U34-Q3	-0.40	IC	10.06
U34-Q4	1.22	IC	9.46
U34-Q5	-5.74	-6.49	IC
U34-Q6	1.23	IC	5.54

IC is Internal Connection

Table 5-5. Type SLC029 A1A2 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	1.07	0.45	14.9
Q2	-1.1	-0.47	-14.9
Q3	11.7	1.07	12.3
Q4	0.00	0.60	-14.9
Q5	0.00	-0.65	14.9
Q6	-11.75	-12.4	-1.10
Q7A	5.05	5.75	0.00
Q7B	5.08	5.76	4.46
Q8	4.46	5.08	0.00
Q9	12.55	11.87	15.00
Q10	1.52	3.03	5.92
Q11	3.70	3.03	4.29
Q12A	11.41	12.15	8.84
Q12B	11.41	12.15	8.90
Q13	8.73	8.76	0.00
Q14	8.10	8.76	7.01
Q15	8.10	8.76	7.02
Q16	9.73	8.76	0.21
Q17	-4.49	-5.10	0.00
Q18A	0.00	0.65	-4.49
Q18B	0.00	0.65	-3.14
Q19	1.54	3.09	9.73
Q20	3.75	3.09	8.10
Q21	-5.95	-6.56	-1.96
Q23	9.67	10.31	0.00
Q24	9.97	10.31	0.00
Q25	9.97	10.31	0.00
Q26	9.65	10.31	3.38
Q27	0.00	3.35	3.35
Q28	0.00	0.00	0.00
Q29	0.00	0.00	0.48
Q30	-0.13	0.49	-15.00
Q31	0.12	-0.51	15.00
Q32	0.00	0.00	0.49
Q33	0.00	0.00	-0.51
Q34	0.57	1.26	1.22
Q35	1.61	2.28	0.56
Q36	-0.74	0.00	0.00
Q37	0.52	0.00	0.00
Q38	0.00	0.00	0.00
Q39	1.61	2.29	0.56

Table 5-5. Type SLC029 A1A2 PC Card, Voltage Measurements (cont)

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q40	3.78	2.29	-12.39
Q41	-11.82	0.00	0.00
Q42	0.00	0.00	0.00
Q43A	14.31	14.98	14.31
Q43B	14.21	14.86	10.15
Q44A	9.59	-3.74	10.14
Q44B	9.51	0.31	10.14
Q45	6.85	7.36	0.00
Q46	6.67	7.36	3.11
Q47	0.00	-0.63	6.67
Q48	0.57	0.00	14.21
Q49	0.57	0.00	0.57
Q50	-12.7	0.31	0.00
Q52	0.08	-0.38	-13.17
Q53	0.26	-0.38	5.00
Q54	0.00	2.07	2.07
Q55	-2.15	0.00	0.00
Q56	1.75	0.00	0.00
Q57	0.00	0.27	0.49
Q58	-0.75	0.00	0.00
Q59	0.05	0.00	-0.51
Q60	0.57	1.27	1.24
Q61	1.63	2.30	0.56
Q62	1.62	2.31	0.56
Q63	3.77	2.31	-12.46
Q64	0.00	0.00	0.00
Q65	-11.89	0.00	0.00
Q66	0.00	0.00	0.00
Q67	9.97	10.32	0.00
Q68	9.65	10.32	3.98
Q69	9.97	10.35	0.00
Q70	9.68	10.35	3.23
U1- Q1	5.92	5.17	11.41
U1- Q2	4.26	5.17	11.55
U1- Q3	5.90	5.17	11.42
U1- Q4	4.24	5.17	11.42
U1- Q5	0.69	0.00	0.69
U2- Q1	0.00	-0.76	4.77
U2- Q2	0.00	-0.76	4.77
U2- Q3	0.00	0.69	0.00
U2- Q4	0.00	0.69	0.00

Table 5-5. Type SLC029 A1A2 PC Card, Voltage Measurements (cont)

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
U2- Q5	-6.16	-6.92	0.00
U3- Q1	-5.10	-5.78	-0.72
U3- Q2	-5.11	-5.78	-0.72
U3- Q3	-5.11	-5.78	-4.49
U3- Q4	-5.11	-5.78	-4.44
U3- Q5	-5.94	-5.94	-5.94
U4- Q1	-3.14	-3.91	-1.13
U4- Q2	-3.14	-3.91	-1.13
U4- Q3	0.00	-0.71	11.42
U4- Q4	0.00	-0.71	11.42
U4- Q5	-5.17	-5.94	-5.17
U11-Q1	8.47	7.75	14.78
U11-Q2	6.73	7.75	14.78
U11-Q3	7.50	6.85	14.78
U11-Q4	-3.74	-4.31	0.32
U11-Q5	-3.74	-4.31	-3.74

Table 5-6. Type VAF026 A1A3 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	6.04	6.69	-5.12
Q2	6.04	6.69	0.00
Q4	12.57	13.20	0.00
Q5	0.00	-0.64	12.57
Q6	0.00	-0.64	0.00
Q7	0.00	0.64	-12.6
Q8	0.00	0.64	0.00
Q9	-12.6	-13.2	0.00
Q10	12.56	13.9	0.00
Q11	0.00	-0.63	12.56
Q12	0.00	-0.63	0.00
Q13	-1.24	-0.59	-15.00
Q14	2.10	2.10	15.00
Q15	1.96	1.29	5.00
Q16	1.60	0.94	5.00
Q17	0.00	0.65	-12.57
Q18	0.00	0.65	0.00
Q19	-12.57	-13.19	0.00
Q20	12.53	13.13	0.00
Q21	0.00	-0.63	12.53
Q22	0.00	-0.63	0.00
Q23	12.30	12.98	9.82
Q24A	8.86	9.60	6.74
Q24B	8.88	9.61	6.72
Q26	1.76	1.10	5.00
Q27	1.80	1.17	5.00
Q29	+14.89	14.59	2.01
Q31	0.00	0.80	14.89
Q32	1.45	0.80	12.00
Q33	-7.42	-8.05	0.80
Q34	12.00	12.68	9.91
Q35A	8.94	9.68	6.79
Q35B	8.94	9.68	6.81
U10-Q1	-6.58	-6.58	-6.58
U10-Q2	-5.84	-6.58	-5.84
U10-Q3	-5.11	-5.84	0.00
U10-Q4	-6.59	0.00	0.00
U10-Q5	-6.87	-7.61	-6.87
U11-Q1	11.12	10.35	14.18
U11-Q2	11.12	10.35	14.18
U11-Q3	0.77	0.00	8.87

Table 5-6. Type VAF026 A1A3 PC Card, Voltage Measurement (cont)

TRANSISTOR/ FET	BASE/ GATE	EMITTER SOURCE	COLLECTOR/ DRAIN
U11-Q4	0.77	0.00	8.86
U11-Q5	0.77	0.00	0.77
U12-Q1	11.12	10.38	14.15
U12-Q2	11.12	10.38	14.15
U12-Q3	0.74	0.00	8.87
U12-Q4	0.74	0.00	8.85
U12-Q5	0.74	0.00	0.74
U13-Q1	11.18	10.43	14.16
U13-Q2	11.18	10.43	14.16
U13-Q3	0.75	0.00	8.95
U13-Q4	0.75	0.00	8.94
U13-Q5	0.75	0.00	0.75

Table 5-7. Type SLC030 A1A4 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	-0.60	0.00	-14.2
Q2	-0.60	0.00	-0.60
Q3	-0.60	0.00	-14.2
Q4	2.16	2.78	-14.92
Q5	9.68	10.35	2.16
Q6	10.09	10.35	0.95
Q7	9.69	10.35	2.06
Q8	10.09	10.35	0.26
Q9	0.57	1.23	-6.22
Q10	2.15	1.23	-6.66
Q11	2.14	1.23	-6.66
Q12	5.65	0.26	0.00
Q13	5.08	0.26	0.00
Q14	5.66	1.00	0.00
Q15	5.08	0.96	0.00
Q16A	14.34	15.00	14.34
Q16B	14.16	14.81	5.31
Q17	4.71	5.29	0.00
Q18	5.22	5.29	0.00
Q19	0.56	1.38	5.22
Q20	2.05	1.38	4.71
Q21	-6.21	-6.83	0.00
Q22	-6.66	-6.83	0.00
Q23	0.00	-0.56	14.17
Q24	-3.90	0.00	0.00
Q25	0.73	0.00	0.00
Q26	-3.47	0.00	0.00
Q27	9.84	10.06	-7.53
Q28	9.42	10.06	0.85
Q29	9.84	10.08	0.00
Q30	9.43	10.08	13.53
Q31	0.84	0.09	0.23
Q32	0.00	0.00	-7.56
Q33	1.32	0.00	-7.54
Q34	-7.54	-7.45	6.27
Q35	-7.63	-7.45	5.41
Q36	-6.73	-7.32	0.00
Q37	-7.56	-7.32	0.00
Q38	5.41	6.00	0.00
Q39	6.27	6.00	0.00
Q40	1.65	0.00	0.00

Table 5-7. Type S1C030 A1&4 PC Card, Voltage Measurements (cont)

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q41	-1.73	-0.002	-0.002
Q42	0.637	-0.100	-0.094
Q43	-3.831	-0.100	-0.090
Q44	1.46	.766	-7.67
Q45	0.002	.766	-0.100
Q46	0.073	.766	-0.100
Q47	0.175	-0.440	14.93
Q48A	14.44	14.92	14.44
Q48B	14.41	14.92	0.002
Q49	0.811	-0.100	-0.095
Q50A	13.55	14.22	12.99
Q50B	13.55	14.21	5.96
Q51	12.99	13.55	-0.08
Q52A	9.72	0.01	-0.05
Q52B	9.72	0.01	-4.46
Q53	7.01	6.599	0.008
Q54	5.93	6.05	2.05
Q55	-0.10	-0.737	5.93
Q56	7.23	7.71	1.57
Q57	7.23	7.70	0.005
Q58	3.49	2.93	4.98
Q59	1.97	2.58	-14.90
U2- Q1	-14.30	-14.90	-6.99
U2- Q2	-14.30	-14.90	-6.90
U2- Q3	-14.30	-14.90	-0.86
U2- Q4	-14.30	-14.90	-0.90
U2- Q5	-14.48	-15.10	-14.48
U8- Q1	-14.30	-14.98	-0.79
U8- Q2	-14.30	-14.98	-0.79
U8- Q3	-14.30	-14.98	-7.48
U8- Q4	-14.30	-14.98	-7.48
U8- Q5	-14.47	-15.10	-14.48
U11-Q1	-0.10	-0.75	12.96
U11-Q2	-0.10	-0.76	12.96
U11-Q3	-0.61	-0.56	14.40
U11-Q4	-0.09	-0.09	0.00
U11-Q5	-0.09	-0.09	-0.09
U12-Q1	7.73	7.08	14.61
U12-Q2	7.81	7.08	14.61
U12-Q3	7.74	7.01	14.61
U12-Q4	-4.47	-4.95	-0.09
U12-Q5	-4.52	-4.95	-4.52

Table 5-8. Type THD001 A1A5 PC Card, Voltage Measurements

TRANSISTOR FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	5.56	6.2	0.17
Q2	5.56	6.2	-5.8
Q3	-0.17	-0.8	14.1
Q4	-4.21	-3.8	-15.1
Q5	8.63	2.64	-0.08
Q6	9.05	2.64	-3.28
Q7	14.95	14.95	2.63
Q8	1.49	0.86	14.95
Q9	0.001	0.86	14.95
Q10	5.56	6.23	-0.02
Q11	5.56	6.20	-5.99
Q12	-14.4	-15.12	-15.09
Q13	-15.12	-15.12	-0.001
Q14	0.200	0.836	-14.40
Q15	1.49	0.85	-15.12
Q16	6.29	6.29	13.45
Q17	0.11	0.34	9.83
Q18	-0.50	-0.22	9.41
Q19	-0.63	-0.26	9.41
Q20	1.73	0.97	8.53
Q21	0.00	-0.64	14.54
Q22	0.001	-0.64	0.00
Q23	0.1	-0.5	14.95
U1- Q1	0.95	0.23	0.85
U1- Q2	0.95	0.23	6.19
U1- Q3	-6.59	-7.35	-5.84
U1- Q4	-5.84	-6.60	-0.18
U1- Q5	-6.90	-7.66	-6.91
U2- Q1	-0.10	-0.83	6.91
U2- Q2	-0.83	-0.83	-0.83
U2- Q3	-0.10	-0.83	6.20
U2- Q4	-3.28	-3.80	-0.08
U2- Q5	-3.29	-3.81	-3.28
U3- Q1	1.46	0.78	6.16
U3- Q2	1.46	0.78	1.46
U3- Q3	-6.72	-7.46	-5.98
U3- Q4	-5.98	-6.71	-0.02
U3- Q5	-7.04	-7.78	-7.04
U4- Q1	-0.83	IC	5.97
U4- Q2	-4.21	0.00	IC
U4- Q3	-0.80	IC	5.97
U4- Q4	0.01	IC	5.48

Table 5-8. Type TIID001 PC Card, Voltage Measurements (cont)

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR DRAIN
U4- Q5	-4.21	-4.97	IC
U4- Q6	-0.83	IC	5.48
U5- Q3	0.01	-0.73	0.76
U5- Q4	-0.08	-0.82	7.67
U5- Q5	-5.68	-6.44	-2.23
U6- Q1	5.96	IC	9.16
U6- Q2	1.10	0.34	IC
U6- Q3	6.15	IC	9.41
U6- Q4	5.67	IC	10.03
U6- Q5	0.51	-0.26	IC
U6- Q6	5.48	IC	9.82
U7- Q1	5.96	IC	9.07
U7- Q2	0.51	-0.25	IC
U7- Q3	5.71	IC	9.07
U7- Q4	6.03	IC	9.80
U7- Q5	+0.63	-0.25	IC
U7- Q6	5.48	IC	9.80
U8- Q1	0.66	-0.09	6.19
U8- Q2	-0.09	-0.09	6.30
U8- Q3	1.42	0.68	6.19
U8- Q4	0.66	0.09	6.19
U8- Q5	-0.11	-0.85	6.20
U9- Q1	4.69	IC	5.85
U9- Q2	-6.79	-7.72	IC
U9- Q3	-0.85	IC	6.33
U9- Q4	-0.09	IC	5.85
U9- Q5	-6.79	7.52	IC
U9- Q6	-0.09	IC	6.33
U10-Q1	0.01	-0.63	6.19
U10-Q2	-0.63	-0.63	6.19
U10-Q3	0.94	0.22	6.19
U10-Q4	0.42	-0.30	6.19
U10-Q5	-0.09	-0.81	6.20
U11-Q1	0.22	IC	5.68
U11-Q2	-4.24	-5.00	IC
U11-Q3	-0.81	IC	6.15
U11-Q4	-0.30	IC	5.68
U11-Q5	-4.25	-5.00	IC
U11-Q6	-0.30	IC	6.15
U12-Q1	0.69	IC	5.16
U12-Q2	-6.79	-7.52	IC
U12-Q3	-0.85	IC	6.15

Table 5-8. Type THD001 PC Card, Voltage Measurements (cont)

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR DRAIN
U12-Q4	-0.09	IC	5.67
U12-Q5	-6.79	-7.52	IC
U12-Q6	-0.09	IC	6.15
U13-Q1	6.33	IC	9.41
U13-Q2	0.54	-0.22	IC
U13-Q3	5.55	IC	9.10
U13-Q4	6.02	IC	9.82
U13-Q5	1.15	0.97	IC
U13-Q6	5.85	IC	10.04
U14-Q1	5.85	IC	10.02
U14-Q2	1.77	1.01	IC
U14-Q3	5.67	IC	10.02
U14-Q4	6.15	IC	9.19
U14-Q5	0.10	1.01	IC
U14-Q6	6.33	IC	9.19
U15-Q1	0.01	-0.70	6.20
U15-Q2	-0.70	-0.70	6.29
U15-Q3	-0.10	-0.79	6.20
U15-Q4	0.43	-0.28	6.19
U15-Q5	-0.08	-0.08	-0.08
U16-Q1	-0.28	IC	5.55
U16-Q2	-6.79	-7.53	IC
U16-Q3	-0.69	IC	5.55
U16-Q4	-0.80	IC	6.02
U16-Q5	-6.79	-7.53	IC
U16-Q6	-0.69	IC	6.02
U17-Q1	5.55	IC	10.02
U17-Q2	0.09	1.01	IC
U17-Q3	5.71	IC	10.02
U17-Q4	6.12	IC	9.48
U17-Q5	1.18	1.01	IC
U17-Q6	6.02	IC	9.48
U18-Q1	6.02	IC	1.98
U18-Q2	0.55	-0.21	IC
U18-Q3	5.60	IC	8.98
U18-Q4	5.89	IC	9.77
U18-Q5	-0.50	-0.21	IC
U18-Q6	-0.55	IC	9.77

IC is Internal Connection

Table 5-9. Type PDT020 A1A6 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	12.03	12.72	9.96
Q2	9.78	9.77	0.02
Q3	9.29	9.97	3.27
Q4	3.44	0.81	0.00
Q5	0.10	0.80	0.73
Q6	3.44	2.77	0.01
Q7	0.08	2.77	9.07
Q8	12.05	12.76	9.90
Q9	9.75	9.90	0.01
Q10	9.22	9.89	3.46
Q11	0.08	2.80	6.15
Q12	3.44	2.80	5.52
Q13	2.07	0.83	0.37
Q14	2.04	0.83	0.38
Q15	-5.86	-5.23	-12.42
Q16	14.94	14.94	7.75
Q17A	13.14	7.75	10.97
Q17B	13.14	7.75	13.63
Q18	14.94	14.94	6.76
Q19A	13.15	6.48	10.97
Q19B	13.15	6.79	13.63
Q20	14.18	14.94	14.93
Q21A	14.19	14.87	10.97
Q21B	14.19	14.87	13.65
Q22	10.28	10.95	0.00
Q23	10.86	10.95	5.45
Q24	0.08	0.58	5.01
Q25	-0.51	-0.09	0.43
Q26	-6.04	-6.70	-0.09
Q27	12.06	12.77	10.10
Q28	9.46	10.10	3.91
Q29	10.00	10.10	0.02
Q30	2.01	3.23	4.19
Q31	3.91	3.23	4.19
Q32	1.50	3.22	5.01
Q33	4.19	4.34	10.87
Q34	5.01	4.34	0.01
Q35	14.94	14.94	7.42
Q36A	13.24	7.42	10.90
Q36B	13.24	7.42	13.71
Q37	14.94	14.94	6.99
Q38A	13.26	6.99	10.91

Table 5-9. Type PDT020 PC Card, Voltage Measurements (cont)

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q38B	13.26	6.99	13.71
Q39	14.18	14.94	14.93
Q40A	14.19	14.86	10.90
Q40B	14.19	14.86	13.71
Q41	10.22	10.88	0.00
Q42	10.70	10.88	5.45
Q43	0.08	0.84	10.70
Q44	1.51	0.84	9.99
Q45	2.01	0.67	-15.14
Q46	0.00	0.67	-14.84
Q47	1.33	2.02	0.93
Q48	3.00	2.02	0.04
U15-Q1	0.04	0.20	5.45
U15-Q2	0.92	0.20	5.85
U15-Q3	-6.70	-7.40	0.20
U15-Q4	-6.70	-7.40	13.56
U16-Q1	0.04	0.05	5.45
U16-Q2	0.64	0.05	6.00
U16-Q3	-6.70	-7.38	-0.05
U16-Q4	-6.70	-7.38	13.67

Table 5-10. Type HLF001 A1A7 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	14.2	14.95	14.92
Q2	5.4	6.46	5.46
Q3	5.4	5.46	5.46
Q4A	5.46	6.12	-11.58
Q4B	5.46	6.12	-11.58
Q5A	15.73	14.44	7.13
Q5B	14.25	14.95	14.23
Q6	5.52	4.60	0.08
Q7	3.62	4.20	0.04
Q8	-0.08	0.57	-13.23
Q9	7.00	8.35	2.34
Q10	-12.25	-12.89	-0.63
Q11	5.82	6.01	-0.08
Q12	5.70	5.20	14.95
Q13	6.16	7.20	14.06
Q14	4.97	3.38	-0.03

Table 5-11. Type PLL102 A1A8 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
FETQ1	4.97	5.46	5.46
FETQ2	4.96	5.46	5.45
FETQ3	4.96	5.45	5.45
FETQ4	4.27	5.44	5.46
Q5	13.14	13.84	13.82
Q6	13.83	13.84	-4.78
FETQ7	-1.87	-2.07	-2.07
Q8	1.93	1.22	4.39
Q9	2.01	1.31	4.35
Q10	15.05	15.05	-13.34

Table 5-12. Type CSD002 A1A9 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	8.86	9.30	0.05
Q2	8.88	9.30	1.99
Q3	12.86	13.36	9.92
Q4	4.72	5.00	-14.48
Q5	4.43	4.43	5.09
Q6	4.43	2.51	5.07
Q7	2.36	2.51	0.03
Q8	1.88	2.51	-5.65
Q9	5.00	5.00	-14.48
Q10	0.04	0.72	-5.26
Q11	0.77	0.71	-5.63
Q12	1.60	2.41	7.12
Q13	1.58	2.41	7.12
Q14	0.04	0.10	2.38
Q15	0.79	0.10	1.88
Q16	6.77	13.87	11.96
Q17	-0.40	0.03	11.97
Q18	-5.63	-5.97	0.03
Q19	-5.26	-5.97	-5.96
Q20	0.79	0.05	0.03
Q21	-5.28	-5.99	-5.97
Q22	-5.27	-5.95	-5.27
FETQ23	-14.08	-3.33	0.03
FETQ24	-14.07	-4.49	0.03
Q25	-5.46	-4.79	-11.21

Table 5-13. Type CCR036 A1A10 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	-5.87	-5.23	-13.38

Table 5-14. Type ACL009 AlAll PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTION/ DRAIN
Q1	-0.05	0.42	-0.08
Q2	1.08	12.87	0.42
Q3	-6.97	-6.24	-8.20
Q4	3.93	3.93	0.42
Q5	0.62	-0.08	3.1
Q6	0.62	-0.08	0.64
Q7	3.94	3.93	0.93
Q8	3.94	3.93	1.93
Q9	2.49	3.10	-0.05
Q10	3.12	2.49	14.94
Q11	4.53	0.01	12.13
Q12	4.54	3.95	12.10
Q13	-0.06	-0.44	4.53
Q14	-0.05	-0.43	4.54
Q15	4.53	3.95	8.64
Q16	4.52	3.95	8.70
Q17	-0.75	-0.08	-7.75
Q18	-0.75	0.01	-12.50
Q19	-12.50	-13.16	-0.08
Q20	-13.16	-12.50	-15.15
U6- Q1	-11.77	-12.48	-8.08
U6- Q2	-11.77	-12.48	-8.54
U6- Q3	-7.76	-8.47	-4.23
U6- Q4	-11.77	-12.49	-11.77
U6- Q5	-11.77	-12.49	-11.77
U7- Q1	-7.75	-8.50	-4.23
U7- Q2	-7.75	-8.50	-4.22
U7- Q3	-3.15	-3.90	-0.95
U7- Q4	-3.14	-3.91	-0.98
U7- Q5	-8.34	-9.09	-8.34

Table 5-15. Type PDC001, A2A4 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	4.86	4.86	0.73
Q2	0.74	0.01	0.03
Q3	14.97	14.98	0.02
Q4	-0.09	1.22	14.97
Q5	1.85	1.22	14.97
Q6	0.01	0.01	3.88
Q7	-0.09	-0.74	14.97
Q8	-2.04	-0.74	14.98
U1- Q1	-0.81	-1.55	4.63
U1- Q2	-8.77	-1.55	4.86
U1- Q3	-8.05	-8.78	4.76
U1- Q4	3.70	2.97	4.76
U1- Q5	-0.07	-0.81	4.63

Type 5-16. Type DDR022, A3A5 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	5.13	3.25	0.01
Q2	2.60	3.25	0.74
Q3	0.74	0.11	0.01

Table 5-17. Type INP050 A4A1 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
FETQ1	0.02	2.72	13.25
Q2	-12.32	-13.00	-7.42
U4- Q1	-6.65	-7.42	-0.30
U4- Q2	-6.65	-7.42	-0.30
U4- Q3	-5.90	-6.65	0.00
U4- Q4	-5.90	-6.64	0.00
U4- Q5	-15.00	-15.00	-15.00

Table 5-18. Type LDR023 A4A9 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR DRAIN
Q1	3.86	1.87	-11.11
Q2	1.20	1.87	-5.26
Q3	-7.39	-6.79	0.00
Q4	-5.97	-6.83	-6.79
Q5	-6.83	-6.88	-5.26
Q6	-10.45	-11.13	-7.38
Q7	-11.10	-11.13	-5.98
Q8	-6.52	-5.89	-14.89
Q9	-6.88	-6.19	-8.20
Q10	-8.20	-7.55	-14.83
Q11	-7.55	-6.88	-14.79

Table 5-19. Type LDR024 A4A11 PC Card, Voltage Measurements

TRANSISTOR/ FET	BASE/ GATE	EMITTER/ SOURCE	COLLECTOR/ DRAIN
Q1	0.38	8.65	5.22
Q2	1.19	1.91	-3.95
Q3	3.84	1.91	-9.82
Q4	9.36	8.67	8.65
Q5	8.68	9.67	9.98
Q6	1.77	2.68	8.65
Q7	2.68	2.69	2.44
Q8	-9.18	-9.74	-4.58
Q9	-9.82	-9.77	9.36
Q10	-4.58	-3.96	8.68
Q11	-3.96	-10.81	-3.91
Q12	-3.86	-3.94	2.60
Q13	-3.94	-3.96	-3.20
Q14	1.19	1.57	-3.98
Q15	2.06	1.57	-9.09
Q16	-3.49	-2.90	-14.81
Q17	-3.96	-3.28	-5.26
Q18	-5.26	-4.62	-14.80
Q19	-4.62	-3.96	-14.45
Q20	-9.11	-9.00	-3.86
Q21	-9.09	-9.09	1.77
U1- Q1	0.33	0.33	0.33
U1- Q2	0.54	0.33	15.07
U1- Q3	0.00	-0.72	5.15
U1- Q4	0.25	-0.59	-0.51
U1- Q5	0.00	0.00	0.00

SECTION VI

PARTS LISTS AND DRAWINGS

6.1 GENERAL

This section contains the parts lists and assembly drawings for the Model 335, a list of accessory items, parts lists, assembly drawings and schematics for each printed circuit card, front and rear panel wiring diagrams, and pc card interconnection wiring diagrams. Table 6-1 lists all elements of this section. Table 6-2 is a list of the manufacturers' codes used in the parts lists.

Table 6-1. Parts Lists and Drawings

TITLE	NUMBER
PCM Bit Synchronizer Top Assembly Model 335	356-0002-☐
PCM Bit Synchronizer Chassis Assembly Model 335	355-0002-☐
List of Accessories Model 335	354-0160-501
Front Panel, Wiring Diagram	F)07-495
Rear Panel, Wiring Diagram	D)07-494
PC Card Type VAF027-1, Parts List, Assembly Drawing and Schematic	460-0908-501
PC Card Type SLC029-1, Parts List, Assembly Drawing and Schematic	460-0921-501
PC Card Type VAF026-1/VAF026-2, Parts List, Assembly Drawing and Schematic	460-0903-501, 502
PC Card Type SLC030-1, Parts List, Assembly Drawing and Schematic	460-0927-501
PC Card Type THD001-1, Parts List, Assembly Drawing and Schematic	460-0906-501
PC Card Type PDT020-1, Parts List, Assembly Drawing and Schematic	460-1058-501
PC Card Type HLF001-2, Parts List, Assembly Drawing and Schematic	460-1065-501

Table 6-1. Parts Lists and Drawings (cont.)

TITLE	NUMBER
PC Card Type PLL102-1, Parts List, Assembly Drawing and Schematic	460-1059-501
PC Card Type CSD002-1, Parts List, Assembly Drawing and Schematic	460-1095-501 600-0335
PC Card Type CCR036-1, Parts List, Assembly Drawing and Schematic	460-0982-501
PC Card Type ACL009-1, Parts List, Assembly Drawing and Schematic	460-1823-501 600-0311
PC Card Type XTL028-1, Parts List, Assembly Drawing and Schematic	460-1105-501
PC Card Type BCD001-1, Parts List, Assembly Drawing and Schematic	460-0981-501
PC Card Type PDC001-1, Parts List, Assembly Drawing and Schematic	460-0985-501
PC Card Type LDY001-1, Parts List, Assembly Drawing and Schematic	460-1085-501
PC Card Type PSR021-1, Parts List, Assembly Drawing and Schematic	460-1096-501
PC Card Type DDR022-1, Parts List, Assembly Drawing and Schematic	460-0836-501
PC Card Type INP050-1, Parts List, Assembly Drawing and Schematic	460-0986-501
PC Card Type DDR030-1, Parts List, Assembly Drawing and Schematic	460-1097-501
PC Card Type LDR023-1, Parts List, Assembly Drawing and Schematic	460-0949-501
PC Card Type LDR024-1, Parts List, Assembly Drawing and Schematic	460-0980-501
PC Card Interconnection Wiring Diagrams (25 sheets)	

Table 6-2. Manufacturers' Codes Index

CODE	MANUFACTURER
00655	Electromec, Inc. Los Angeles, CA
00656	Aerovex Industries, Inc. 740 Belleville Ave. New Bedford, MA 02741
00779	AMP, Inc. P.O. Box 3608 Harrisburg, PA 17105
01295	Texas Instruments, Inc. Semiconductor Components Div. 13500 North Central Expressway Dallas, TX 75231
03508	General Electric Co. Semiconductor Products Dept. Electronics Park Syracuse, NY 13201
03877	Transitron Electronic Corp. 168-186 Albion St. Wakefield, MA 01880
04713	Motorola Semiconductor Products, Inc. 5005 East McDowell Road Phoenix, AZ 85008
05236	Jonathan Mfg. Co. 1101 S. Acacia Ave. Fullerton, CA 92631
05820	EG & G Wakefield Engineering 60 Audubon Road Wakefield, MA 01880
06401	Sperry Corp. Univac Defense System Div. Special Programs 640 North 2200 West SLC, UT 84116
07047	Ross Milton Co. 511 Second Street Pike Southampton, PA 18966
07137	TEC Inc. 2727 N. Fairview Avenue Tucson, AZ 85705
07263	Fairchild Camera and In- strument Corp. Semiconductor Div. 464 Ellis Street Mountain View, CA 94042
07993	Conservomatic Corp. 113 Bala Ave. Oreland, PA 19075
08324	Stewart, Fred E. Co. DBA FESCO 13900 B. Shoemaker Ave. Norwalk, CA 90650
08742	acdc Electronics, Inc. Oceanside Industrial Cente 401 Jones Road Oceanside, CA 92054
09213	General Electric Co. Semiconductor Products Dep Power Components Operation W. Genesee St. Auburn, NY 13021
09214	General Electric Co. Semiconductor Products Dep Power Components Operation W. Genesee St. Auburn, NY 13021
09353	C & K Components, Inc. 15 Riverdale Avenue Newton, MA 02158
12040	National Semiconductor Corp Commerce Drive P.O. Box 443 Danbury, CT 06810
12065	Incon Inc. Transitron Precision Connecto Division 316 Ash Street Reading, MA 01867
13103	Thermalloy Co., Inc. 2021 W. Valley View Lane P.O. Box 34829 Dallas, TX 75234

Table 6-2. Manufacturers' Codes Index (cont)

CODE	MANUFACTURER
14752	Electro Cube Inc. 1710 S. Del Mar Ave. San Gabriel, CA 91776
14949	Trompeter Electronics, Inc. 8936 Comanche Ave. Chatsworth, CA 91311
17117	Electronic Molding Corp. 96 Mill St. Woonsocket, RI 02895
18324	Signetics Corp. 811 E. Arques Ave. Sunnyvale, CA 94086
18583	Curtis Instruments, Inc. 200 Kisco Ave. Mt. Kisco, NY 10549
18612	Vishay Resistor Products Div. Vishay Intertechnology Inc. 63 Lincoln Hwy. Malvern, PA 19355
18786	Micro Power Inc. Long Island City, NY
20747	Aydin Monitor Systems 502 Office Center Drive Fort Washington, PA 19034
20891	Cosar Corp. 3121 Benton Street Garland, TX 75042
21604	Buckeye Stamping Co. 555 Marion Road Columbus, OH 43207
24355	Analog Devices, Inc. Rte 1 Industrial Park P.O. Box 280 Norwood, MA 02062
27014	National Semiconductor Corp. 2900 Semiconductor Drive Santa Clara, CA 95051
27802	Vectron Laboratories Inc. 166 Glover Avenue Norwalk, CT 06850
31433	Union Carbide Corporation Electronics Division Components Dept. Highway 276 SE P.O. Box 5928 Greenville, SC 29606
32559	Bivar Inc. 1617 Edinger Avenue Santa Ana, CA 92705
32997	Bourns, Inc. Trimpot Products Div. 1200 Columbia Ave. Riverside, CA 92507
33888	Fairchild Camera & Instrument Corp. 464 Ellis Street Mountain View, CA 94042
49956	Raytheon Co. 141 Spring Street Lexington, MA 02173
50507	Unitrode Corp. Micro Networks Division 324 Clark Street Worcester, MA 01606
55289	Environmental Sciences Associates, Inc. 45 Wiggons Ave. Bedford, MA 01730
56289	Sprague Electric Co. 87 Marshall Street North Adams, MA 01247
65092	Weston Instruments Div. Sangamo Weston, Inc. 614 Frelinghuysen Ave. Newark, NJ 07114

Table 6-2. Manufacturers' Codes Index (cont)

CODE	MANUFACTURER
70903	Belden Corp. 2000 S. Batavia Avenue Geneva, IL 60134
71002	Birnbach Co., Inc. 177 Hanse Avenue Freeport Long Island, NY 11520
71279	Cambridge Thermionic Corp. 445 Concord Ave. Cambridge, MA 02138
71400	McGraw Edison Co. Bussmann Mfg. Div. 502 Earth City Plaza P.O. Box 14460 St. Louis, MO 63178
71590	Globe-Union Inc. Centralab Division Hwy. 20W P.O. Box 858 Ft. Dodge, IA 50501
72136	Electro Motive Mfg. Co., Inc. Lauter Avenue P.O. Box 7600 Florence, SC 29501
72619	Dialight Div. Amperex Electronics Corp. 203 Harrison Place Brooklyn, NY 11237
72962	Esna Div. of Amerace Corp. 2330 Vauxhall Rd. Union, NJ 07083
72982	Erie Technological Products Inc. 645 W. 11th St. Erie, PA 16512
73138	Beckman Instruments, Inc. Helipot Div. 2500 Harbor Blvd. Fullerton, CA 92634
74545	Hubbell Harvey, Inc. 584 Derby Milford Road Orange, CT 06477
74970	Johnson E.F. Co. 299 10th Ave. SW Waseca, MN 56093
75382	Kulka Electric Corp. Fulton Ave. Mt. Verson, NY 10550
75915	Littlefuse, Inc. 800 E. Northwest Hwy. Des Plaines, IL 60016
78769	Titchener, E.H. 1 Titchener Place Binghamton, NY 13902
81073	Grayhill Inc. 561 Hillgrove Ave. P.O. Box 373 La Grange, IL 60525
81348	Federal Specifications Promulgated by General Services Administration Washington, DC
81349	Military Specifications Promulgated by Military Depts. under Authority of Defense Standardization
81640	Eaton Corp. Cutler-Hammer Group 2074 Whitfield Avenue E P.O. Box 1978 Sarasota, FL 33578
82877	Rotron, Inc. 7-9 Hasbrouck Lane Woodstock, NY 12498
83003	Varo, Inc. 2203 Walnut Street P.O. Box 401426 Garland, TX 75040

Table 6-2. Manufacturers' Codes Index (cont)

CODE	MANUFACTURER
83508	Grant Hardware Co. 7 Hoover Avenue Haverstraw, NY 10927
84411	TRW Inc. TRW Electronics Components Div. TRW Capacitors 301 West 0 Street Opallala, NE 69153
86684	RCA Corp. Distribution & Special Prod. Bldg. 206-2 Cherry Hill Offices Cherry Hill, NJ 08358
91506	Augat, Inc. 33 Perry Ave. P.O. Box 779 Attleboro, MA 02703
91637	Dale Electronics, Inc. P.O. Box 609 Columbus, NE 68601
91662	Elco Corp. A Gulf & Western Mfg. Co. Connector Division Huntingdon Industrial Park Huntingdon, PA 16652
94271	Weston Components & Controls Div. of Sangamo Western Inc. Archbald, PA 18403
95146	ALCO Electronics Prod. Inc. 1551 Osgood Street North Andover, MA 01845
96733	San Fernando Electric Mfg. Co. 1591 First Street San Fernando, CA 91341
96906	Military Standards Promulgated by Military Depts. under Authority of Defense Standardization
97954	US Components Inc. 35 Carlough Rd. Bohemia, NY 11716
98975	Model Rectifier Corp. Brooklyn, NY
98978	International Electronic Research Corp. Sub. of Dynamics Corp. of America 135 W. Magnolia Blvd. Burbank, CA 91502

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		22 Feb 83	RS Volz
K	REVISED PER ECO 08630 R.P.E. 11-21-83		29 Nov 83	RSM

ATP: A) 297-0477-501
ATP ADDENDUM: A) 297-0477-501
CIRCUIT CARD TEST PROC: A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L.GRUCELLA	4-11-80	ENGINEER	D.R.McKINNEY	4-18-80	DWG NO.	REV
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80	PL356-0002-501	K
DRAFTING	E.S.	5-5-80	MFG 5/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

R00-0066

800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	PDT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY	8/12	8/12	8/12	8/12	8/12											
	FILE A4	INP 050-1						DDR 030	DDR 030	LDR 023		LDR 024-1					
	KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/36					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY L. GRUCELLA DATE 4-9-80	CHECKED DATE	TITLE PCM BIT SYNCHRONIZER TOP ASSEMBLY, MODEL 335	CODE IDENT NO. 20747	DWG. NO. PL356-0002-501 SHEET 2 OF	REV K

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		22 Feb 83	RS Volz
K	REVISED PER ECO 08630 R.P.K. 11-21-83		29 Nov 83	RSM

ATP: A) 297-0477-501
ATP ADDENDUM: A) 297-0477-501
CIRCUIT CARD TEST PROC: A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA	4-11-80	ENGINEER	D.R. McKINNEY	4-18-80	DWG NO.	REV
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80	PL356-0002-501	K
DRAFTING	E.S.	5-5-80	MFG 5/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

800-0068

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		22Feb 83	RS Volz
K	REVISED PER ECO 08630 R.P.K. 11-21-83		29 Nov 83	[illegible]

ATP: A) 297-0477-501 WIRE LIST: A) 730-2011
ATP ADDENDUM: A) 297-0477-502
ATP ADDENDUM: A) 297-0477-504
CIRCUIT CARD TEST PROC: A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER TOP ASSEMBLY MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L.GRUCELLA	4-11-80	ENGINEER	D.R.McKINNEY	4-18-80	DWG NO.	REV
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80	PL356-0002-502	K
DRAFTING	E.S.	5-5-80	MFG 5/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

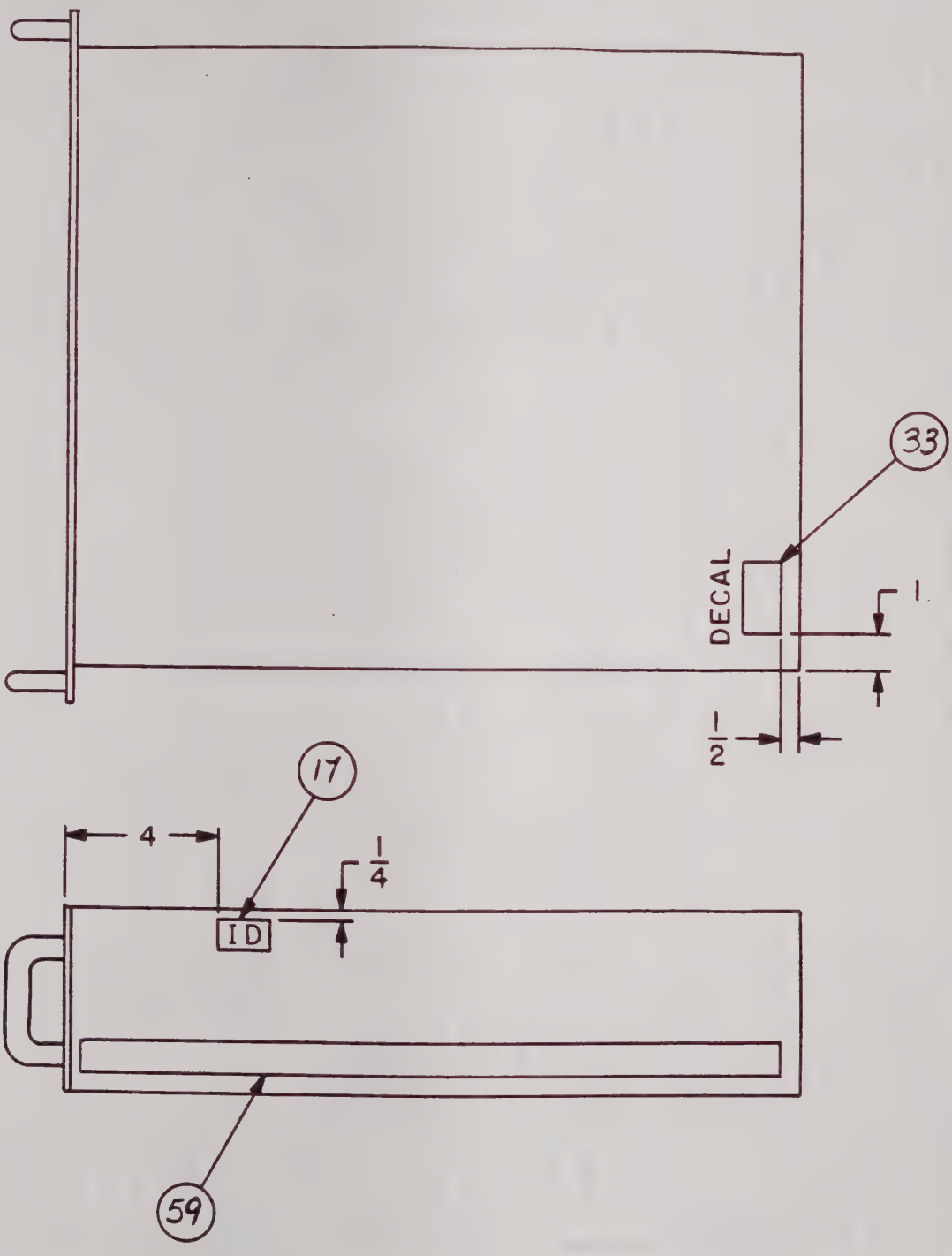
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	PDT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY																
	FILE A4	INP 050-1				UX 801-30		DDR 030-2	DDR 030-2	LDR 023		LDR 024-1					
	KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/36					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY	CHECKED	TITLE	CODE IDENT NO.	DWG. NO.	REV
L. GRUCELLA		PCM BIT SYNCHRONIZER TOP ASSEMBLY - MODEL 335	20747	PL 356-0002-502	K
DATE 4-9-80	DATE			SHEET 2 OF	

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		356-0002-501		K	PARENT 335-10-20-P0	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-002			IDENT DECAL CONN	
1	048	355-0002-501		E	MOD 335 CHASSIS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MAN-335	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0836-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	108	460-0980-501		E	LDR024-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	112	460-0986-501		H	INP050-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	116	460-1065-501		W	HLF001-1	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		L	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	120	460-1097-501		G	DDR030-1	
1	122	460-1823-501		A	ACL009-1	
1	123	460-1105-501		H	XTL028-1	



AYDIN MONITOR SYSTEMS

800-0155A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-501	K
	SHEET 4 OF	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		22 Feb 83	RS Volz
K	REVISED PER ECO 08630 R.P.K. 11-21-83		29 Nov 83	[illegible]

ATP: A) 297-0477-501 WIRE LIST: A) 730-2012
ATP ADDENDUM: A) 297-0477-502
ATP ADDENDUM: A) 297-0477-503
CIRCUIT CARD TEST PROC: A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER TOP ASSEMBLY MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA	4-11-80	ENGINEER	D.R. McKINNEY	4-18-80	DWG NO.	REV
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80	PL356-0002-503	K
DRAFTING	E.S.	5-5-80	MFG 5/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

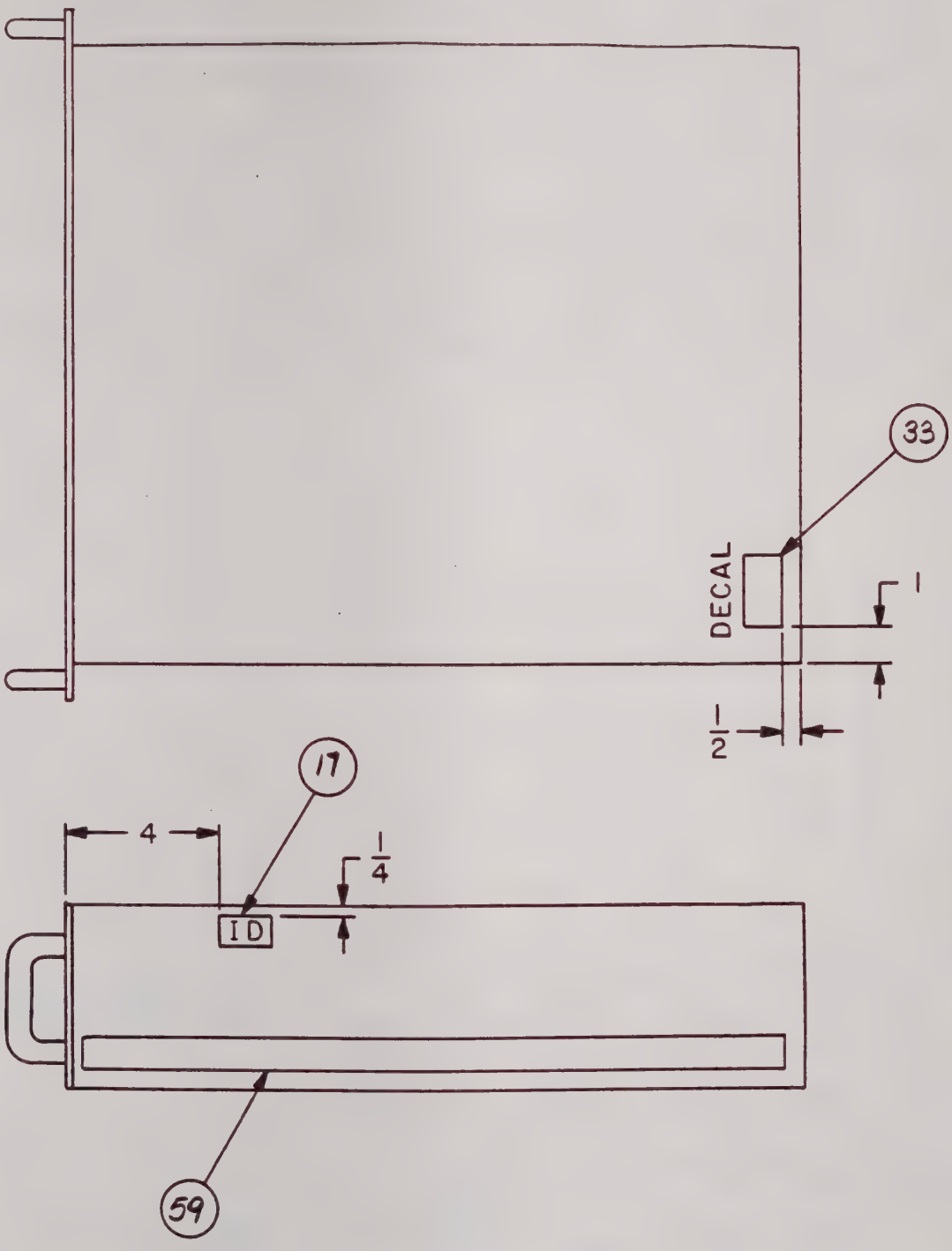
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	POT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY																
	FILE A4	INP 050-1		BLD 001-1	BLD 002-2			DDR 030	DDR 030	LDR 023		LDR 024-1					
	KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/36					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY	CHECKED	TITLE	CODE IDENT NO.	DWG. NO.	REV
L. GRUCELLA		PCM BIT SYNCHRONIZER TOP ASSEMBLY MODEL 335	20747	PL356-0002-503	K
DATE 4-9-80	DATE			SHEET 2 OF	

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.D
		356-0002-502		K	PARENT 335-11-20-PO	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-002			IDENT DECAL CONN	& 1126E
1	048	355-0002-501		E	MOD 335 CHASSIS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MAN-335	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0836-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	108	460-0980-501		E	LDR024-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	112	460-0986-501		H	INP050-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	116	460-1065-501		W	HLF001-1	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		L	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	121	460-1097-502		G	DDR030-2	
1	122	460-1823-501		A	ACL009-1	
1	123	460-1105-501		H	XTL028-1	
1	131	481-0026-30			UX801-30	



AYDIN MONITOR SYSTEMS

800-0153A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-502	K
	SHEET 4 OF	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		22 Feb 83	RS Volz
K	REVISED PER ECO 08630 R.P.R. 11-21-83		29 Nov 83	RSM

ATP: A) 297-0477-501
ATP ADDENDUM: A) 297-0477-502
ATP ADDENDUM: A) 297-0477-503
ATP ADDENDUM: A) 297-0477-505

C.C. TEST PROC: A) 297-0481
WIRE LIST: A) 730-2013

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA	4-11-80	ENGINEER	D.R. McKINNEY	4-18-80	DWG NO. PL356-0002-504	REV K
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80		
DRAFTING	E.S.	5-5-80	MFG 6/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

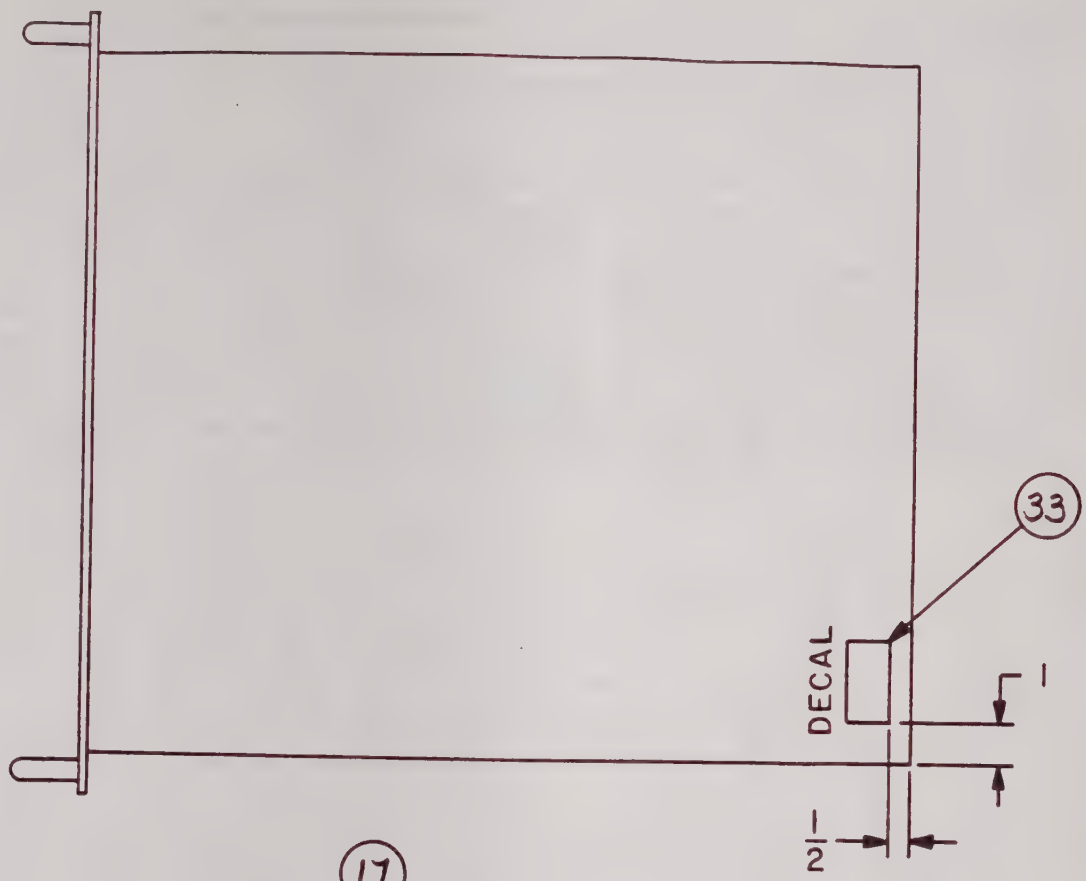
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES

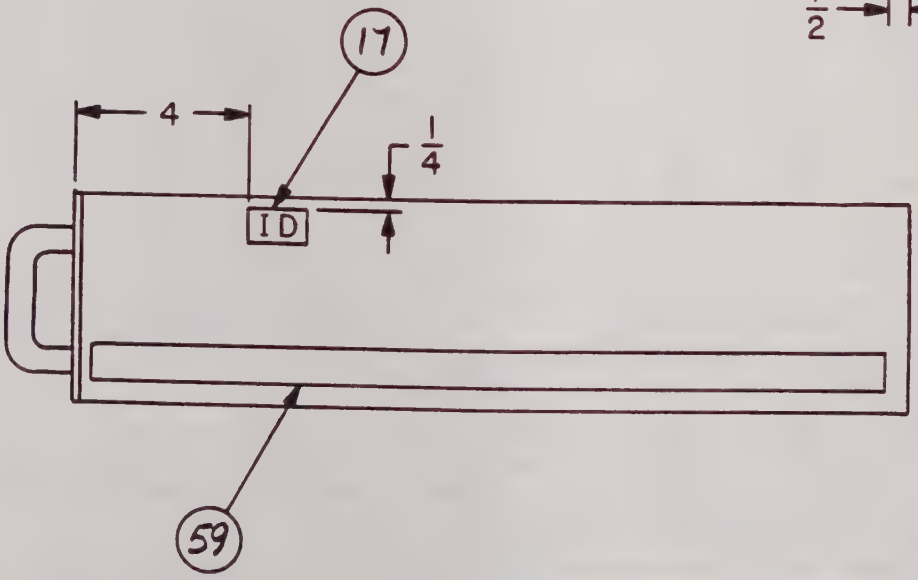
POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	PDT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/30	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY	8/12	8/12	8/12	8/12	8/12											
	FILE A4	INP 050-1		BLD 001-1	BLD 002-2	UX 80-30		DDR 030-2	DDR 030-2	LDR 023		LDR 024-1					
	KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/36					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY	CHECKED	TITLE	CODE IDENT NO.	DWG. NO.	REV
L. GRUCELLA		PCM BIT SYNCHRONIZER TOP ASSEMBLY - MODEL 335	20747	PL356-0002-504	K
DATE 4-9-80	DATE			SHEET 2 OF	

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DE
		356-0002-503		K	PARENT 335-10-21-P0	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-004			CONNECTOR DECAL	
1	048	355-0002-501		E	MOD 335 CHASSIS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MAN-335	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0836-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	108	460-0980-501		E	LDR024-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	112	460-0986-501		H	INP050-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	116	460-1065-501		W	HLF001-1	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		L	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	120	460-1097-501		G	DDR030-1	
1	122	460-1823-501		A	ACL009-1	
1	123	460-1105-501		H	XTL028-1	
1	124	460-1161-501		G	BLD001-1	
1	126	460-1164-502		D	BLD002-2	





AYDIN MONITOR SYSTEMS

800-0155A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-503	K
	SHEET 4 OF	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		22 Feb 83	RS Volz
K	REVISED PER ECO 08457 JSG		10 June 83	RS Volz
L	REVISED PER ECO 08630 R.P.K. 11-27-83		29 Nov 83	RSV

ATP: A) 297-0477-501 WIRE LIST: A) 730-2219
ATP ADDEN: A) 297-0477-502
ATP ADDEN: A) 297-0477-506
C.C. TEST PROC: A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER TOP ASSEMBLY MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA	4-11-80	ENGINEER	D.R. McKINNEY	4-18-80	DWG NO.	REV
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80	PL356-0002-505	L
DRAFTING	E.S.	5-5-80	MFG 5/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

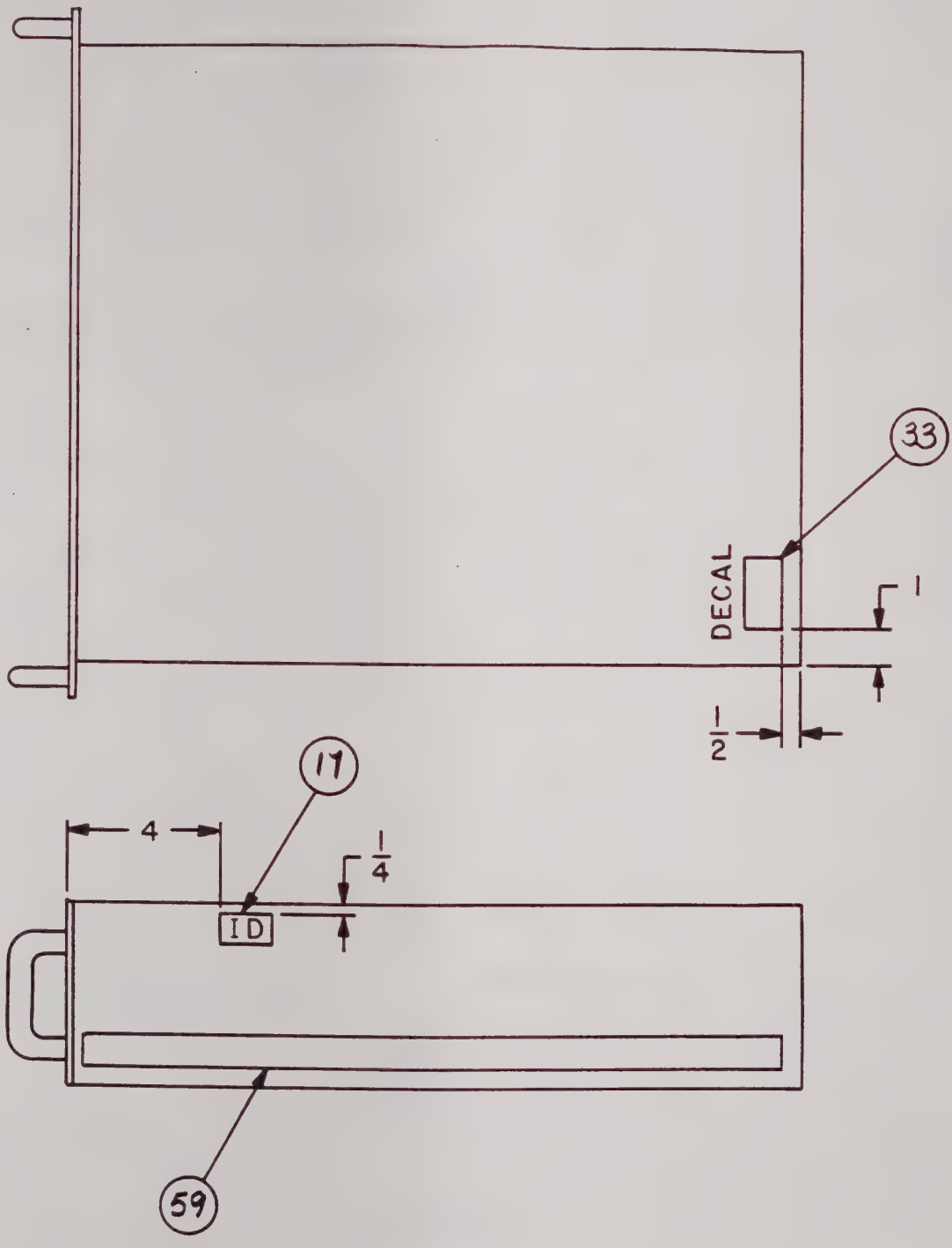
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	PDT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY	8/12	8/12	8/12	8/12	8/12											
	FILE A4	INP 050-1		BLD 001-3	BLD 002-2			DDR 030	DDR 030	LDR 023		LDR 024-1					
	KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/36					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY	CHECKED	TITLE	CODE IDENT NO.	DWG. NO.	REV
L. GRUCELLA		PCM BIT SYNCHRONIZER TOP ASSEMBLY - MODEL 335	20747	PL356-0002-505	L
DATE 4-9-80	DATE			SHEET 2 OF	

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DE
		356-0002-504		K	PARENT 335-11-21-P0	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-004			CONNECTOR DECAL	
1	048	355-2002-501		E	MOD 335 CHASSIS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MAN-335	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0836-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	108	460-0980-501		E	LDR024-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	112	460-0986-501		H	INP050-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	116	460-1065-501		W	HLF001-1	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		L	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	121	460-1097-502		G	DDR030-2	
1	122	460-1823-501		A	ACL009-1	
1	123	460-1105-501		H	XTL028-1	
1	124	460-1161-501		B	BLD001-1	
1	126	460-1164-502		D	BLD002-2	
1	131	481-0026-30			UX801-30	



AYDIN MONITOR SYSTEMS

800-0153A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-504	K
	SHEET 4 OF	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		24 Feb 83	RS Volz
K	REVISED PER ECO 08630 R.F.K. 11-21-83		29 Nov 83	Rem

ATP: A) 297-0477-501
ATP ADDEN: A) 297-0477-502
ATP ADDEN: A) 297-0477-506
CIR. CD. TEST PROC: A) 297-0481

WIRE LIST: A) 730-2015

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA	4-11-80	ENGINEER	D.R. McKINNEY	4-18-80	DWG NO. PL356-0002-506	REV K
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80		
DRAFTING	E.S.	5-5-80	MFG 6/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

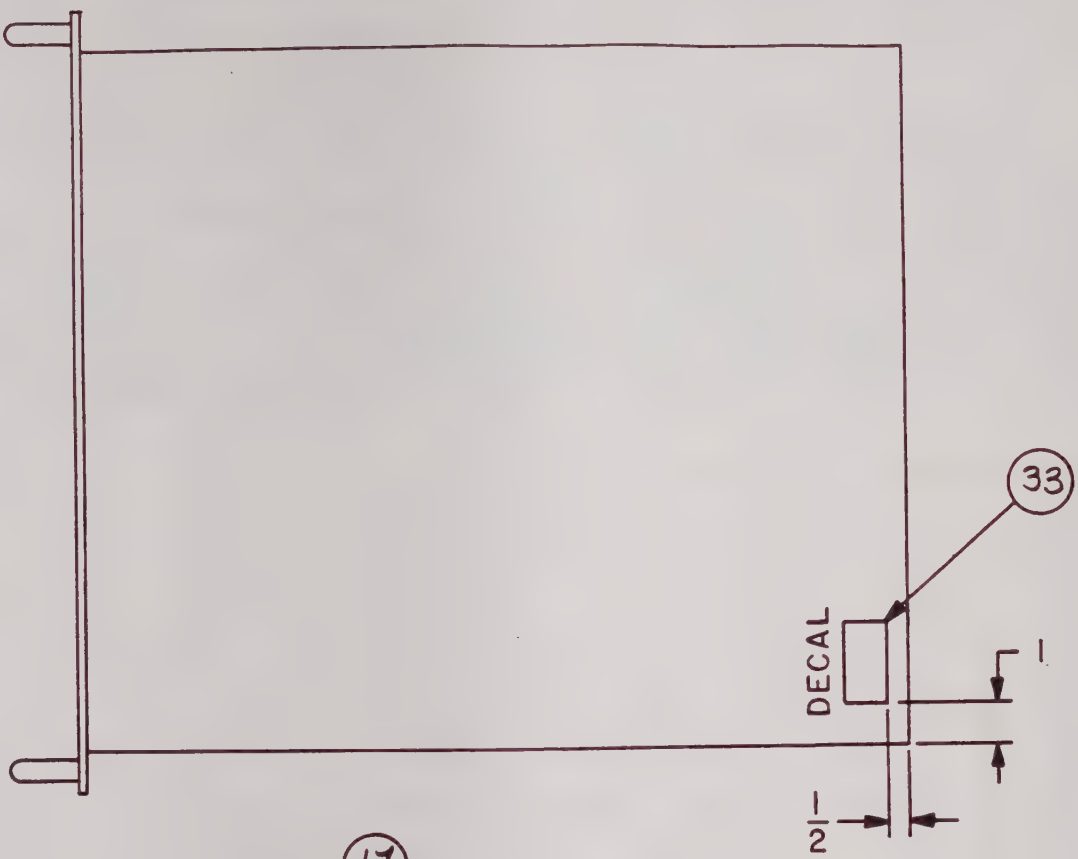
POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	PDT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/24					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY	8/12	8/12	8/12	8/12	8/12											
	FILE A4	INP 050-1		BLD 001-3	BLD 002-2	UX 801-30		DDR 030	DDR 030	LDR 023		LDR 024-1					
	KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/36					

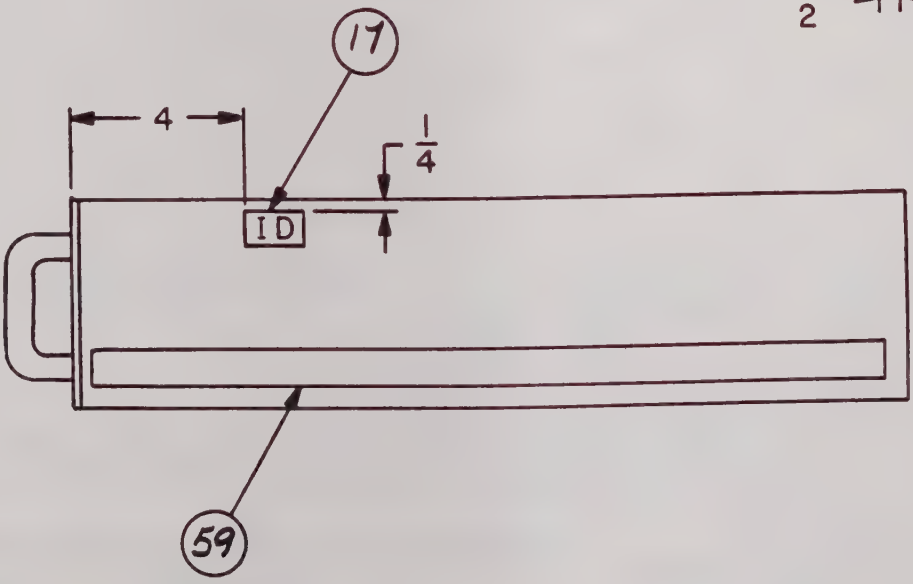
POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY L. GRUCELLA DATE 4-9-80	CHECKED DATE	TITLE PCM BIT SYNCHRONIZER TOP ASSEMBLY - MODEL 335	CODE IDENT NO. 20747	DWG. NO. PL356-0002-506 SHEET 2 OF	REV K

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		356-0002-505		L	PARENT 335-10-22-P0	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	036	216-0213-039	216-0213-039		DECAL CONN IDENT	
1	048	355-0002-501		E	MOD 335 CHASSIS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MANUAL MODEL 335	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0836-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	108	460-0980-501		E	LDR024-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	112	460-0986-501		H	INP050-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	116	460-1065-501		W	HLF001-1	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		M	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	120	460-1097-501		G	DDR030-1	
1	122	460-1823-501		B	ACL009-1	
1	123	460-1105-501		H	XTL028-1	
1	125	460-1161-503		J	BLD001-3	
1	126	460-1164-502		D	BLD002-2	

PL 356-0002-505 L
SHEET 3





AYDIN MONITOR SYSTEMS

800-0153-A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-505	L
	SHEET 4 OF	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		22 Feb 83	RS Volz
K	REVISED PER ECO 08630 R.P.K. 11-21-82		29 Nov 83	RSVolz

ATP: A) 297-0477-501 WIRE LIST A) 730-2016
ATP ADDEN: A) 297-0477-502
ATP ADDEN: A) 297-0477-507
CIR. CD. TEST PROC: A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
PORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA	4-11-80	ENGINEER	D.R. McKINNEY	4-18-80	DWG NO. PL356-0002-507	REV K
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80		
DRAFTING	E.S.	5-5-80	MFG 5/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

800-0068

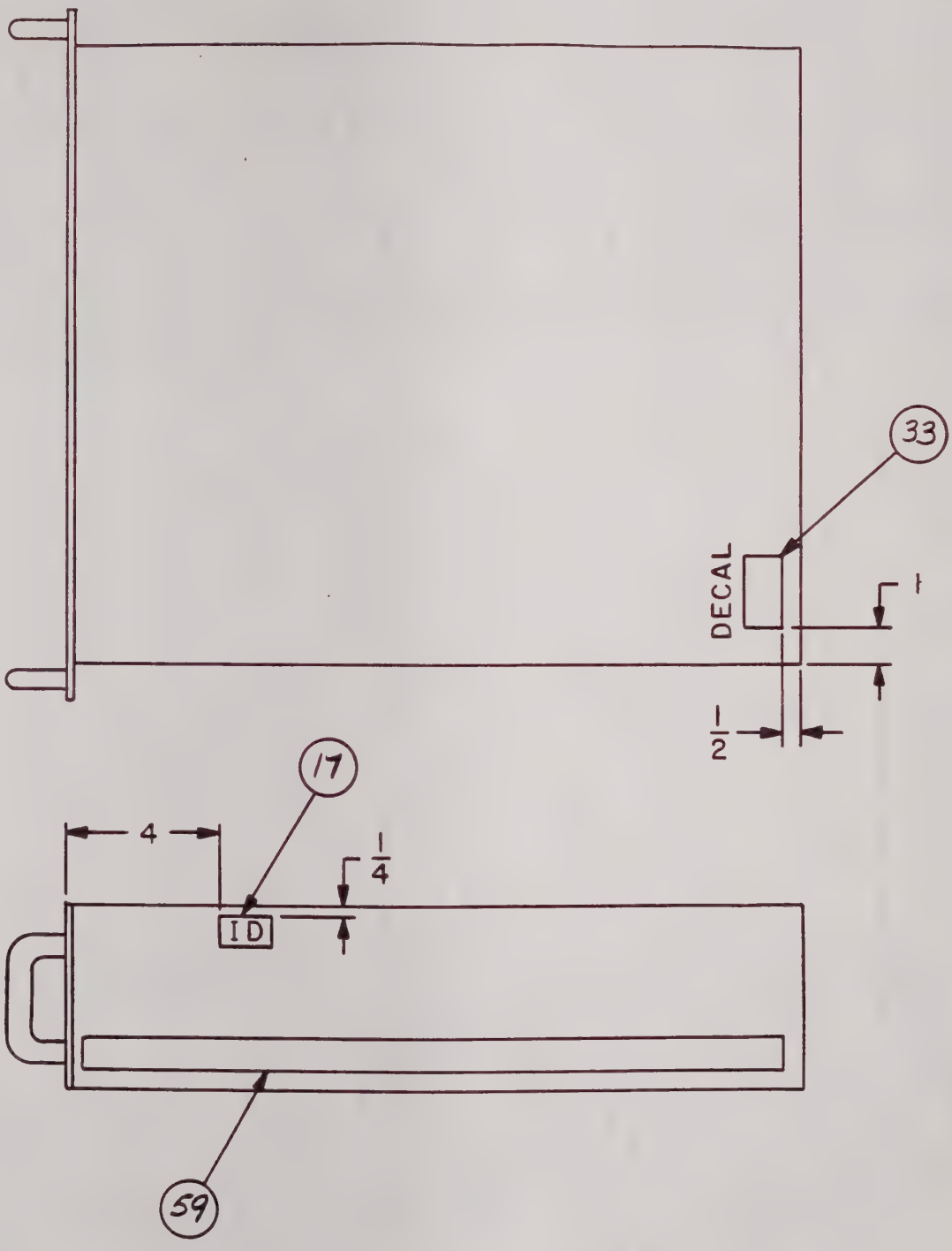
800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	PDT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY	8/12	8/12	8/12	8/12	8/12											
	FILE A4	INP 050-1		BLD 001-3	BLD 002-2			DDR 030	DDR 030	LDR 023		LDR 024-1					
	KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/36					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY	CHECKED	TITLE	CODE IDENT NO.	DWG. NO.	REV
L. GRUCELLA		PCM BIT SYNCHRONIZER TOP ASSEMBLY - MODEL 335	20747	PL356-0002-507	K
DATE 4-9-80	DATE			SHEET 2 OF	

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DE
		356-0002-506		K	PARENT 335-11-22	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-009			CONNECTOR DECAL	
1	048	355-0002-501		E	MOD 335 CHASSIS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MAN-335	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0836-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	108	460-0980-501		E	LDR024-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	112	460-0986-501		H	INP050-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	116	460-1065-501		W	HLF001-1	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		L	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	121	460-1097-502		G	DDR030-2	
1	122	460-1823-501		A	ACL009-1	
1	123	460-1105-501		H	XTL028-1	
1	125	460-1161-503		G	BLD001-3	
1	126	460-1164-502		D	BLD002-2	
1	131	481-0026-30			UX801-30	



AYDIN MONITOR SYSTEMS

800-0153A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-506	K
	SHEET 4 OF	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 JFS. 2-8-83		22 Feb 83	RS Volz
K	REVISED PER ECO 08630 RFK. 11-21-83		29 Nov 83	[illegible]

ATP: A) 297-0477-501
ATP ADDEN: A) 297-0477-502
ATP ADDEN: A) 297-0477-503
ATP ADDEN: A) 297-0477-508

CIR. CD. TEST PROC: A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA	4-11-80	ENGINEER	D.R. McKINNEY	4-18-80	DWG NO.	REV
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80	PL356-0002-508	K
DRAFTING	E.S.	5-5-80	MFG 5/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

800-0066

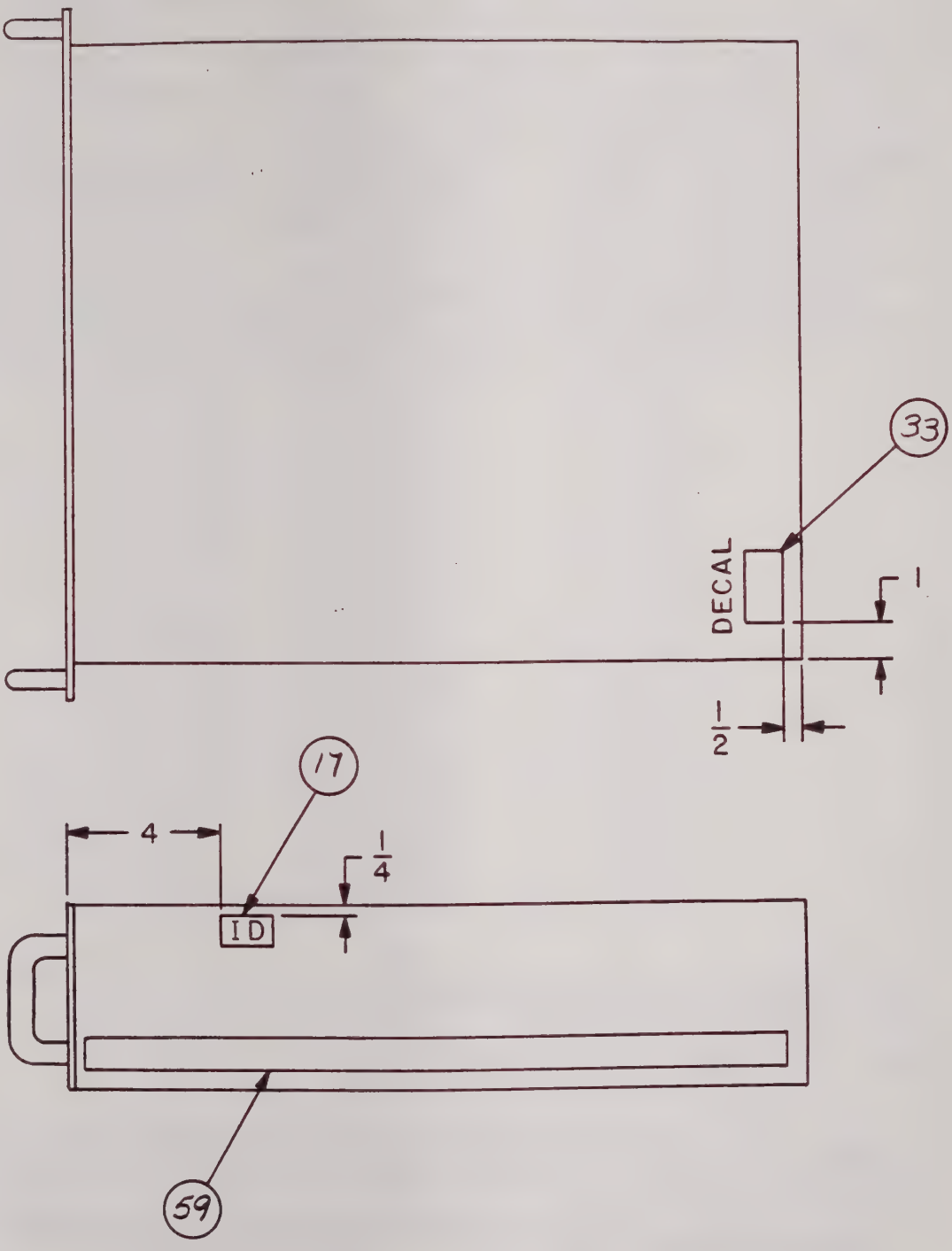
800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	PDT 020	HLF 001-2	PLL 102	CSD 002	CCR 036	ACL 009-1	GP 018-1				
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34	8/16				
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY	8/12	8/12	8/12	8/12	8/12											
	FILE A4	INP 050-2						DDR 030	DDR 030	LDR 023		LDR 024-2					
	KEY	18/22						8/12	8/12	4/26		10/36					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY	CHECKED	TITLE	CODE IDENT NO.	DWG. NO.	REV
DATE	DATE	PCM BIT SYNC ASSY MODEL 335	20747	356-0002 509	K
				SHEET 2 OF	

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		356-0002-507		K	PARENT 335-SINGER	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-017	216-0213-017		DECAL CONN ID	
1	048	355-0002-501		E	MOD 335 CHASSIS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MAN-335	
1	082	298-0373			MANUAL	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0836-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	108	460-0980-501		E	LDR024-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	112	460-0986-501		H	INP050-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	116	460-1065-501		W	HLF001-1	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		L	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	120	460-1097-501		G	DDR030-1	
1	122	460-1823-501		A	ACL009-1	
1	123	460-1105-501		H	XTL028-1	
1	125	460-1161-503		G	BLD001-3	
1	126	460-1164-502		D	BLD002-2	



AYDIN MONITOR SYSTEMS

800-0153A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-501	K
	SHEET 4 OF	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J. MATHER
C	REVISED PER ECO 05636 BAKER 10-10-80		10-21-80	F. HINKLE
D	REVISED PER ECO 05732 BAKER 10-27-80		10-27-80	R.S. VOLZ
E	REVISED PER ECO 06065 BAKER 3-3-81		3-4-81	R.S. VOLZ
F	REVISED PER ECO 06192 JSG		3-26-81	A.T.F.
G	REVISED PER ECO 06203 BAKER 3-28-81		4-14-81	R.S. VOLZ
H	REVISED PER ECO 06778 CMT 9-8-81		9-19-81	R.S. VOLZ
J	REVISED PER ECO 08206 J.F.S. 2-8-83		22 Feb 83	RS Volz
K	REVISED PER ECO 08630 R.P.K. 11-21-83		29 Nov 83	RSVolz

ATP ADDEN: A) 297-0477-502
ATP: A) 297-0337
CIR. CD. TEST PROC: A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—																			

AYDIN MONITOR SYSTEMS
PORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA	4-11-80	ENGINEER	D.R. McKINNEY	4-18-80	DWG NO.	REV
CHECKED	D.D. MOUAT	4-29-80	APPROVED	D.D. MOUAT	4-29-80	PL356-0002-509	K
DRAFTING	E.S.	5-5-80	MFG 5/8/80 WASLICK	R. MARGRAFF	5-1-80	SHEET 1 OF 4	

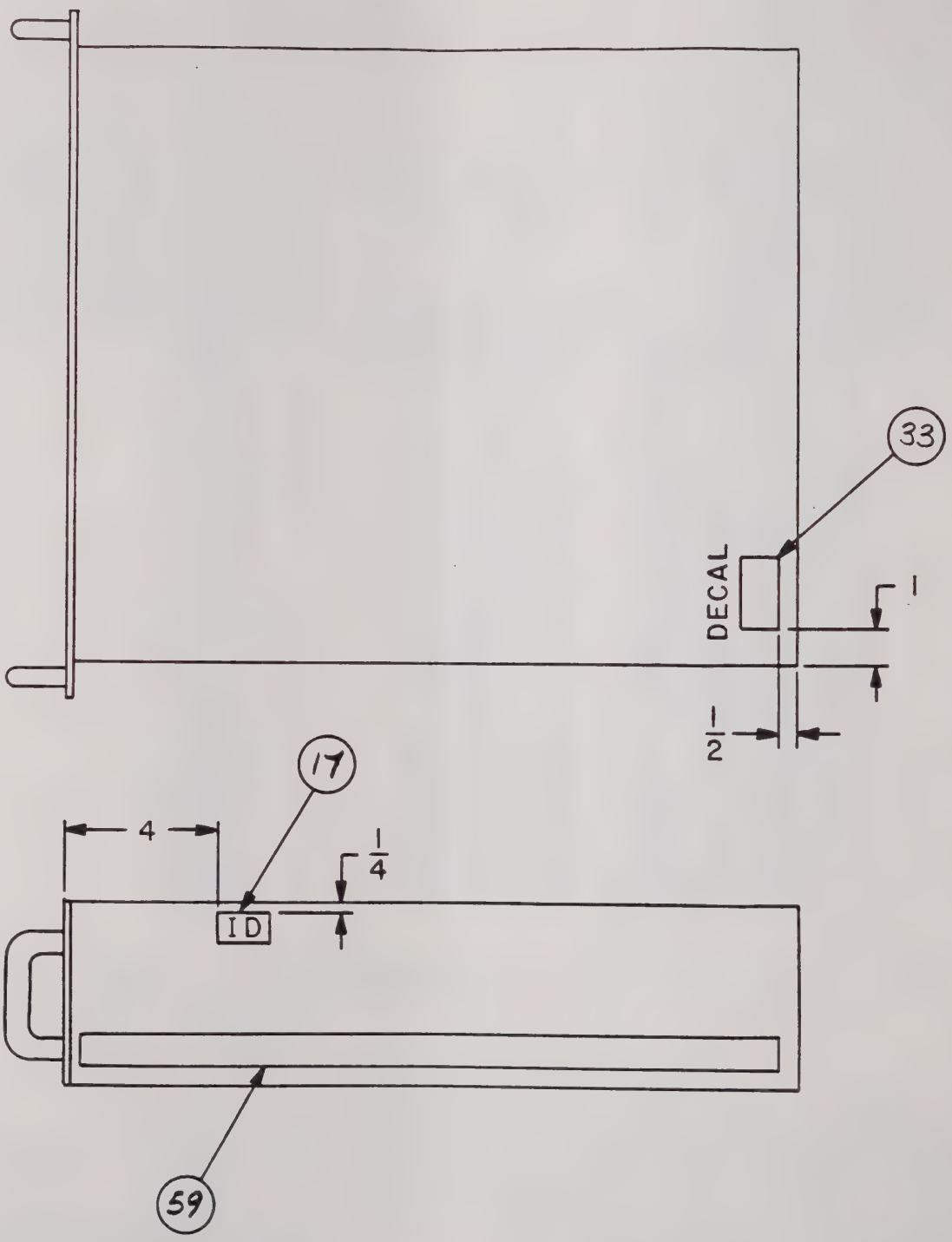
800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		356-0002-508		K	PARENT 335-10-(ENGL AND)	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-043	216-0213-043		DECAL CONN IDENT	
1	048	355-0002-502	355-0002-502	F	MODEL 335 CHASSIS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MANUAL MODEL 335	
1	082	298-0354	298-0354		MANUAL MODEL 355 ADD	
1	089	354-0160-501	354-0160-501	A	MOD 335 ACC	
2	095	790-0621	790-0621		CABLE ASSY	
1	100	460-0836-501	460-0836-501	G	DDR022-1	
1	101	460-0903-502	460-0903-502	W	VAF026-2	
1	102	460-0906-501	460-0906-501	N	THD001-1	
1	103	460-0908-501	460-0908-501	AB	VAF027-1	
1	104	460-0921-501	460-0921-501	X	SLC029-1	
1	106	460-0927-501	460-0927-501	R	SLC030-1	
1	107	460-0949-501	460-0949-501	E	LDR023-1	
1	108	460-0980-501	460-0980-501	E	LDR024-1	
1	109	460-0981-501	460-0981-501	E	BCD001-1	
1	110	460-0982-501	460-0982-501	J	CCR036-1	
1	111	460-0985-501	460-0985-501	F	PDC001-1	
1	112	460-0986-501	460-0986-501	H	INP050-1	
1	113	460-1058-501	460-1058-501	P	PDT020-1	
1	114	460-1059-501	460-1059-501	R	PLL102-1	
1	116	460-1065-501	460-1065-501	W	HLF001-1	
1	117	460-1085-501	460-1085-501	C	LDY001-1	
1	118	460-1095-501	460-1095-501	M	CSD002-1	
4	119	460-1096-501	460-1096-501	C	PSR021-1	
2	120	460-1097-501	460-1097-501	G	DDR030-1	
1	122	460-1823-501	460-1823-501	C	ACL009-1	
1	123	460-1105-501	460-1105-501	H	XTL028-1	
1	124	460-1161-501	460-1161-501	J	BLD001-1	
1	126	460-1164-502	460-1164-502	D	BLD002-2	
2	127	460-1638-501	460-1638-501	B	CUP001-1	

?

PL 356-0002-508 K

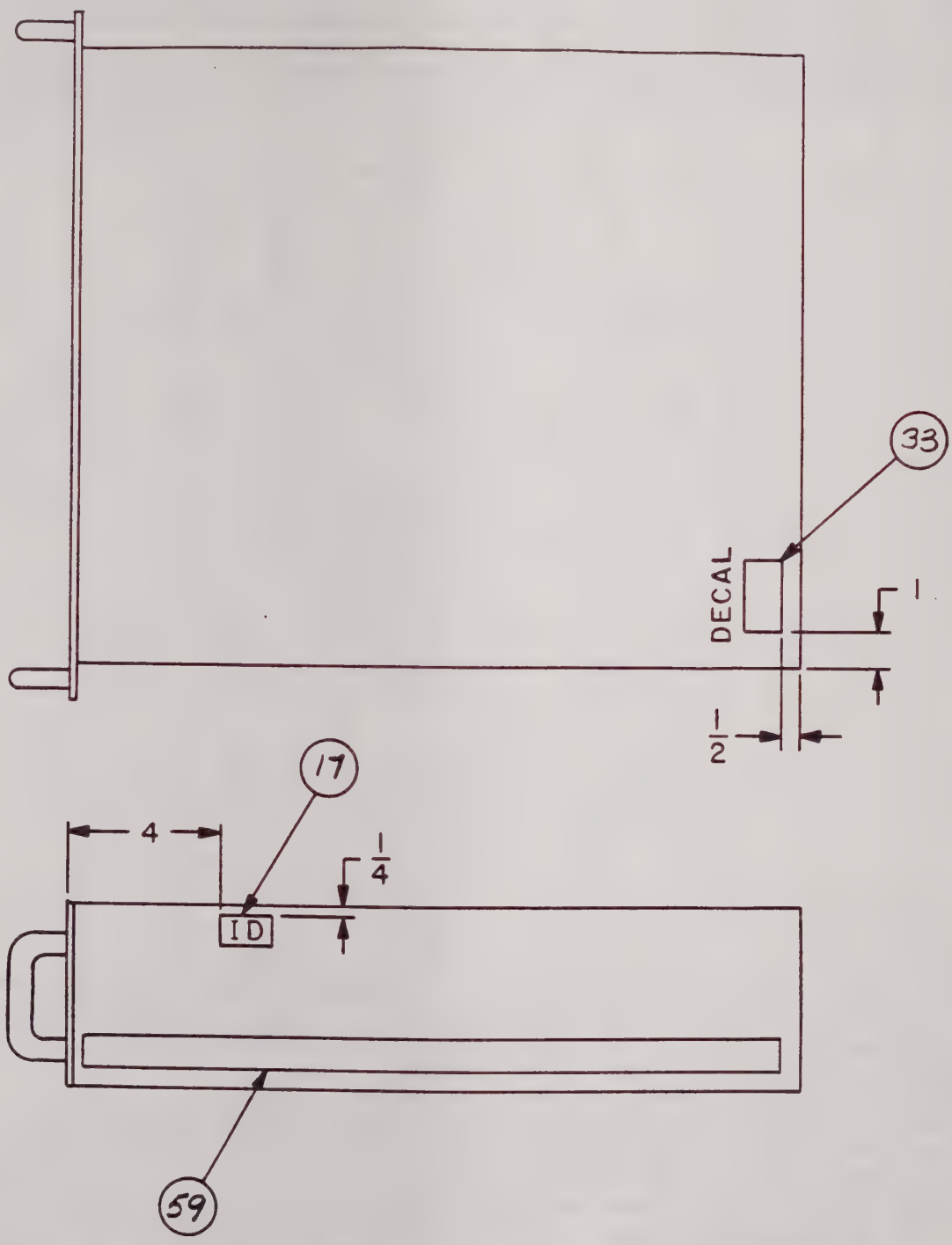
SHEET 3



AYDIN MONITOR SYSTEMS

800-0153A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-509	K
	SHEET 4 OF	



AYDIN MONITOR SYSTEMS

800-0153A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-508	K
	SHEET 4 OF	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 08765 R.P.K.		4Nov83	RS Vol2
C	REVISED PER ECO 08630 R.P.K. 11-21-83		29 Nov 83	[illegible]
D	REVISED PER ECO 08797 K.M.		6DEC83	RS Vol2

ATP: A) 297-0477-501
ATP ADDENDUM: A) 297-0477-504
ATP ADDENDUM: A) 297-0807
CIRCUIT CARD PROC.: A) 297-0481

WIRE LIST MOD.: A) 730-2229
RACK MTG: C) 353-0071

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—																						

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 1209-30

DRAWN	J. SHIELDS	6-22-83	ENGINEER	RS Vol2	11Nov83	DWG NO.	REV
CHECKED	ES		APPROVED	RS Vol2	11Nov83	PL356-0002-510	D
DRAFTING	E Stricker	7-1-83				SHEET 1 OF 4	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001-3	PDT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/30	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY	8/12	8/12	8/12	8/12	8/12											
	FILE A4	INP 050-1		BLD 001-1	BLD 003-1	UX 801-30		DDR 030-2	DDR 030-2	LDR 023		LDR 024-1					
	KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/30					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY J. SHIELDS
DATE 6-22-83
CHECKED
DATE

TITLE PCM BIT SYNCHRONIZER TOP ASSEMBLY - MODEL 335

CODE IDENT NO. 20747

DWG. NO. PL 356-0002-510

SHEET 2 OF

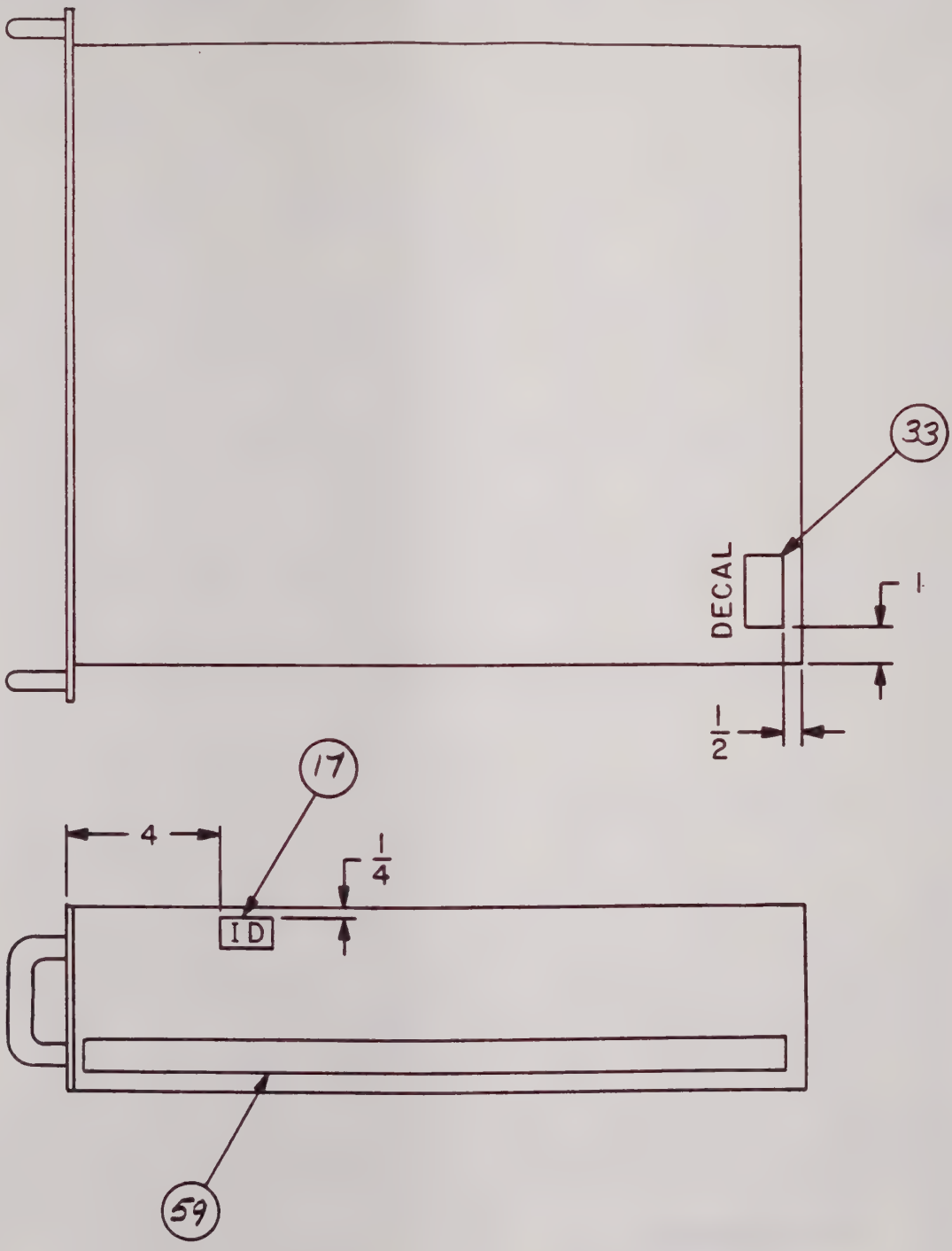
REV D

*** SINGLE LEVEL BILL BY ITEM ***

LB.MFG.ITEM

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.
		356-0002-509		K	PARENT 335 (TIPS)	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-003			CONNECTOR DECAL	
1	048	355-0002-503		E	335 CHS	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MAN-335	
1	082	298-0254			MANUAL ADDENDUM	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0836-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	115	460-0986-502		H	INP050-2	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		L	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	120	460-1097-501		G	DDR030-1	
1	122	460-1823-501		A	ACL009-1	
1	123	460-1105-501		H	XTL028-1	
1	128	460-1065-502		W	HLF001-2	
1	129	460-1341-501		B	GP018-1	
1	130	460-0980-502		E	LDR024-2	

PL356-0002-509 K
SHEET 3



AYDIN MONITOR SYSTEMS

800-0155A

CODE IDENT NO.	DWG NO.	REV
20747	PL956-0002-510	D
	SHEET 4 OF	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED

ATP : A) 297-0477-501
ATP ADDENDUM : A) 297-0822-501
CIRCUIT CARD TEST PROCEDURE : A) 297-0481

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION																							

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
TOP ASSEMBLY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 1230-51

DRAWN	C. FAZIO	7/29/83	ENGINEER	RSV.12	12 Sept 83	DWG NO. PL 356-0002-511	REV A
CHECKED	ES		APPROVED	RSV.12	12 Sept 83		
DRAFTING	E Stucker	9-13-83				SHEET 1 OF 4	

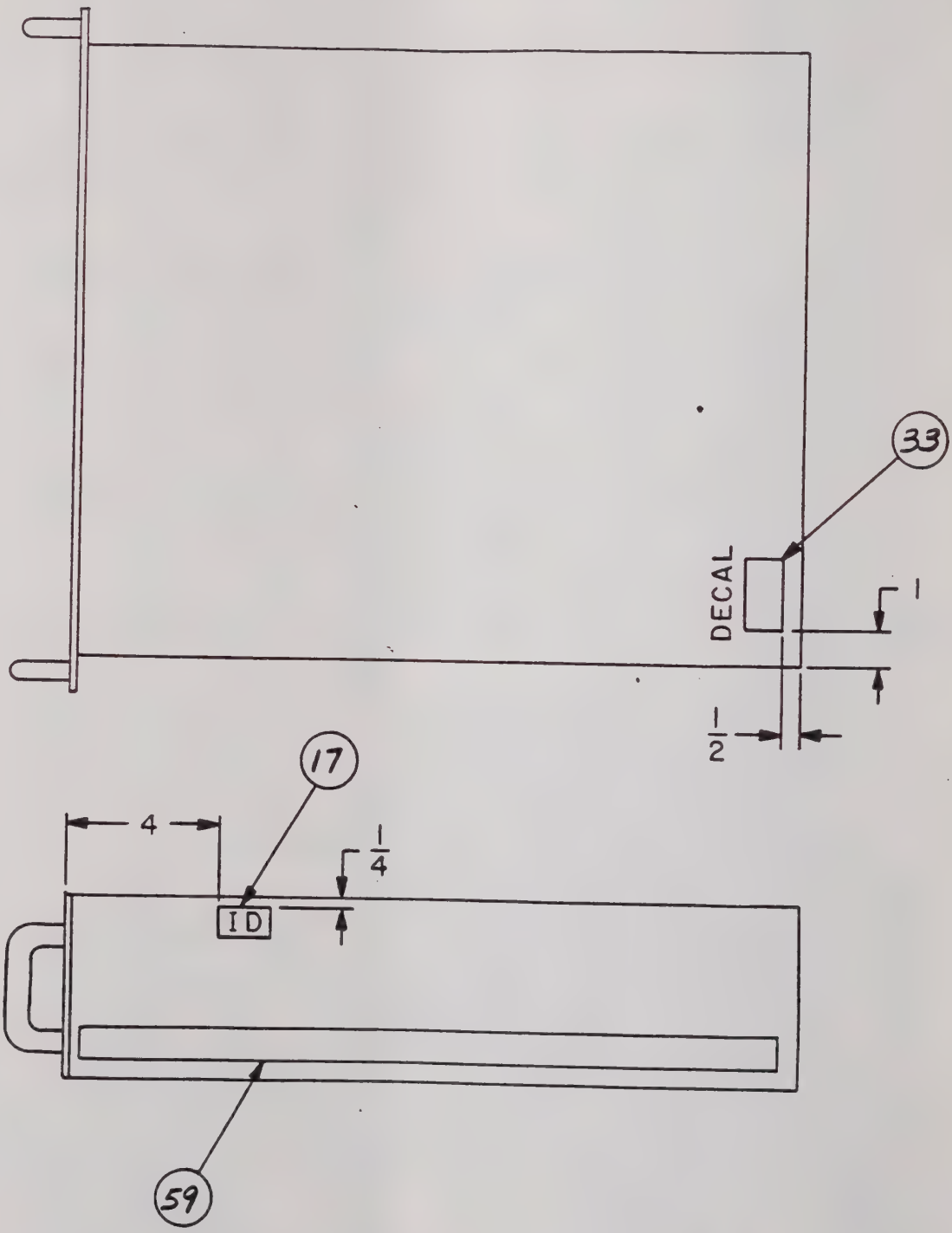
800-0066

800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1	VAF 027	SLC 029	VAF 026-2	SLC 030	THD 001	PDT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY	8/12	8/12	8/12	8/12	8/12											
	FILE A4	INP 050-1	INP 065	SPARE	REG 062	LDR 034-1	SPARE	DDR 030	DDR 030	LDR 023	SPARE	LDR 024-1					
	KEY	18/22	8/12	12/38	12/38	8/12		8/12	8/12	4/26		10/36					

POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY	CHECKED	TITLE	CODE IDENT NO.	DWG. NO.	REV
C. FAZIO		PCM BIT SYNCHRONIZER TOP ASSEMBLY, MODEL 335	20747	PL35L-0002-511	A
DATE 9-29-83	DATE			SHEET 2 OF	



AYDIN MONITOR SYSTEMS

800-0153A

CODE IDENT NO.	DWG NO.	REV
20747	PL356-0002-511	A
	SHEET 4 OF	

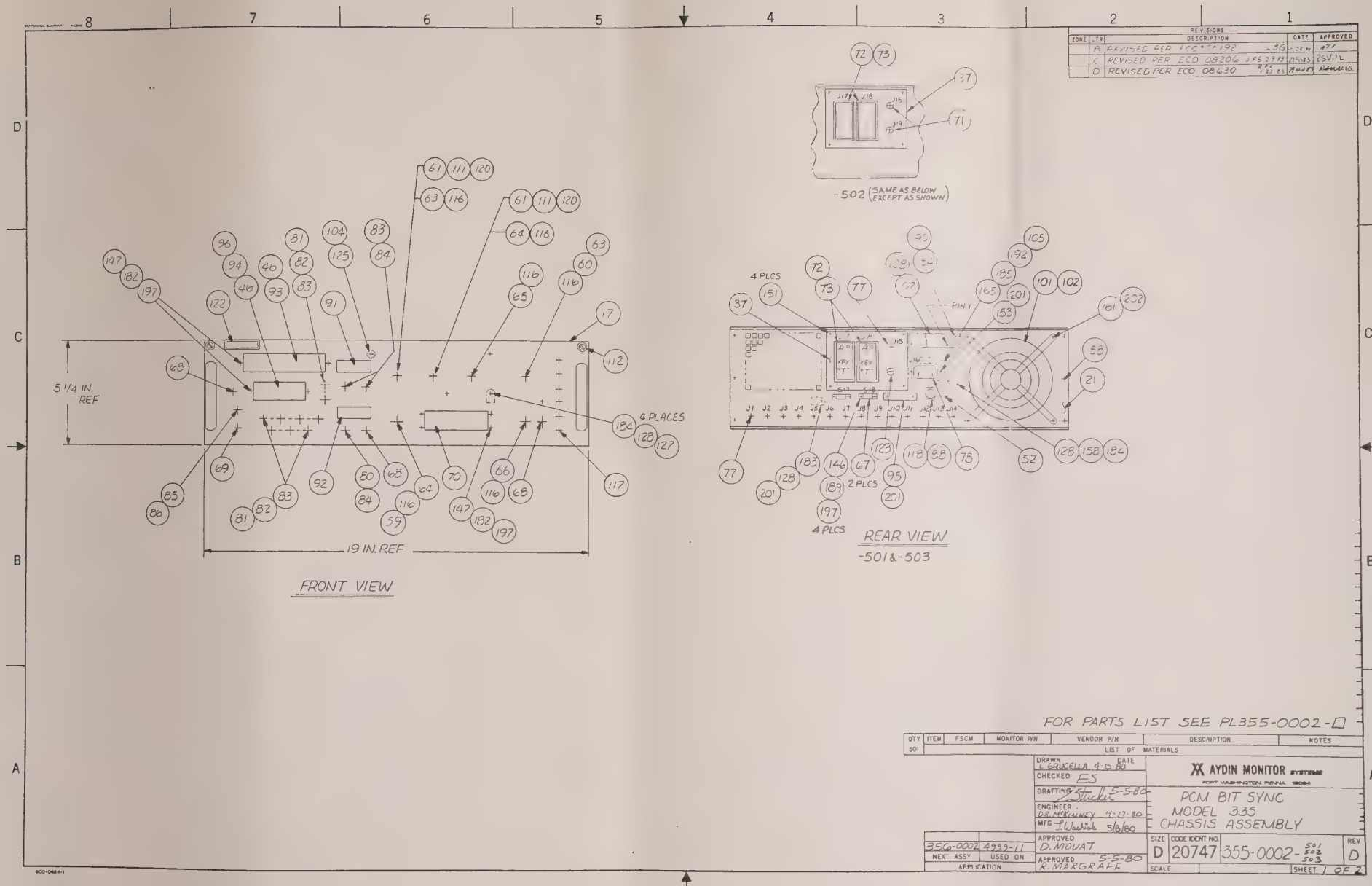
800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1	VAF 027	SLC 029	VAF 026	SLC 030	THD 001	POT 020	HLF 001	PLL 102	CSD 002	CCR 036	ACL 009-1					
	KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
	FILE A2		XTL 028-1	BCD 001	PDC 001	LDY 001											
	KEY		8/12	8/12	18/22	8/12											
	FILE A3	PSR 021	PSR 021	PSR 021	PSR 021	DDR 022											
	KEY																
	FILE A4	INP 050-1		BLD 001-1	BLD 002-2	CUP 001	CUP 001	DDR 030	DDR 030	LDR 023		LDR 024-1					
	KEY	18/22	8/12	12/38	12/38	8/12	8/12	8/12	8/12	4/26		10/36					

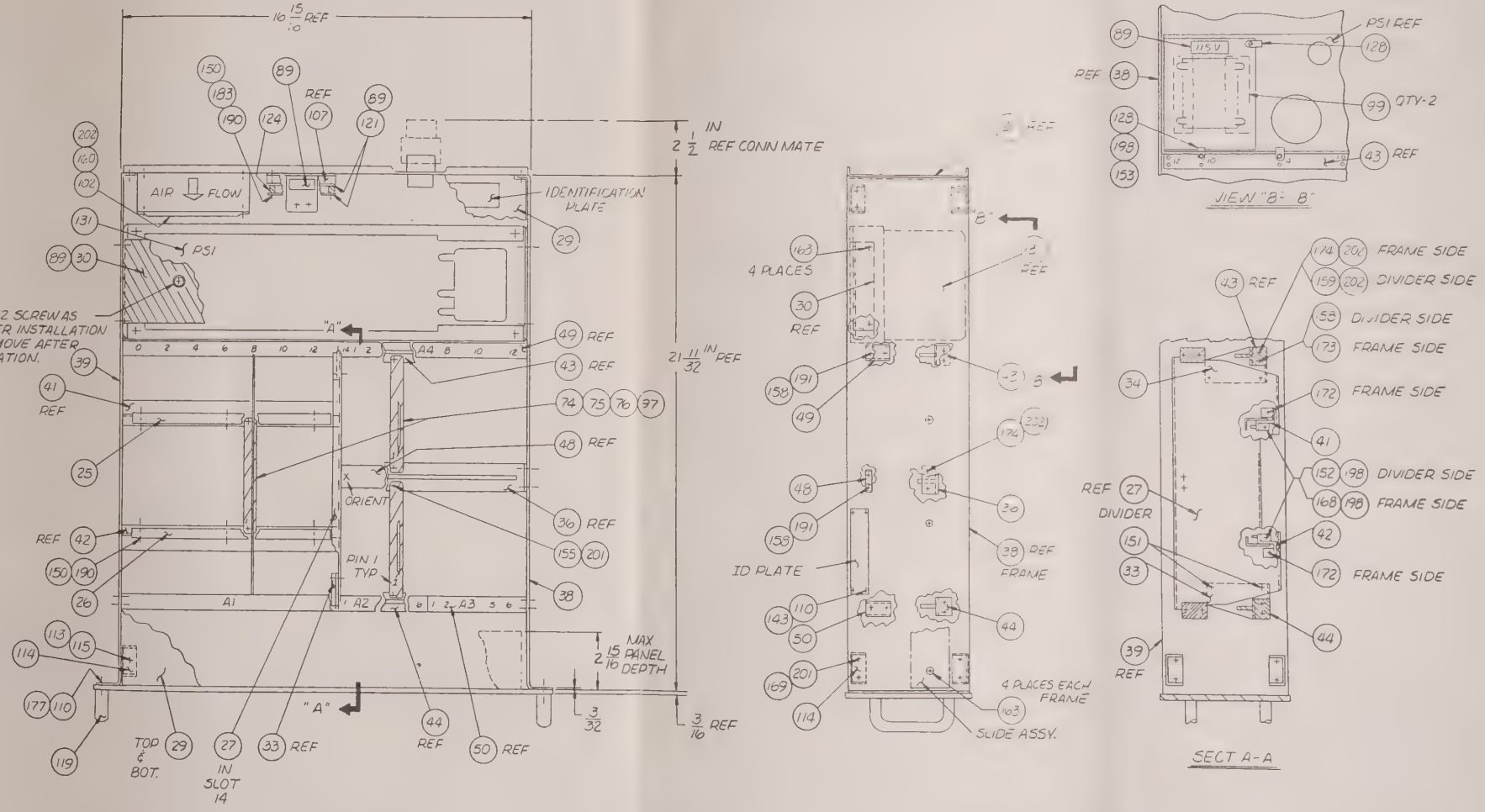
POSITION NO.		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
KEY AND CONNECTOR POSITIONS AND P.C. CARD TYPES	FILE A1																
	KEY																
	FILE A2																
	KEY																
	FILE A3																
	KEY																
	FILE A4																
	KEY																

DRAWN BY L. GRUCELLA DATE 4-9 80	CHECKED DATE	TITLE PCM BIT SYNCHRONIZER TOP ASSEMBLY MODEL 335	CODE IDENT NO. 20747	DWG. NO. PL356-0002-508 SHEET 2 OF	REV K

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		356-0002-511		A	PARENT 335-10-20-30 -TO-905	
1	017	124-013-001	PER SPEC	D	NAMEPLATE SELF ADHES	
1	033	216-0213-044	216-0213-044		DECAL CONN IDENT	
1	048	355-0002-504		A	MODEL 335 CHASSIS-905	
1	059	132-031-005	03000-0107-14-1	A	CHASSIS SLIDE 20 IN	
1	077	298-0253		D	MANUAL MODEL 335	
1	078	298-0601	298-0601		MANUAL ADD MODEL 335	
1	089	354-0160-501		A	MOD 335 ACC	
1	100	460-0833-501		G	DDR022-1	
1	101	460-0903-502		W	VAF026-2	
1	102	460-0906-501		N	THD001-1	
1	103	460-0908-501		AB	VAF027-1	
1	104	460-0921-501		X	SLC029-1	
1	106	460-0927-501		R	SLC030-1	
1	107	460-0949-501		E	LDR023-1	
1	108	460-0980-501		E	LDR024-1	
1	109	460-0981-501		E	BCD001-1	
1	110	460-0982-501		J	CCR036-1	
1	111	460-0985-501		F	PDC001-1	
1	112	460-0986-501		H	INP050-1	
1	113	460-1058-501		P	PDT020-1	
1	114	460-1059-501		R	PLL102-1	
1	116	460-1065-501		W	HLF001-1	
1	117	460-1085-501		C	LDY001-1	
1	118	460-1095-501		M	CSD002-1	
4	119	460-1096-501		C	PSR021-1	
2	120	460-1097-501		G	DDR030-1	
1	123	460-1105-501		H	XTL028-1	
1	125	460-1437-501		G	LDR034-1	
1	126	460-1438-501		B	REG062-1	
1	130	460-1823-501		C	ACL009-1	
1	132	460-1888-501		0	INP065-1	



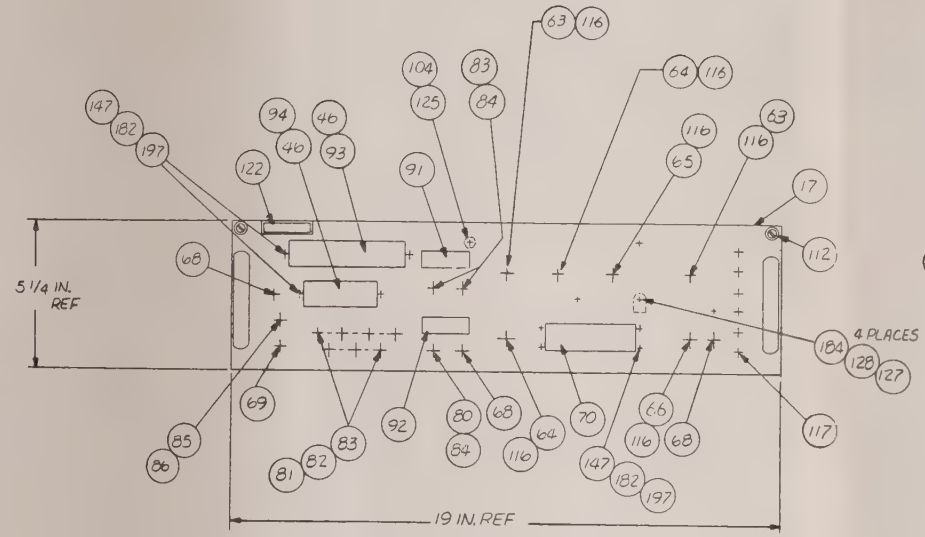
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B REVISED PER ECO 08206 JFS 2983
C REVISED PER ECO 08206 JFS 2983
D REVISED PER ECO 08630
-502 (SAME AS BELOW EXCEPT AS SHOWN)
5 1/4 IN. REF
19 IN. REF
4 PLACES
FRONT VIEW
4 PLCS
2 PLCS
4 PLCS
REAR VIEW
-501&-503
FOR PARTS LIST SEE PL355-0002-□
QTY ITEM FSCM MONITOR P/N VENDOR P/N DESCRIPTION NOTES
501
LIST OF MATERIALS
DRAWN L. GRUCELLA 4-15-80
CHECKED ES
DRAFTING 5-5-80
ENGINEER D.R. McKinney 4-17-80
MFG S. Washick 5/8/80
APPROVED D. MOUAT
APPROVED 5-5-80 R. MARGRAFF
AYDIN MONITOR SYSTEMS
PCM BIT SYNC
MODEL 335
CHASSIS ASSEMBLY
SIZE D
CODE IDENT NO. 20747
355-0002-501 502 503
REV D
SCALE
SHEET 1 OF 2
356-0002 4999-11
NEXT ASSY USED ON
APPLICATION



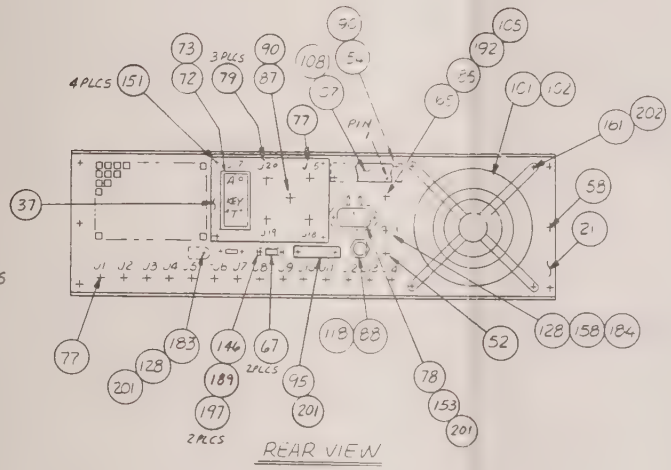
SIZE	CODE IDENT NO.		REV
D	20747	355-0002-501 502 503	D
SCALE		SHEET 2 OF 2	

800-0564-2

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED



FRONT VIEW



REAR VIEW

FOR PARTS LIST SEE PL355-0002-504

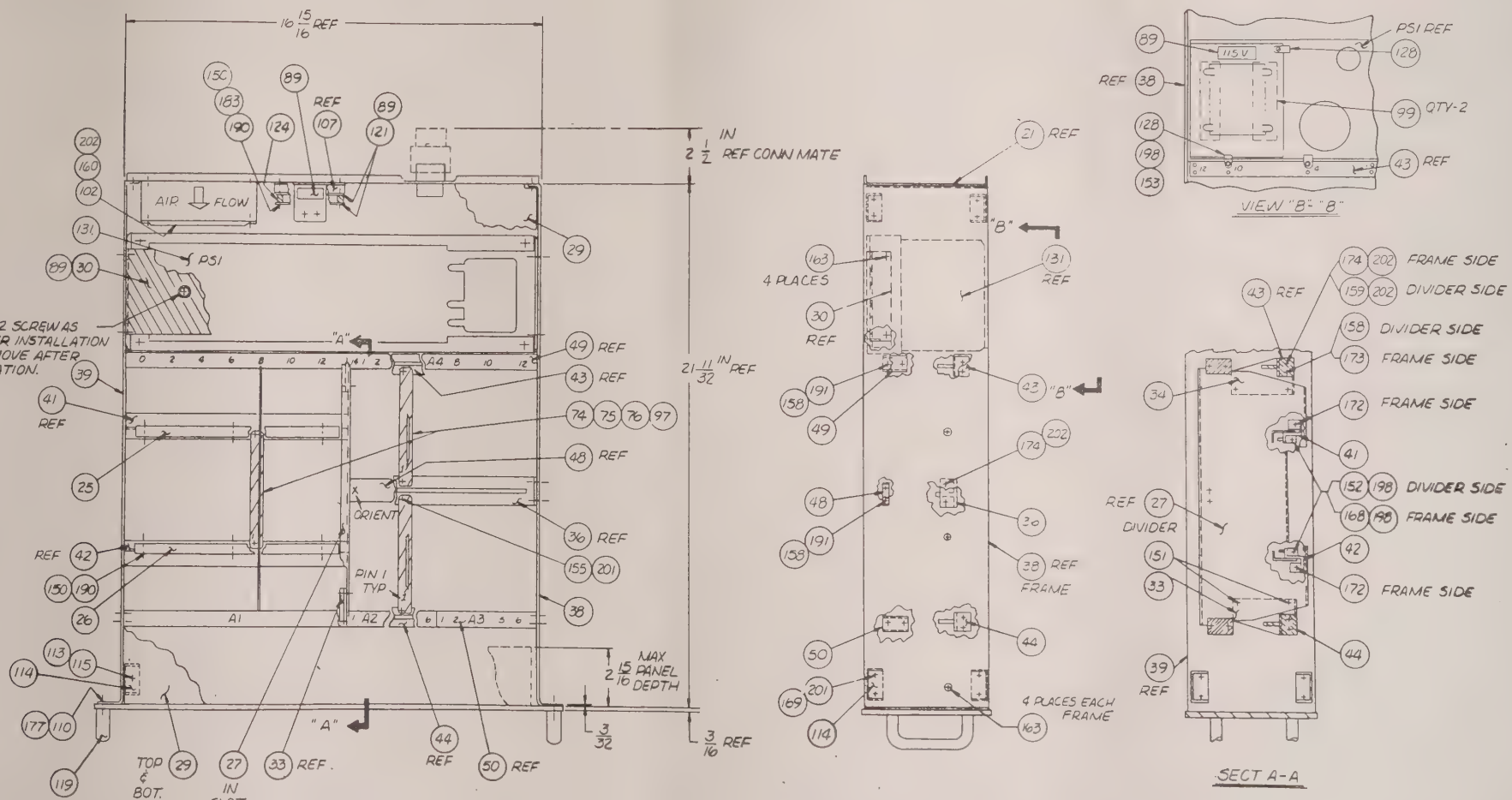
QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501			LIST OF MATERIALS			

DRAWN C. FAZIO DATE 8-5-83	AYDIN MONITOR SYSTEMS FORT WASHINGTON, PENNA. 19034	
CHECKED ES	PCM BIT SYNC MODEL 335 CHASSIS ASSEMBLY	
DRAFTING S Stuckey 8-24-83		
ENGINEER KSW2 24AUG 83		
MFG 8/23/83		
APPROVED KSW2 24AUG 83	SIZE D	CODE IDENT NO. 20747
APPROVED	SCALE	SHEET 1 OF 2

NEXT ASSY	USED ON
350-0002	1230-51
APPLICATION	

355-0002-504 REV A

800-0864-1



SIZE	CODE IDENT NO.		REV
D	20747	355-0002-504	A
SCALE		SHEET 2 OF	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J.MATHER
C	REVISED PER ECO 05587 BAKER 10-10-80		10-16-80	J.MATHER
D	REVISED PER ECO 06192 JSG		3-26-81	ATF
E	REVISED PER ECO 08206 J.F.S. 2-10-83		22FEB83	RSVolz
F	REVISED PER ECO 08630 RPK 11-21-83		11-29-83	R. MARGRAFF
G	REVISED PER ECO 08861 KEN MAC 2-22-83		1-3-84	J.C. Boytim
H	REVISED PER ECO 09049 R.B. 8MAR84		14MAR84	RSVolz

WIRE LIST: A) 730-1702
WIRE LIST, LIBRARY: A) 760-0219
R. PANEL HARNESS: D) 790-0415
F. PANEL HARNESS: D) 790-0454

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION																							

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER CHASSIS ASSEMBLY MODEL 335

CODE IDENT 20747
CONTRACT NO. 4911-11

DRAWN	L.GRUCELLA		ENGINEER	D.R.McKINNEY	4-18-80	DWG NO. PL355-0002-501	REV H
CHECKED	D.D.MOUAT	4-29-80	APPROVED	D.D.MOUAT	4-29-80		
DRAFTING	E.S.	5-5-80	MFG. 5-8-80 WASHICK	R.MARGRAFF	5-9-80	SHEET 1 OF 6	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
FILE A1	■	■	■	■	■	■	■									
KEY	10/16	8/22	12/22	8/22	10/30	8/16	12/32	12/30	12/34	8/22	12/34					
FILE A2		■	■	■	■											
KEY		8/12	8/12	13/22	8/12											
FILE A3	■	■	■	■	■											
KEY	8/12	8/12	8/12	8/12	8/12											
FILE A4	■	■	■	■	■	■	■	■	■	■	■					
KEY	18/22		12/38	12/38	8/12		8/12	8/12	4/26		10/30					

INDICATES P.C. CONN AND KEY INSTALLED

POSITION NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
FILE A1																
KEY																
FILE A2																
KEY																
FILE A3																
KEY																
FILE A4																
KEY																

INDICATES P.C. CONN AND KEY INSTALLED

DRAWN BY L. GRUCELLA DATE 4-11-80	CHECKED DATE	TITLE PCM BIT SYNCHRONIZER CHASSIS ASSEMBLY, MODEL 335	CODE IDENT NO. 20747 DWG. NO. PL355-0002-501 SHEET 2 OF	REV H

		355-0002-501		-	PARENT MOD 335 CHASSIS	
C		113-016-002	MIL-W-16878D/1	C	WIRE INSUL STR 22 BLK	
.5		113-006-004	MIL-W-16878D/1	C	WIRE INSUL STR 22 GRN	
.02		113-008-221	1853-1	B	WIRE INSUL STR 26 WHT	
90		113-217-002	ITWP267U	F	WIRE TW PR 26 BLK/GRN	
35		113-004-002	1857/19-2	A	WIRE INSUL STR 18 BLK	
2		113-004-003	MIL-W-16878 D/1	A	WIRE INSUL STR 18 RED	
20		113-004-005	MIL-W-16878 D/1	A	WIRE INSUL STR 18 YEL	
10		113-004-010	MIL-W-16878 D/1	A	WIRE INSUL STR 18 VIO	
20		113-008-002	MIL-W-16878D/1	B	WIRE INSUL STR 26 BLK	
4		113-219-222	3221	B	CABLE SHLD 2 COND 22	
15		113-006-003	MIL-W-16878D/1	C	WIRE INSUL STR 22 RED	
15		113-006-010	MIL-W-16878D/1	C	WIRE INSUL STR 22 VIO	
3		113-205-006	SEE SPEC	E	CAB UNSHLD 6 COND 26	
15		113-004-001	MIL-W-16878 D/1	A	WIRE INSUL STR 18 WHT	
20		113-008-005	MIL-W-16878D/1	B	WIRE INSUL STR 26 YEL	
6		113-205-012	MIL-W-16878	E	CAB UNDHLD 12 COND 26	
8		113-205-025	MIL-W-16878	E	CAB UNSHLD 25 COND 26	
10		113-004-004	MIL-W-16878 D/1	A	WIRE INSUL STR 18 GRN	
12		113-219-218	3241	B	CABLE SHLD 2 COND 18	
35		113-305-001	8417	D	CABLE SHLD 1 COND 25	
1	017	201-0525-002	201-0525-002	C	PANEL FRONT MODEL 335	
1	021	203-0600-001			PANEL REAR	
1	025	205-0595-001			BRACKET	
1	026	205-0595-002			BRACKET	
1	027	205-0596-001			BRACKET	
2	029	206-0258-001			COVER	
1	030	206-0260-001		B	COVER	
1	033	207-0601-001			PLATE	
1	034	207-0601-002			PLATE	
1	036	208-0297-001			SUPPORT	
1	037	207-0704-004	207-0704-004	E	PLATE CONN MTG	
1	038	210-0293-001			SIDE FRAME	
1	039	210-0293-002			SIDE FRAME	
1	041	211-0234-001			ANGLE	
1	042	211-0234-002			ANGLE	
1	043	211-0235-001			ANGLE	
1	044	211-0235-002			ANGLE	
8	046	217-0345-001		Ø	MOD CONN	
1	048	225-0198-001			BAR	
1	049	225-0199-001			BAR	
1	050	225-0199-002			BAR	
1	052	351-0273-501	351-0273-501	C	INSUL GRND	S7
2	063	107-025-001	1030-F-101-2N	AG	SW RTY 30 DEG 2 POS	S1 S6
2	064	107-025-019	1030F-102-4N	AG	SW RTY 30 DEG 4 POS	S5 S13
1	065	107-025-020	1030F-104-9N	AG	SW RTY 30 DEG 9 POS	S4
1	066	107-026-014	1036F-101-6N	L	SW RTY 36 DEG 6 POS	S3
2	067	107-107-003	MSS-44	A	SW SLIDE SUBMIN DPDT	S31 S32
3	068	107-112-001	MBS-C-ALO	H	SW BUT MINI TAP PIN C	S2 S14 S15

PL355-0002-501 H
SHT. 3

QTY	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.D
1	069	107-232-002	MTG-106D	D	SW TGL SPDT	S16
1	070	107-328-001	8-Y-352	G	THUMBWH SW ASSY 4 POS	S7
						S8
						S9
						S10
						S11
						S12
2	072	108-101-010	1-202663-8	Z	CONNECTOR 34 POS MALE	J17
						J18
68	073	108-101-100	66106-1	Z	CONN PIN CONT 26-24	
.015	074	108-107-046	200-62-8017-03-	J	CONN CONTACT (LOOSE)	
01	075	108-207-225	7015-041-000-00	C	CONN RECEP 41 POS	A1
						A2
						A3
						A4
56	076	108-207-009	60-5006-3414	C	CONN POLARIZ INSERT	
15	077	108-302-001	8J-27	L	CONN STD RECEPT	J1
						J2
						J3
						J4
						J5
						J6
						J7
						J8
						J9
						J10
						J11
						J12
						J13
						J14
						J15
1	078	108-817-001	5004-6622	F	CONN PWR LINE FILTER	J16
1	080	110-008-006	507-39111432600	C	LAMP INCAND GRN	DS3
7	081	110-008-011	515-0012	C	LAMP CONN CARTRIDGE	
7	082	110-008-013	515-0051	C	LAMP SPEED CLIP	
9	083	110-019-001	507-47573731500	H	LAMP CART RED	XDS1
						XDS2
						XDS14
						XDS15
						XDS16
						XDS17
						XDS18
						XDS19
						XDS20
3	084	110-019-009	250-873814504	H	LMPHOLDER W/O COLLAR	XDS1
						XDS2
						XDS3
1	085	110-027-001	507-45380931610	C	LAMP CART RED	DS21
1	086	110-027-005	508-8745-504	C	LAMPHOLD W/COLLAR	XDS21
1	088	111-005-025	31302.5	B	FUSE 2-1/2 A SLO-BLO	F1
4	089	111-200-001	111-200-001	D	LABEL WARNING 115V	
1	091	112-012-001	260-781	D	METER THIN LINE-HORIZ	MI
1	092	112-015-001	260-780	L	METER THIN LINE-HORIZ	
1	093	112-021-001	749-1506-803	P	DISPLAY LED 6 CHAR	X[illegible]
						XDS5

QTY	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						XDS6
						XDS7
						XDS8
						XDS9
-	094	112-021-002	749-1503-801	J	DISPLAY LED 3 CHAR	XDS11
						XDS12
						XDS13
1	095	112-024-001	550-SS-115VAC-1	A	INDICATOR ELP TIME	M3
7	097	113-406-002	60 8017 0723	A	BUS STRIP VARILOK	
0	099	114-031-001	7361-1	A	TAPE FILM PRESS SENS	
1	101	116-005-001	4600X	N	FAN 115 VAC	
2	102	116-005-004	08122	N	FAN FINGER GUARD	
5	104	118-015-004	1511-1-0519	A	TERM TUR INSUL SOLD	E1
						E2
						E3
						E4
						E6
1	105	118-202-212	32836	N	TERM CRIMP 22-16 #10	
1	107	119-004-008	410-8	A	TERMINAL BLOCK 8 POS	TB1
3	108	119-004-023	410-J	A	TERMINAL BLOCK JUMPER	
1	110	120-004-059	222	C	SEALANT THREAD	
2	112	121-004-003	F7500-10-D-3	J	CAPTIVE SCREW 10-32	
8	113	121-005-001	82-11-140-16	H	FASTENER 1/4 TURN	
8	114	121-005-009	82-45-101-15	H	RECEPTACLE 1/4 TURN	
8	115	121-005-010	82-32-101-20	H	RETAINING WASHER	
6	116	121-115-001	SS-70PL-2	B	KNOB RD POINTED 1/4 S	
6	117	121-200-001	105-0253-001	D	TEST POINT STD BLK	TP1
						TP2
						TP3
						TP4
						TP5
						TP6
1	118	121-303-001	HKP	C	FUSE HOLDER NON IND	XF1
2	119	121-503-001	10923-B-1032-A	K	HANDLE OVAL 3" CTR	
2	121	124-002-008	MS410-8-XP 1A	A	MARKER STRIP 8 POS	
1	122	124-011-002	SEE SPEC	C	LOGO PLATE	
1	123	121-409-032	SS-4815Z-K2915	F	PLUG BUTTON	
2	124	128-003-010	8104-SS-0440	C	STDF HX .19 4-40X3/8	
5	125	128-008-011	9224A140	C	SPACER RD .25D 6 1/4	
4	127	130-203-001	SST1.5	E	CABLE TIE 1-1/4 DIA	
7	128	130-204-001	TA1S8-*	E	MOUNT CABLE TIE	
18	130	135-004-001	56 590 65/3B	A	FERRITE BEAD	
1	131	136-079-003	ET602-1	G	PWR SPLY 5V-12A/15V-3	PS1
4	146	127-109-004	MS51957-04	A	SCR PAN HD 2-56X5\16	
8	147	127-109-006	MS51957-06	A	SCR PAN HD 2-56X7\16	
8	150	127-109-012	MS51957-12	A	SCR PAN HD 4-40X3\16	
8	151	127-109-013	MS51957-13	A	SCR PAN HD 4-40X1\4	
2	152	127-109-014	MS51957-14	A	SCR PAN HD 4-40X5\16	
5	153	127-109-015	MS51957-15	A	SCR PAN HD 4-40X3/8	
2	154	127-109-017	MS51957-17	A	SCR PAN HD 4-40X1\2	
34	155	127-109-019	MS51957-19	A	SCR PAN HD 4-40X3\4	
1	156	127-109-016	MS51957-16	A	SCR PAN HD 4-40X7\16	
2	157	127-109-027	MS51957-27	A	SCR PAN HD 6-32X5\16	
24	158	127-109-028	MS51957-28	A	SCR PAN HD 6-32X3\8	
2	159	127-109-029	MS51957-29	A	SCR PAN HD 6-32X7\16	

		VENDOR #	MFG PART NBR	REV	DESCRIPTION	REF.
	.60	127-109-030	MS51957-30	A	SCR PAN HD 6-32X1\2	
	.61	127-109-123	MS51957-123	A	SCR PAN HD 6-32X9\16	
3	.62	127-109-043	MS51957-43	A	SCR PAN HD 8-32X3\8	
	.63	127-101-052	MS51958-52	A	SCR PAN HD 10-32X7\16	
4	.66	127-105-003	MS24693-03	A	SCR 100 FH 4-40X 5\16	
16	.69	127-105-004	MS24693-04	A	SCR 100 FH 4-40 X 3/8	
4	.72	127-105-025	MS24693-25	A	SCR 100 FH 6-32X 5\16	
2	.73	127-105-026	MS24693-26	A	SCR 100 FH 6-32X 3\8	
6	.74	127-105-027	MS24693-27	A	SCR 100 FH 6-32X7\16	
1	.77	127-105-272	MS24693-272	A	SCR 100 FH 10-32X1\2	
12	182	128-200-802	MS15795-802	A	WASHER FLAT RD NO 2	
2	183	128-200-803	MS15795-803	A	WASHER FLAT RD NO.4	
4	184	128-200-805	MS15795-805	A	WASHER FLAT RD NO.6	
1	185	128-200-808	MS15795-808	A	WASHER FLAT RD NO.10	
4	189	128-202-134	MS35338-134	A	WASHER LK SPLIT NO.2	
10	190	128-202-135	MS35338-135	A	WASHER LK SPLIT NO.4	
10	191	128-202-136	MS35338-136	A	WASHER LK SPLIT NO.6	
1	192	128-202-138	MS35338-138	A	WASHER LK SPLIT NO.10	
12	197	129-001-002	92-1660-26	D	NUT HEX LK MINTR 2-56	
7	198	129-001-003	92-1660-40	C	NUT HEX LK MINTR 4-40	
5	199	129-004-001	22NM107-62	A	NUT SLFLK RED HD 6-32	
56	201	129-005-014	MS-20365-14	A	NUT SELF LOCK 4-40	
20	202	129-005-015	MS-20365-15		NUT SELF-LOCKING 6-32	

PL355-0002-501 H
SHT. 6

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J.MATHER
C	REVISED PER ECO 05587 BAKER 10-10-80		10-16-80	J.MATHER
D	REVISED PER ECO 06192 JSG		3-26-81	ATF
E	REVISED PER ECO 08206 J.F.S. 2-10-83		22 Feb 83	RS Vol 2
F	REVISED PER ECO 08630 R.P.K. 11-21-83		11-29-83	R. MARGRAFF
G	REVISED PER ECO 08861 KEN MAC 12-22-83		1-3-84	J. B. Bogrim

WIRE LIST: A) 730-2009
WIRE LIST: LIBRARY, A) 760-0286
R. PANEL HARNESS: D) 790-0415
F. PANEL HARNESS; D) 790-0454

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION																							

AYDIN MONITOR SYSTEMS
PORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER CHASSIS ASSEMBLY MODEL 335

CODE IDENT 20747
CONTRACT NO. 4911-11

DRAWN	L.GRUCELLA		ENGINEER	D.R.McKINNEY	4-18-80	DWG NO.	REV
CHECKED	D.D.MOUAT	4-29-80	APPROVED	D.D.MOUAT	4-29-80	PL355-0002-502	G
DRAFTING	E.S.	5-5-80	MFG. 58-80 WASHICK	R.MARGRAFF	5-9-80	SHEET 1 OF 6	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
FILE A1	■	■	■	■	■	■	■	■	■	■	■					
KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
FILE A2		■	■	■	■											
KEY		8/12	8/12	18/22	8/12											
FILE A3	■	■	■	■	■											
KEY	8/12	8/12	8/12	8/12	8/12											
FILE A4	■	■	■	■	■	■	■	■	■		■					
KEY	18/22	8/12	12/38	12/38	8/21	8/12	8/12	8/12	4/26		10/36					

INDICATES P.C. CONN AND KEY INSTALLED

POSITION NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
FILE A1																
KEY																
FILE A2																
KEY																
FILE A3																
KEY																
FILE A4																
KEY																

INDICATES P.C. CONN AND KEY INSTALLED

DRAWN BY	CHECKED	TITLE	CODE IDENT NO.	DWG. NO.	REV
L. GRUCELLA		PCM BIT SYNCHRONIZER CHASSIS ASSEMBLY - MODEL 335	20747	PL355-0002-502	G
DATE 4-11-80	DATE			SHEET 2 OF	

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
		355-0002-502		G	PARENT MODEL 335 CH ASSIS	
15		113-006-002	MIL-W-16878D/1	C	WIRE INSUL STR 22 BLK	
15		113-006-004	MIL-W-16878D/1	C	WIRE INSUL STR 22 GRN	
100		113-008-001	1853-1	B	WIRE INSUL STR 26 WHT	
90		113-217-002	1TWP267U	F	WIRE TW PR 26 BLK/GRN	
35		113-004-002	1857/19-2	A	WIRE INSUL STR 18 BLK	
10		113-004-003	MIL-W-16878 D/1	A	WIRE INSUL STR 18 RED	
20		113-004-005	MIL-W-16878 D/1	A	WIRE INSUL STR 18 YEL	
10		113-004-010	MIL-W-16878 D/1	A	WIRE INSUL STR 18 VIO	
20		113-008-002	MIL-W-16878D/1	B	WIRE INSUL STR 26 BLK	
4		113-219-222	3221	B	CABLE SHLD 2 COND 22	
15		113-006-003	MIL-W-16878D/1	C	WIRE INSUL STR 22 RED	
15		113-006-010	MIL-W-16878D/1	C	WIRE INSUL STR 22 VIO	
3		113-205-006	SEE SPEC	E	CAB UNSHLD 6 COND 26	
15		113-004-001	MIL-W-16878 D/1	A	WIRE INSUL STR 18 WHT	
20		113-008-005	MIL-W-16878D/1	B	WIRE INSUL STR 26 YEL	
6		113-205-012	MIL-W-16878	E	CAB UNDHLD 12 COND 26	
8		113-205-025	MIL-W-16878	E	CAB UNSHLD 25 COND 26	
10		113-004-004	MIL-W-16878 D/1	A	WIRE INSUL STR 18 GRN	
12		113-219-218	3241	B	CABLE SHLD 2 COND 18	
35		113-305-001	8417	D	CABLE SHLD 1 COND 25	
10		113-307-006	TWC-124-2	G	CABLE TWINAX 20 AWG	
1	017	201-0525-002	201-0525-002	C	PANEL FRONT MODEL 335	
1	021	203-0600-001			PANEL REAR	
1	025	205-0595-001			BRACKET	
1	026	205-0595-002			BRACKET	
1	027	205-0596-001			BRACKET	
2	029	206-0258-001			COVER	
1	030	206-0260-001		B	COVER	
1	033	207-0601-001			PLATE	
1	034	207-0601-002			PLATE	
1	036	208-0297-001			SUPPORT	
1	037	207-0704-003	207-0704-003		PLATE	
1	038	210-0293-001			SIDE FRAME	
1	039	210-0293-002			SIDE FRAME	
1	041	211-0234-001			ANGLE	
1	042	211-0234-002			ANGLE	
1	043	211-0235-001			ANGLE	
1	044	211-0235-002			ANGLE	
8	046	217-0345-001		0	MOD CONN	
1	048	225-0198-001			BAR	
1	049	225-0199-001			BAR	
1	050	225-0199-002			BAR	
1	052	351-0273-501	351-0273-501	C	INSUL GRND	E7
2	063	107-025-001	1030-F-101-2N	AG	SW RTY 30 DEG 2 POS	S1 S6
2	064	107-025-019	1030F-102-4N	AG	SW RTY 30 DEG 4 POS	S5 S13
1	065	107-025-020	1030F-104-9N	AG	SW RTY 30 DEG 9 POS	S4
1	066	107-026-014	1036F-101-6N	L	SW RTY 36 DEG 6 POS	S3
2	067	107-107-003	MSS-44	A	SW SLIDE SUBMIN DPDT	S31 S32
3	068	107-112-001	MBS-C-ALO	H	SW BUT MINI TAP PIN C	S2 S14

PL355-0002-502G
SHT. 3

*** SINGLE LEVEL BILL - BY ITEM ***
SUB. MTG. ITEM 13:49:35 21 DEC 1983 PAGE 4

QTA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
1	069	107-232-003	MTG-106D	B	SW TGL SPDT	S15
1	070	107-328-001	8-M-352	G	THUMBWH SW ASSY 4 POS	S16
						S7
						S8
						S9
						S10
						S11
2	071	108-306-001	BJ-72	B	CONN BULKHD JACK	S12
						J15
2	072	108-101-010	1-202663-8	Z	CONNECTOR 34 POS MALE	J19
						J17
68	073	108-101-108	66106-1	Z	CONN PIN CONT 26-24	J18
1025	074	108-107-046	000-60-8017-03-	J	CONN CONTACT (LOOSE)	
29	075	108-207-005	7015-041-000-00	C	CONN RECEP 41 POS	
58	076	108-207-009	60-5006-3414	C	CONN POLARIZ INSERT	
14	077	108-302-001	BJ-27	L	CONN STD RECEPT	J1
						J2
						J3
						J4
						J5
						J6
						[illegible]
						[illegible]
						J9
						J10
						J11
						J12
						J13
						J14
1	078	108-817-001	5004-6622	F	CONN PWR LINE FILTER	J16
1	080	110-008-006	507-39111432600	C	LAMP INCAND GRN	DS3
7	081	110-008-011	515-0012	C	LAMP CONN CARTRIDGE	
7	082	110-008-013	515-0051	C	LAMP SPEED CLIP	
9	083	110-019-001	507-47573731500	H	LAMP CART RED	XDS1
						XDS2
						XDS14
						XDS15
						XDS16
						XDS17
						XDS18
						XDS19
						XDS20
3	084	110-019-009	250-873814504	H	LMPHOLDER W/O COLLAR	XDS1
						XDS2
						XDS3
1	085	110-027-001	507-45380931610	C	LAMP CART RED	DS21
1	086	110-027-005	508-8745-504	C	LAMPHOLD W/COLLAR	XDS21
1	088	111-005-025	31302.5	B	FUSE 2-1/2 A SLO-BLO	F1
4	089	111-200-001	111-200-001	D	LABEL WARNING 115V	
1	091	112-012-001	260-781	D	METER THIN LINE-HORIZ	
1	092	112-015-001	260-780	L	METER THIN LINE-HORIZ	M1
1	093	112-021-001	749-1506-803	P	DISPLAY LED 6 CHAR	XDS4
						XDS5
						XDS6

PL355-0002-502G
SHT. 4

QTY	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
						XDS7
						XDS8
						XDS9
1	094	112-021-002	749- -801	P	DISPLAY LED 3 CHAR	XDS11
						XSD12
						XSD13
1	095	112-024-001	550-50-115VAC-1	A	INDICATOR ELP TIME	M3
10	097	113-406-002	60 80./ 0723	A	BUS STRIP VARILOK	
0	099	114-031-001	7361-1	A	TAPE FILM PRESS SENS	
1	101	116-005-001	4600X	N	FAN 115 VAC	
2	102	116-005-004	08122	N	FAN FINGER GUARD	
5	104	118-015-004	1511-1-0519	A	TERM TUR INSUL SOLD	E1
						E2
						E3
						E4
						E6
1	105	118-202-212	3283[illegible]	N	TERM CRIMP 22-16 #10	
1	107	119-004-008	410-8	A	TERMINAL BLOCK 8 POS	TB1
3	108	119-004-023	410-J	A	TERMINAL BLOCK JUMPER	
1	110	120-004-059	222	C	SEALANT THREAD	
2	112	121-004-003	F7500-10-D-3	J	CAPTIVE SCREW 10-32	
8	113	121-005-001	82-11-140-16	H	FASTENER 1/4 TURN	
8	114	121-005-009	82-45-101-15	H	RECEPTACLE 1/4 TURN	
8	115	121-005-010	82-32-101-20	H	RETAINING WASHER	
6	116	121-115-001	SS-70PL-2	B	KNOB RD POINTED 1/4 S	
6	117	121-200-001	105-0253-001	D	TEST POINT STD BLK	TP1
						TP2
						TP3
						TP4
						TP5
						TP6
1	118	121-303-001	HKP	C	FUSE HOLDER NON IND	XF1
2	119	121-503-001	10923-B-1032-A	K	HANDLE OVAL 3" CTR	
2	121	124-002-008	MS410-8-XP 1A	A	MARKER STRIP 8 POS	
1	122	124-011-002	SEE SPEC	C	LOGO PLATE	
2	124	128-003-010	8104-SS-0440	C	STDF HX .19 4-40X3/8	
5	125	128-008-011	9224A140	C	SPACER RD .25D 6 1/4	
4	127	130-203-001	SST1.5	E	CABLE TIE 1-1/4 DIA	
7	128	130-204-001	TA1S8-*	E	MOUNT CABLE TIE	
18	130	135-004-001	56 590 65/3B	A	FERRITE BEAD	
1	131	136-079-003	ET602-1	G	PWR SPLY 5V-12A/15V-3	PS1
4	146	127-109-004	MS5195[illegible] -04	A	SCR PAN HD 2-56X5\16	
8	147	127-109-006	MS51957-06	A	SCR PAN HD 2-56X7\16	
8	150	127-109-012	MS5195[illegible] 12	A	SCR PAN HD 4-40X3\16	
8	151	127-109-013	MS51957-13	A	SCR PAN HD 4-40X1\4	
2	152	127-109-014	MS51957-14	A	SCR PAN HD 4-40X5\16	
5	153	127-109-015	MS51957-15	A	SCR PAN HD 4-40X3/8	
2	154	127-109-017	MS51957-17	A	SCR PAN HD 4-40X1\2	
38	155	127-109-019	MS51957-19	A	SCR PAN HD 4-40X3\4	
1	156	127-109-016	MS51957-16	A	SCR PAN HD 4-40X7\16	
2	157	127-109-027	MS51957-27	A	SCR PAN HD 6-32X5\16	
24	158	127-109-028	MS51957-28	A	SCR PAN HD 6-32X3\8	
2	159	127-109-029	MS51957-29	A	SCR PAN HD 6-32X7\16	
4	160	127-109-030	MS51957-30	A	SCR PAN HD 6-32X1\2	
4	161	127-109-123	MS51957-123	A	SCR PAN HD 6-32X9\16	

PL355-0002-5024
SHT. 5

Q'TY	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
8	163	127-109-043	MS51957-43	A	SCR PAN HD 8-32X3\8	
1	165	127-101-062	MS51958-62	A	SCR PAN HD 10-32X7\16	
2	168	127-105-003	MS2469[illegible]-03	A	SCR 100 FH 4-40X 5\16	
16	167	127-105-004	MS2469 -04	A	SCR 100 FH 4-40 X 3/8	
4	172	127-105-025	MS2469 -25	A	SCR 100 FH 6-32X 5\16	
2	173	127-105-026	MS2469 -26	A	SCR 100 FH 6-32X 3\8	
6	174	127-105-027	MS2469 -27	A	SCR 100 FH 6-32X7\16	
4	177	127-105-272	MS2469[illegible]-272	A	SCR 100 FH 10-32X1\2	
12	182	128-200-802	MS15795-802	A	WASHER FLAT RD NO 2	
2	183	128-200-803	MS15795-803	A	WASHER FLAT RD NO.4	
4	184	128-200-805	MS15795-805	A	WASHER FLAT RD NO.6	
1	185	128-200-808	MS15795-808	A	WASHER FLAT RD NO.10	
4	189	128-202-134	MS35338-134	A	WASHER LK SPLIT NO.2	
10	190	128-202-135	MS35338-135	A	WASHER LK SPLIT NO.4	
12	191	128-202-136	MS35338-136	A	WASHER LK SPLIT NO.6	
1	192	128-202-138	MS35338-138	A	WASHER LK SPLIT NO.10	
12	197	129-001-002	92-1660-26	C	NUT HEX LK MINTR 2-56	
7	198	129-001-003	92-1660-40	C	NUT HEX LK MINTR 4-40	
5	199	129-004-001	22NM107-62	A	NUT SLFLK RED HD 6-32	
60	201	129-005-014	MS-20365-14	A	NUT SELF LOCK 4-40	
20	202	129-005-015	MS-20365-15		NUT SELF-LOCKING 6-32	

REVISIONS

REV	DESCRIPTION	EFFECTIVITY	DATE	APPROVED
B	REVISED PER ECO 05389		9-2-80	J.MATHER
C	REVISED PER ECO 05587 BAKER 10-10-80		10-16-80	J.MATHER
D	REVISED PER ECO 06192 JSG		3-26-81	ATF
E	REVISED PER ECO 08206 J.F.S. 2-10-83		22Feb83	RSVitz
F	REVISED PER ECO 08630 R.P.K. 11-21-83		11-21-83	R. MARGRAFF
G	REVISED PER ECO 08861 K. MACNEIL 4/27/84		1-3-84	

WIRE LIST; A) 730-1746
WIRE LIST, LIBRARY: A) 760-0225
R. PANEL HARNESS: D) 790-0415
F. PANEL HARNESS: D) 790-0454

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	G	G	G	G	G	G																	

AYDIN MONITOR SYSTEMS
PORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER CHASSIS ASSEMBLY MODEL 335

CODE IDENT 20747
CONTRACT NO. 4911-11

DRAWN	L.GRUCELLA		ENGINEER	D.R.McKINNEY	4-18-80	DWG NO. PL355-0002-503	REV G
CHECKED	D.D.MOUAT	4-29-80	APPROVED	D.D.MOUAT	4-29-80		
DRAFTING	E.S.	5-5-80	MFG. 5-8-80 WASHICK	R.MARGRAFF	5-9-80	SHEET 1 OF 6	

800-0066

800-0197A AYDIN MONITOR SYSTEMS

POSITION NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
FILE A1	■	■	■	■	■	■	■	■	■	■	■	■				
KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34	8/16				
FILE A2		■	■	■	■											
KEY		8/12	8/12	18/22	8/12											
FILE A3	■	■	■	■	■											
KEY	8/12	8/12	8/12	8/12	8/12											
FILE A4	■						■	■	■		■					
KEY	18/22						8/12	8/12	4/26		10/36					

INDICATES P.C. CONN AND KEY INSTALLES

POSITION NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
FILE A1																
KEY																
FILE A2																
KEY																
FILE A3																
KEY																
FILE A4																
KEY																

DRAWN BY	CHECKED	TITLE PCM BIT SYNCHRONIZER CHASSIS ASSEMBLY MODEL 335	CODE IDENT NO. 20747	DWG. NO. 355-0002-503	REV G
DATE	DATE			SHEET 2 OF	

		355-0002-503		G	PARENT 335 CHS
15		113-006-002	MIL-W-16878D/1	C	WIRE INSUL STR 22 BLK
15		113-006-004	MIL-W-16878D/1	C	WIRE INSUL STR 22 GRN
100		113-008-001	1853-1	B	WIRE INSUL STR 26 WHT
90		113-217-002	1TWP267U	F	WIRE TW PR 26 BLK/GRN
35		113-004-002	1857/19-2	A	WIRE INSUL STR 18 BLK
10		113-004-003	MIL-W-16878 D/1	A	WIRE INSUL STR 18 RED
20		113-004-005	MIL-W-16878 D/1	A	WIRE INSUL STR 18 YEL
10		113-004-010	MIL-W-16878 D/1	A	WIRE INSUL STR 18 VIO
20		113-008-002	MIL-W-16878D/1	B	WIRE INSUL STR 26 BLK
4		113-219-222	3221	B	CABLE SHLD 2 COND 22
15		113-006-003	MIL-W-16878D/1	C	WIRE INSUL STR 22 RED
15		113-006-010	MIL-W-16878D/1	C	WIRE INSUL STR 22 VIO
3		113-205-006	SEE SPEC	E	CAB UNSHLD 6 COND 26
15		113-004-001	MIL-W-16878 D/1	A	WIRE INSUL STR 18 WHT
20		113-008-005	MIL-W-16878D/1	B	WIRE INSUL STR 26 YEL
6		113-205-012	MIL-W-16878	E	CAB UNDHLD 12 COND 26
8		113-205-025	MIL-W-16878	E	CAB UNSHLD 25 COND 26
10		113-004-004	MIL-W-16878 D/1	A	WIRE INSUL STR 18 GRN
12		113-219-218	3241	B	CABLE SHLD 2 COND 18
35		113-305-001	8417	D	CABLE SHLD 1 COND 25
1	017	201-0525-003	201-0525-003	C	PANEL FRONT MODEL 335
1	021	203-0600-001			PANEL REAR
1	025	205-0595-001			BRACKET
1	026	205-0595-002			BRACKET
1	027	205-0596-001			BRACKET
2	029	206-0258-001			COVER
1	030	206-0260-001		B	COVER
1	033	207-0601-001			PLATE
1	034	207-0601-002			PLATE
1	035	207-0632-001			PLATE, COVER, SLIDE S W.
1	036	208-0297-001			SUPPORT
1	037	207-0704-004	207-0704-004		PLATE CONN MTG
1	038	210-0293-001			SIDE FRAME
1	039	210-0293-002			SIDE FRAME
1	041	211-0234-001			ANGLE
1	042	211-0234-002			ANGLE
1	043	211-0235-001			ANGLE
1	044	211-0235-002			ANGLE

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
9	046	217-0345-001		0	MOD CONN	
1	048	225-0198-001			BAR	
1	049	225-0199-001			BAR	
1	050	225-0199-002			BAR	
1	052	351-0273-501	351-0273-501	C	INSUL GRND	E7
1	059	107-025-019	1030F-102-4N	AG	SW RTY 30 DEG 4 POS	S13
1	060	107-025-001	1030-F-101-2N	AG	SW RTY 30 DEG 2 POS	S1
1	061	107-029-007	1630F-102-3N-60	J	SW RTY 30/60 DEG CONC	S6
1	062	107-029-005	1630F/1246	J	SW RTY 30/30 DEG CONC	S5
1	065	107-035-020	1030F-104-9N	AG	SW RTY 30 DEG 9 POS	S4
1	066	107-036-014	1036F-101-6N	L	SW RTY 36 DEG 6 POS	S3
1	067	107-107-003	MSS-44	A	SW SLIDE SUBMIN DPDT	S32
3	068	107-112-001	MBS-C-ALO	H	SW BUT MINI TAP PIN C	S2
						S14
1	069	107-232-003	MTG-106D	B	SW TGL SPDT	S15
1	070	107-328-001	8-M-352	G	THUMBWH SW ASSY 4 POS	S16
						S7
						S8
2	072	108-101-010	1-202663-8	Z	CONNECTOR 34 POS MALE	S9
						J17
68	073	108-101-108	66106-1	Z	CONN PIN CONT 26-24	J18
1025	074	108-107-046	000-60-8017-03-	J	CONN CONTACT (LOOSE)	
26	075	108-207-005	7015-041-000-00	C	CONN RECEP 41 POS	
52	076	108-207-009	60-5006-3414	C	CONN POLARIZ INSERT	
15	077	108-302-001	BJ-27	L	CONN STD RECEPT	J1
						J2
						J3
						J4
						J5
						J6
						J7
						J8
						J9
						J10
						J11
						J12
						J13
						J14
1	078	108-817-001	5004-6622	F	CONN PWR LINE FILTER	J15
1	080	110-008-006	507-39111432600	C	LAMP INCAND GRN	J16
9	081	110-008-011	515-0012	C	LAMP CONN CARTRIDGE	DS3
9	082	110-008-013	515-0051	C	LAMP SPEED CLIP	
11	083	110-019-001	507-47573731500	H	LAMP CART RED	XDS1
						XDS2
						XDS10
						XDS14
						XDS15
						XDS16
						XDS17
						XDS1
						XDS1
						XDS20
						XDS23

PL355-0002-503G

SHT. 4

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
3	084	110-019-009	250-873814504	H	LMPHOLDER W/O COLLAR	XDS1 XDS2 XDS3
1	085	110-027-001	507-45380931610	C	LAMP CART RED	DS21
1	086	110-027-005	508-8745-504	C	LAMPHOLD W/COLLAR	XDS21
1	088	111-005-025	31302.5	B	FUSE 2-1/2 A SLO-BLO	F1
4	089	111-200-001	111-200-001	D	LABEL WARNING 115V	
1	091	112-012-001	260-781	D	METER THIN LINE-HORIZ	M1
1	092	112-015-001	260-780	L	METER THIN LINE-HORIZ	M2
1	093	112-021-001	749-1506-803	P	DISPLAY LED 6 CHAR	XDS4 XDS5 XDS6 XDS7 XDS8 XDS9
1	095	112-024-001	550-SS-115VAC-1	A	INDICATOR ELP TIME	M3
1	096	112-021-006	749-1504-801	P	DISPLAY LED 4 CHAR	XDS11 XDS12 XDS13 XDS22
7	097	113-406-002	60 8017 0723	A	BUS STRIP VARILOK	
0	099	114-031-001	7361-1	A	TAPE FILM PRESS SENS	
1	101	116-005-001	4600X	N	FAN 115 VAC	
2	102	116-005-004	08122	N	FAN FINGER GUARD	
5	104	118-015-004	1511-1-0519	A	TERM TUR INSUL SOLD	E1 E2 E3 E4 E6
1	105	118-202-212	32836	N	TERM CRIMP 22-16 #10	
1	107	119-004-008	410-8	A	TERMINAL BLOCK 8 POS	TB1
3	108	119-004-023	410-J	A	TERMINAL BLOCK JUMPER	
1	110	120-004-059	222	C	SEALANT THREAD	
2	111	121-113-001	70CPL-2	A	KNOB RD POINTED 1/4 S	
2	112	121-004-003	F7500-10-D-3	J	CAPTIVE SCREW 10-32	
8	113	121-005-001	82-11-140-16	H	FASTENER 1/4 TURN	
8	114	121-005-009	82-45-101-15	H	RECEPTACLE 1/4 TURN	
8	115	121-005-010	82-32-101-20	H	RETAINING WASHER	
4	116	121-115-001	SS-70PL-2	B	KNOB RD POINTED 1/4 S	
6	117	121-200-001	105-0253-001	D	TEST POINT STD BLK	TP1 TP2 TP3 TP4 TP5 TP6
1	118	121-303-001	HKP	C	FUSE HOLDER NON IND	XF1
2	119	121-503-001	10923-B-1032-A	K	HANDLE OVAL 3" CTR	
2	120	121-112-001	R50-1WD-1G	A	KNOB ROUND 1/8 SHAFT	
2	121	124-002-008	MS410-8-XP 1A	A	MARKER STRIP 8 POS	
1	122	124-011-002	SEE SPEC	C	LOGO PLATE	
1	123	121-409-032	SS-4815Z-K2915	F	PLUG BUTTON	
2	124	128-003-010	8104-SS-0440	C	STDF HX .19 4-40X3/8	
5	125	128-008-011	9224A140	C	SPACER RD .25D 6 1/4	
4	127	130-203-001	SST1.5	E	CABLE TIE 1-1/4 DIA	
7	128	130-204-001	TA1S8-*	E	MOUNT CABLE TIE	

PL355-0002-5036 SHT. 5

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
18	130	135-004-001	56 590 65/3B	A	FERRITE BEAD	
1	131	136-079-003	ET602-1	G	PWR SPLY 5V-12A/15V-3	PS1
4	146	127-109-004	MS51957-04	A	SCR PAN HD 2-56X5\16	
8	147	127-109-006	MS51957-06	A	SCR PAN HD 2-56X7\16	
8	150	127-109-012	MS51957-12	A	SCR PAN HD 4-40X3\16	
8	151	127-109-013	MS51957-13	A	SCR PAN HD 4-40X1\4	
2	152	127-109-014	MS51957-14	A	SCR PAN HD 4-40X5\16	
5	153	127-109-015	MS51957-15	A	SCR PAN HD 4-40X3/8	
2	154	127-109-017	MS51957-17	A	SCR PAN HD 4-40X1\2	
34	155	127-109-019	MS51957-19	A	SCR PAN HD 4-40X3\4	
1	156	127-109-016	MS51957-16	A	SCR PAN HD 4-40X7\16	
2	157	127-109-027	MS51957-27	A	SCR PAN HD 6-32X5\16	
24	158	127-109-028	MS51957-28	A	SCR PAN HD 6-32X3\8	
2	159	127-109-029	MS51957-29	A	SCR PAN HD 6-32X7\16	
4	160	127-109-030	MS51957-30	A	SCR PAN HD 6-32X1\2	
4	161	127-109-123	MS51957-123	A	SCR PAN HD 6-32X9\16	
8	163	127-109-043	MS51957-43	A	SCR PAN HD 8-32X3\8	
1	165	127-101-062	MS51958-62	A	SCR PAN HD 10-32X7\16	
2	168	127-105-003	MS24693-03	A	SCR 100 FH 4-40X 5\16	
16	169	127-105-004	MS24693-04	A	SCR 100 FH 4-40 X 3/8	
4	172	127-105-025	MS24693-25	A	SCR 100 FH 6-32X 5\16	
2	173	127-105-026	MS24693-26	A	SCR 100 FH 6-32X 3\8	
6	174	127-105-027	MS24693-27	A	SCR 100 FH 6-32X7\16	
4	177	127-105-272	MS24693-272	A	SCR 100 FH 10-32X1\2	
10	182	128-200-802	MS15795-802	A	WASHER FLAT RD NO 2	
2	183	128-200-803	MS15795-803	A	WASHER FLAT RD NO.4	
4	184	128-200-805	MS15795-805	A	WASHER FLAT RD NO.6	
1	185	128-200-808	MS15795-808	A	WASHER FLAT RD NO.10	
2	189	128-202-134	MS35338-134	A	WASHER LK SPLIT NO.2	
10	190	128-202-135	MS35338-135	A	WASHER LK SPLIT NO.4	
12	191	128-202-136	MS35338-136	A	WASHER LK SPLIT NO.6	
1	192	128-202-138	MS35338-138	A	WASHER LK SPLIT NO.10	
12	197	129-001-002	92-1660-26	C	NUT HEX LK MINTR 2-56	
7	198	129-001-003	92-1660-40	C	NUT HEX LK MINTR 4-40	
5	199	129-004-001	22NM107-62	A	NUT SLFLK RED HD 6-32	
46	201	129-005-014	MS-20365-14	A	NUT SELF LOCK 4-40	
16	202	129-005-015	MS-20365-15		NUT SELF-LOCKING 6-32	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 08861 K. MAC NEEL 12-27-93		1-3-94	

NIKE LIST · A) 730-2231
NIKE LIST LIBRARY: B) 760-0310
REAR PANEL HARNESS: D) 790-0415
[illegible] HARNESS: D) 790-0454

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION																							

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PCM BIT SYNCHRONIZER
CHASSIS ASSY
MODEL 335

CODE IDENT 20747
CONTRACT NO. 1230-51

DRAWN	C. FAZIO	7/29/93	ENGINEER	RSV012	24AUG93	DWG NO. PL355-0002-504	REV B
CHECKED	ES		APPROVED	RSV012	24AUG93		
DRAFTING	[signature]	8-24-93				SHEET 1 OF 6	

800-0066

800-0197-2 AYDIN MONITOR SYSTEMS

POSITION NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
FILE A1																
KEY	10/16	8/22	12/22	8/22	10/36	8/16	12/32	12/30	12/34	8/22	12/34					
FILE A2																
KEY		8/12	8/12	18/22	8/12											
FILE A3																
KEY	8/12	8/12	8/12	8/12	8/12											
FILE A4																
KEY	18/22	8/12	12/38	12/38	8/12		8/12	8/12	4/26		10/36					

INDICATES P.C. CONN. INSTALLED

POSITION NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
FILE A1																
KEY																
FILE A2																
KEY																
FILE A3																
KEY																
FILE A4																
KEY																

INDICATES P.C. CONN. INSTALLED

DRAWN BY C. FAZIO DATE 7-29-83	CHECKED DATE	TITLE PCM BIT SYNCHRONIZER CHASSIS ASSEMBLY, MODEL 335	CODE IDENT NO. 20747	DWG. NO. PL355-0002-504 SHEET 2 OF	REV B

QTY	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	CODE
		355 0002 504		B	PARENT MODEL 355-0 ASSIS-905	
15		113-006-001	MIL-W-16878D/1	C	WIRE INSUL STR 22 BLK	
15		113-006-004	MIL-W-16878D/1	C	WIRE INSUL STR 22 GRN	
100		113-008-001	1003/1	B	WIRE INSUL STR 26 WHT	
70		113-217-002	TFWP26/7U		WIRE TW PR 26 BLK/GRN	
55		113-004-002	1857/19-2	A	WIRE INSUL STR 18 BLK	
10		113-004-003	MIL-W-16878 D/1	A	WIRE INSUL STR 18 RED	
10		113-004-005	MIL-W-16878 D/1	A	WIRE INSUL STR 18 YEL	
0		113-004-010	MIL-W-16878 D/1	A	WIRE INSUL STR 18 VIO	
20		113-008-002	MIL-W-16878D/1	B	WIRE INSUL STR 26 BLK	
4		113-219-222	3221	B	CABLE SHLD 2 COND 22	
15		113-006-003	MIL-W-16878D/1	C	WIRE INSUL STR 22 RED	
15		113-006-010	MIL-W-16878D/1	C	WIRE INSUL STR 22 VIO	
3		113-205-006	SEE SPEC	E	CAB UNSHLD 6 COND 26	
15		113-004-001	MIL-W-16878 D/1	A	WIRE INSUL STR 18 WHT	
20		113-008-005	MIL-W-16878D/1	B	WIRE INSUL STR 26 YEL	
6		113-205-012	MIL-W-16878	E	CAB UNDHLD 12 COND 26	
8		113-205-025	MIL-W-16878	E	CAB UNSHLD 25 COND 26	
10		113-004-004	MIL-W-16878 D/1	A	WIRE INSUL STR 18 GRN	
12		113-219-218	3241	B	CABLE SHLD 2 COND 18	
35		113-305-001	8417	D	CABLE SHLD 1 COND 25	
1	017	201-0525-002	201-0525-002	C	PANEL FRONT MODEL 335	
1	021	203-0600-001			PANEL REAR	
1	025	205-0595-001			BRACKET	
1	026	205-0595-002			BRACKET	
1	027	205-0596-001			BRACKET	
2	029	206-0258-001			COVER	
1	030	206-0260-001		B	COVER	
1	033	207-0601-001			PLATE	
1	034	207-0601-002			PLATE	
1	036	208-0297-001			SUPPORT	
1	037	207-0704-006	207-0704-006		PLATE CONN MTG	
1	038	210-0293-001			SIDE FRAME	
1	039	210-0293-002			SIDE FRAME	
1	041	211-0234-001			ANGLE	
1	042	211-0234-002			ANGLE	
1	043	211-0235-001			ANGLE	
1	044	211-0235-002			ANGLE	
8	046	217-0345-001		Ø	MOD CONN	
1	048	225-0198-001			BAR	
1	049	225-0199-001			BAR	
1	050	225-0199-002			BAR	
1	052	351-0273-501	351-0273-501	C	INSUL GRND	E7
2	063	107-025-001	1030-F-101-2N	AG	SW RTY 30 DEG 2 POS	S1 S6
2	064	107-025-019	1030F-102-4N	AG	SW RTY 30 DEG 4 POS	S5 S13
1	065	107-025-020	1030F-104-9N	AG	SW RTY 30 DEG 9 POS	S4
1	066	107-026-014	1036F-101-6N	L	SW RTY 36 DEG 6 POS	S3
2	067	107-107-003	MSS-44	A	SW SLIDE SUBMIN DPDT	S31 S32
3	068	107-112-001	MBS-C-ALO	H	SW BUT MINI TAP PIN C	S2 S14 S15

PL355-0002-504B
SHT. 3

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DE
1	069	107-232-003	MTG-106D	B	SW TGL SPDT	S16
1	070	107-328-001	8-M-352	G	THUMBWH SW ASSY 4 POS	S7
						S8
						S9
						S10
						S11
						S12
1	072	108-101-010	1-202663-8	Z	CONNECTOR 34 POS MALE	J17
34	073	108-101-108	66106-1	Z	CONN PIN CONT 26-24	
1025	074	108-107-046	000-60-8017-03-	J	CONN CONTACT (LOOSE)	
31	075	108-207-005	7015-041-000-00	C	CONN RECEP 41 POS	A1
						A2
						A3
						A4
62	076	108-207-009	60-5006-3414	C	CONN POLARIZ INSERT	
15	077	108-302-001	BJ-27	L	CONN STD RECEPT	J1
						J2
						J3
						J4
						J5
						J6
						J7
						J8
						J
						J11
						J12
						J13
						J14
1	078	108-817-001	5004-6622	F	CONN PWR LINE FILTER	J15
3	079	108-306-001	BJ-72	B	CONN BULKHD JACK	J16
						J18
						J19
						J20
1	080	110-008-006	507-39111432600	C	LAMP INCAND GRN	DS3
7	081	110-008-011	515-0012	C	LAMP CONN CARTRIDGE	
7	082	110-008-013	515-0051	C	LAMP SPEED CLIP	
9	083	110-019-001	507-47573731500	H	LAMP CART RED	XDS1
						XDS2
						XDS14
						XDS15
						XDS16
						XDS17
						XDS18
						XDS19
						XDS20
3	084	110-019-009	250-873814504	H	LMPHOLDER W/O COLLAR	XDS1
						XDS2
						XDS3
1	085	110-027-001	507-45380931610	C	LAMP CART RED	DS21
1	086	110-027-005	508-8745-504	C	LAMPHOLD W/COLLAR	XI 1
1	087	107-037-016	50YY23165-01-2-	G	SW RTY SCRDRIV 4 POS	
1	088	111-005-025	31302.5	B	FUSE 2-1/2 A SLO-BLO	
4	089	111-200-001	111-200-001	D	LABEL WARNING 115V	
1	090	107-037-015	50J1066	G	SW RTY NON-TURN WASH	

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
1	091	112-012-001	260-781	D	METER THIN LINE-HORIZ	M1
1	092	112-015-001	260-780	L	METER THIN LINE-HORIZ	M2
1	093	112-021-001	749-1506-803	P	DISPLAY LED 6 CHAR	XDS4 XDS5 XDS6 XDS7 XDS8 XDS9
1	094	112-021-002	749-1503-801	P	DISPLAY LED 3 CHAR	XDS11 XDS12 XDS13
1	095	112-024-001	550-SS-115VAC-1	A	INDICATOR ELP TIME	M3
7	097	113-406-002	60 8017 0723	A	BUS STRIP VARILOK	
0	099	114-031-001	7361-1	A	TAPE FILM PRESS SENS	
1	101	116-005-001	4600X	N	FAN 115 VAC	
2	102	116-005-004	08122	N	FAN FINGER GUARD	
5	104	118-015-004	1511-1-0519	A	TERM TUR INSUL SOLD	E1 E2 E3 E4 E6
1	105	118-202-212	32836	N	TERM CRIMP 22-16 #10	
1	107	119-004-008	410-8	A	TERMINAL BLOCK 8 POS	TB1
3	108	119-004-023	410-J	A	TERMINAL BLOCK JUMPER	
1	110	120-004-059	222	C	SEALANT THREAD	
2	112	121-004-003	F7500-10-D-3	J	CAPTIVE SCREW 10-32	
8	113	121-005-001	82-11-140-16	H	FASTENER 1/4 TURN	
8	114	121-005-009	82-45-101-15	H	RECEPTACLE 1/4 TURN	
8	115	121-005-010	82-32-101-20	H	RETAINING WASHER	
6	116	121-115-001	SS-70PL-2	B	KNOB RD POINTED 1/4 S	
6	117	121-200-001	105-0253-001	D	TEST POINT STD BLK	TP1 TP2 TP3 TP4 TP5 TP6
1	118	121-303-001	HKP	C	FUSE HOLDER NON IND	XF1
2	119	121-503-001	10923-B-1032-A	K	HANDLE OVAL 3" CTR	
2	121	124-002-008	MS410-8-XP 1A	A	MARKER STRIP 8 POS	
1	122	124-011-002	SEE SPEC	C	LOGO PLATE	
2	124	128-003-010	8104-SS-0440	C	STDF HX .19 4-40X3/8	
5	125	128-008-011	9224A140	C	SPACER RD .25D 6 1/4	
4	127	130-203-001	SST1.5	E	CABLE TIE 1-1/4 DIA	
7	128	130-204-001	TA1S8-*	E	MOUNT CABLE TIE	
18	130	135-004-001	56 590 65/3B	A	FERRITE BEAD	
1	131	136-079-003	ET602-1	G	PWR SPLY 5V-12A/15V-3	PS1
4	146	127-109-004	MS51957-04	A	SCR PAN HD 2-56X5\16	
8	147	127-109-006	MS51957-06	A	SCR PAN HD 2-56X7\16	
8	150	127-109-012	MS51957-12	A	SCR PAN HD 4-40X3\16	
8	151	127-109-013	MS51957-13	A	SCR PAN HD 4-40X1\4	
2	152	127-109-014	MS51957-14	A	SCR PAN HD 4-40X5\16	
5	153	127-109-015	MS51957-15	A	SCR PAN HD 4-40X3/8	
2	154	127-109-017	MS51957-17	A	SCR PAN HD 4-40X1\2	
34	155	127-109-019	MS51957-19	A	SCR PAN HD 4-40X3\4	
1	156	127-109-016	MS51957-16	A	SCR PAN HD 4-40X7\16	

QTY	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
2	157	127-109-027	MS51957-27	A	SCR PAN HD 6-32X5\16	
14	158	127-109-028	MS51957-28	A	SCR PAN HD 6-32X3\8	
2	159	127-109-029	MS51957-29	A	SCR PAN HD 6-32X7\16	
4	160	127-109-030	MS51957-30	A	SCR PAN HD 6-32X1\2	
4	161	127-109-123	MS51957-123	A	SCR PAN HD 6-32X9\16	
8	163	127-109-043	MS51957-43	A	SCR PAN HD 8-32X3\8	
1	165	127-101-062	MS51958-62	A	SCR PAN HD 10-32X7\16	
3	168	127-105-003	MS24693-03	A	SCR 100 FH 4-40X 5\16	
16	169	127-105-004	MS24693-04	A	SCR 100 FH 4-40 X 3/8	
4	172	127-105-025	MS24693-25	A	SCR 100 FH 6-32X 5\16	
3	173	127-105-026	MS24693-26	A	SCR 100 FH 6-32X 3\8	
6	174	127-105-027	MS24693-27	A	SCR 100 FH 6-32X7\16	
4	177	127-105-272	MS24693-272	A	SCR 100 FH 10-32X1\2	
12	182	128-200-802	MS15795-802	A	WASHER FLAT RD NO 2	
2	183	128-200-803	MS15795-803	A	WASHER FLAT RD NO.4	
4	184	128-200-805	MS15795-805	A	WASHER FLAT RD NO.6	
1	185	128-200-808	MS15795-808	A	WASHER FLAT RD NO.10	
4	189	128-202-134	MS35338-134	A	WASHER LK SPLIT NO.2	
10	190	128-202-135	MS35338-135	A	WASHER LK SPLIT NO.4	
12	191	128-202-136	MS35338-136	A	WASHER LK SPLIT NO.6	
1	192	128-202-138	MS35338-138	A	WASHER LK SPLIT NO.10	
12	197	129-001-002	92-1660-02	C	NUT HEX LK MINTR 2-56	
7	198	129-001-003	92-1660-03	C	NUT HEX LK MINTR 4-40	
5	199	129-004-001	22NM107-62	A	NUT SLFLK RED HD 6-32	
56	201	129-005-014	MS-20365-14	A	NUT SELF LOCK 4-40	
20	202	129-005-015	MS-20365-15		NUT SELF-LOCKING 6-32	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	A	A	A																				

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE
LIST OF ACCESSORIES
MODEL 335

CODE IDENT 20747
CONTRACT NO. 4999-11

DRAWN	L. GRUCELLA		ENGINEER	DR McKINNEY	4-18-80	DWG NO. PL354-0160-501 REV A
CHECKED	D.D. Mount	4-29-80	APPROVED	D.D. Mount	4-29-80	
DRAFTING	ES	5-5-80		RJ MARGRAFF	4-30-80	SHEET 1 OF 3

800-0066

All 5-1-80

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			X	1	A	354-0160-501		20747	LIST OF ACCESSORIES	
				2						
				3						
				4						
				5						
				6						
			2	7	A	108-101-011			CONN. FEMALE (34 POS.)	P17, P18 (KEY "T")
			68	8	A	108-101-115			CONTACT, SOCK, 24-26 AWG	USE WITH ITEM 7
				9						
			1	10	A	113-208-002			POWER CORD	P16
				11						
			1	12	A	122-004-001			CARD, PULLER	
				13						
				14			SEE			
				15			SPEC			
				16						
			4	17	A	127-101-063			SCREW, PAN HD, 10-32 X 1/2	
				18						
				19						
			4	20	A	127-105-272			SCREW, FLAT HD, 100°, 10-32 X 1/2	
				21						
				22						

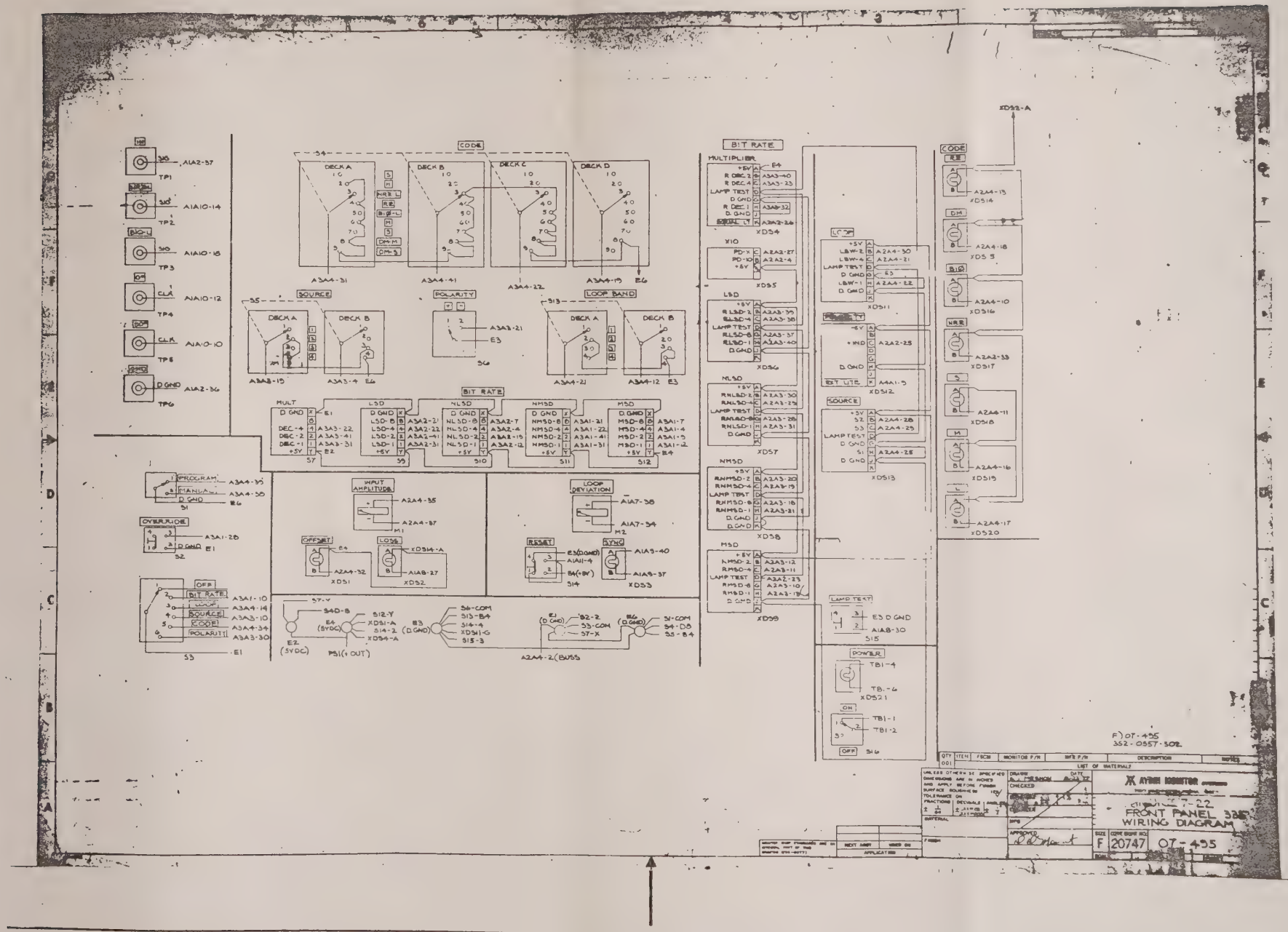
DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
L. GRUCELLA		LIST OF ACCESSORIES	20747	PL354-0160-501	A1
DATE 4-18-80	DATE	MODEL 335		SHEET 2 OF 3	

AYDIN MONITOR SYSTEMS

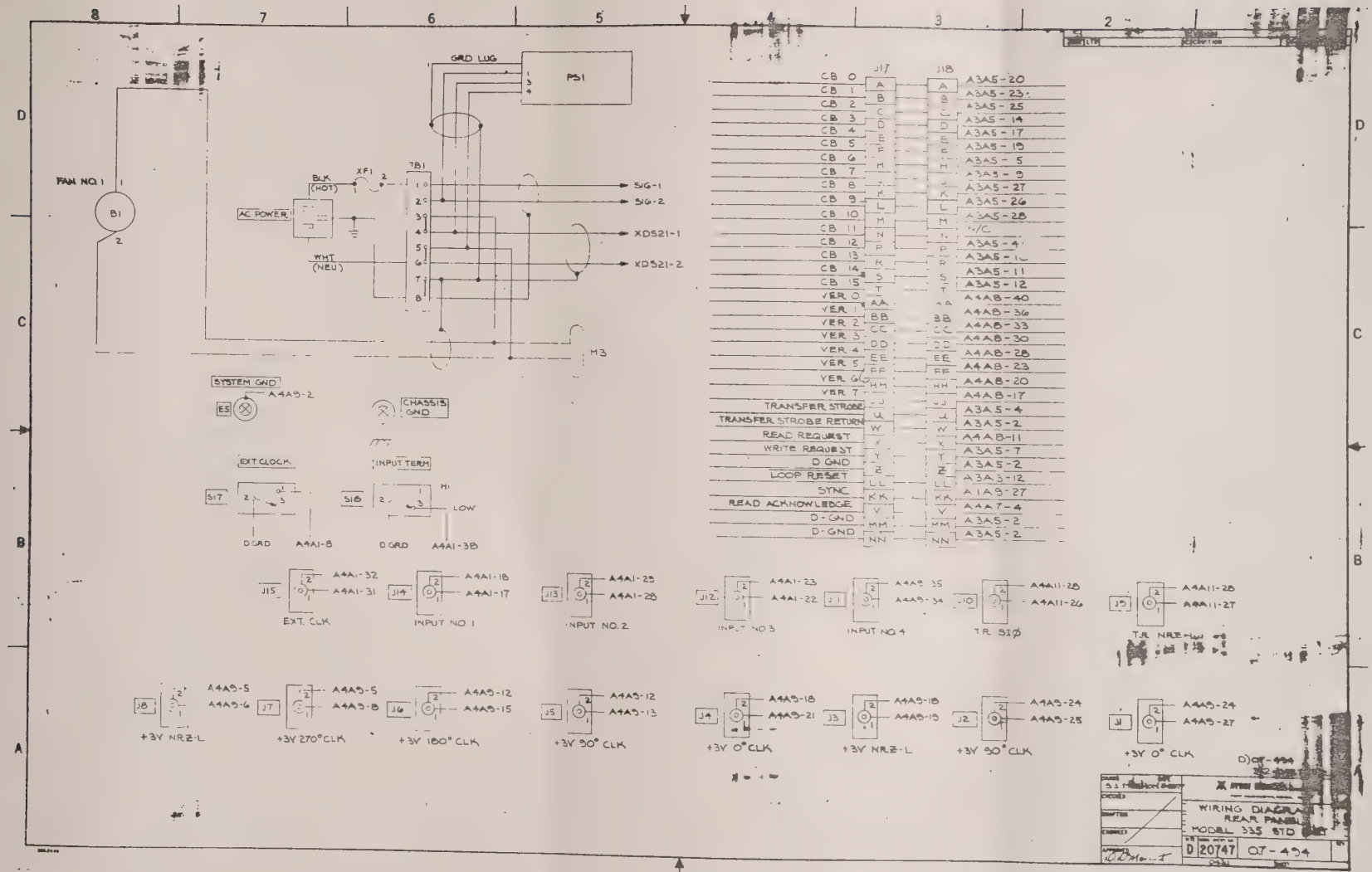
QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			4	23	A	128-200-808			WASHER, FLAT - NO. 10	
				24						
				25						
			4	26	A	128-202-138			WASHER, SPLIT - NO. 10	
				27						
				28			SEE			
			2	29	A	129-003-001	SPEC		NUT, BAR - 10-32	
				30						
				31						
				32						
				33						
			1	34	D	460-0354-2		20747	CARD EXTENDER	

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
L. GRUCELLA DATE 4-18-80	DATE	LIST OF ACCESSORIES MODEL 335	20747	PL354-0160-501 SHEET 3 OF 3	1

800-0438A



CODE
DECK A
DECK B
DECK C
DECK D
SOURCE
POLARITY
LOOP BAND
BIT RATE
MULT
LSD
NLSD
NMSD
MSD
INPUT AMPLITUDE
LOOP DEVIATION
OFFSET
LOSS
RESET
SYNC
PROGRAM
MANUAL
OVERRIDE
OFF
BIT RATE
LOOP
SOURCE
CODE
POLARITY
MULTIPLIER
LAMP TEST
EXT LITE
POWER
ON
OFF
F) 07-495
352-0557-502
LIST OF MATERIALS
AYDIN MONITOR
FRONT PANEL 335
WIRING DIAGRAM
F 20747 07-495


GRD LUG
PS1
FAN NO. 1
B1
BLK (HOT)
XF1
WHT (NEU)
AC POWER
TB1
SIG-1
SIG-2
XDS21-1
XDS21-2
M3
SYSTEM GND
A4A9-2
ES
CHASSIS GND
EXT CLOCK
INPUT TERM
S17
S18
HI
LOW
D GRD
A4A1-8
D GRD
A4A1-38
J17
J18
CB 0
CB 1
CB 2
CB 3
CB 4
CB 5
CB 6
CB 7
CB 8
CB 9
CB 10
CB 11
CB 12
CB 13
CB 14
CB 15
VER 0
VER 1
VER 2
VER 3
VER 4
VER 5
VER 6
VER 7
TRANSFER STROBE
TRANSFER STROBE RETURN
READ REQUEST
WRITE REQUEST
D GND
LOOP RESET
SYNC
READ ACKNOWLEDGE
D-GND
D-GND
A3A5-20
A3A5-23
A3A5-25
A3A5-14
A3A5-17
A3A5-19
A3A5-5
A3A5-9
A3A5-27
A3A5-26
A3A5-28
N/C
A3A5-41
A3A5-10
A3A5-11
A3A5-12
A4AB-40
A4AB-36
A4AB-33
A4AB-30
A4AB-28
A4AB-23
A4AB-20
A4AB-17
A3A5-4
A3A5-2
A4AB-11
A3A5-7
A3A5-2
A3A3-12
A1A9-27
A4A7-4
A3A5-2
A3A5-2
J15
A4A1-32
A4A1-31
EXT. CLK
J14
A4A1-18
A4A1-17
INPUT NO 1
J13
A4A1-29
A4A1-28
INPUT NO. 2
J12
A4A1-23
A4A1-22
INPUT NO 3
J11
A4A9-35
A4A9-34
INPUT NO 4
J10
A4A11-28
A4A11-26
T.R. 31Ø
J9
A4A11-25
A4A11-27
T.R. NRZ-L
J8
A4A9-5
A4A9-6
+3V NRZ-L
J7
A4A9-5
A4A9-8
+3V 270° CLK
J6
A4A9-12
A4A9-15
+3V 180° CLK
J5
A4A9-12
A4A9-13
+3V 90° CLK
J4
A4A9-18
A4A9-21
+3V 0° CLK
J3
A4A9-18
A4A9-19
+3V NRZ-L
J2
A4A9-24
A4A9-25
+3V 90° CLK
J1
A4A9-24
A4A9-27
+3V 0° CLK
WIRING DIAGRAM
REAR PANEL
MODEL 335 STD
D 20747
07-494

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	G THRU V	SEE PL 460-0908-501 FOR PREVIOUS ECO'S	7 3 79	D MOUAT
	W	REVISED PER ECO 04220	7-3-79	F HINKLE
	Y	REVISED PER ECO 06702	7-29-81	J.L2
	Z	REVISED PER ECO 06710		EJ
	AA	REVISED PER ECO 06825		
	AB	REVISED PER ECO 07095	1-27-82	EJ
	AC	REVISED PER ECO 07738	7-[illegible]-82	[illegible]
	AD	REVISED PER ECO 08152	1-18-83	RSV.12

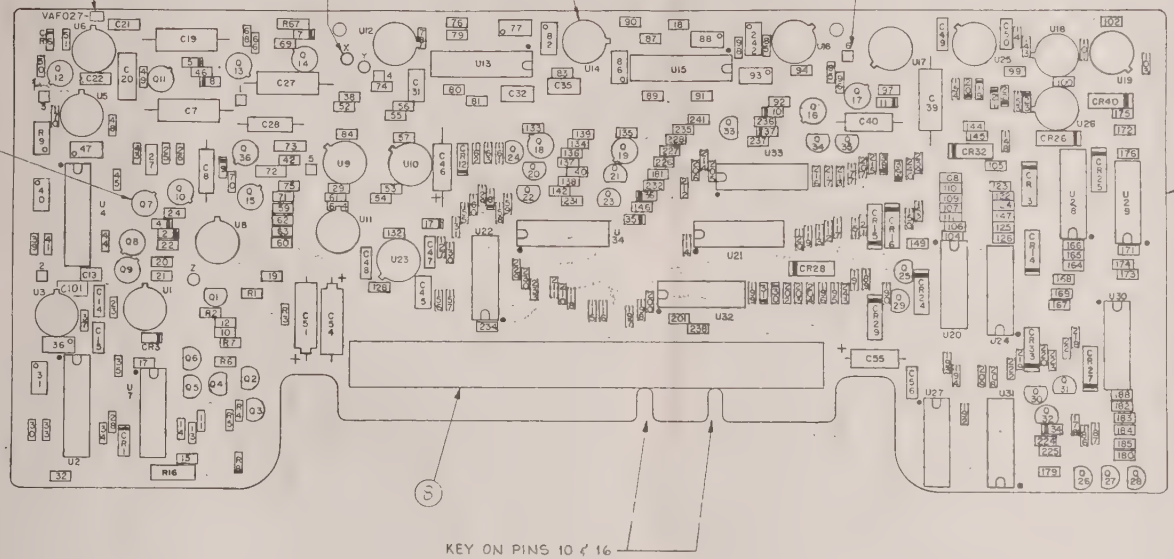
MARK DASH NO. AS REQD.

(163) 3 PLACES (X, Y, & Z) INSTALL FROM NEARSIDE

(152) USE WITH U1, U3, U5, U6, U8, U9, U10, U11, U12, U14, U16, U17, U18, U19, U23, U25, U26.

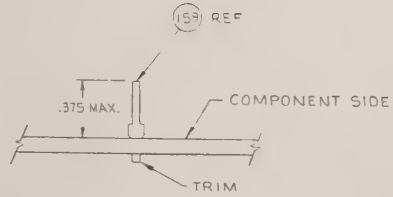
(159) 6 PLACES SEE DETAIL "A"

(151) USE WITH Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q36.



NOTES:

1. DO NOT CRIMP C45 LEAD.
2. COMPONENT DESIGNATIONS NOT USED – C1-C6, C9-C13, C16, C17, C18, C23-C26, C29, C30, C33, C34, C36, C37, C38, C41-C44, C52, C53, C57-C100, R58, R65.



DETAIL - A
SCALE : NONE

FOR PARTS LIST SEE PL-460-0908-□

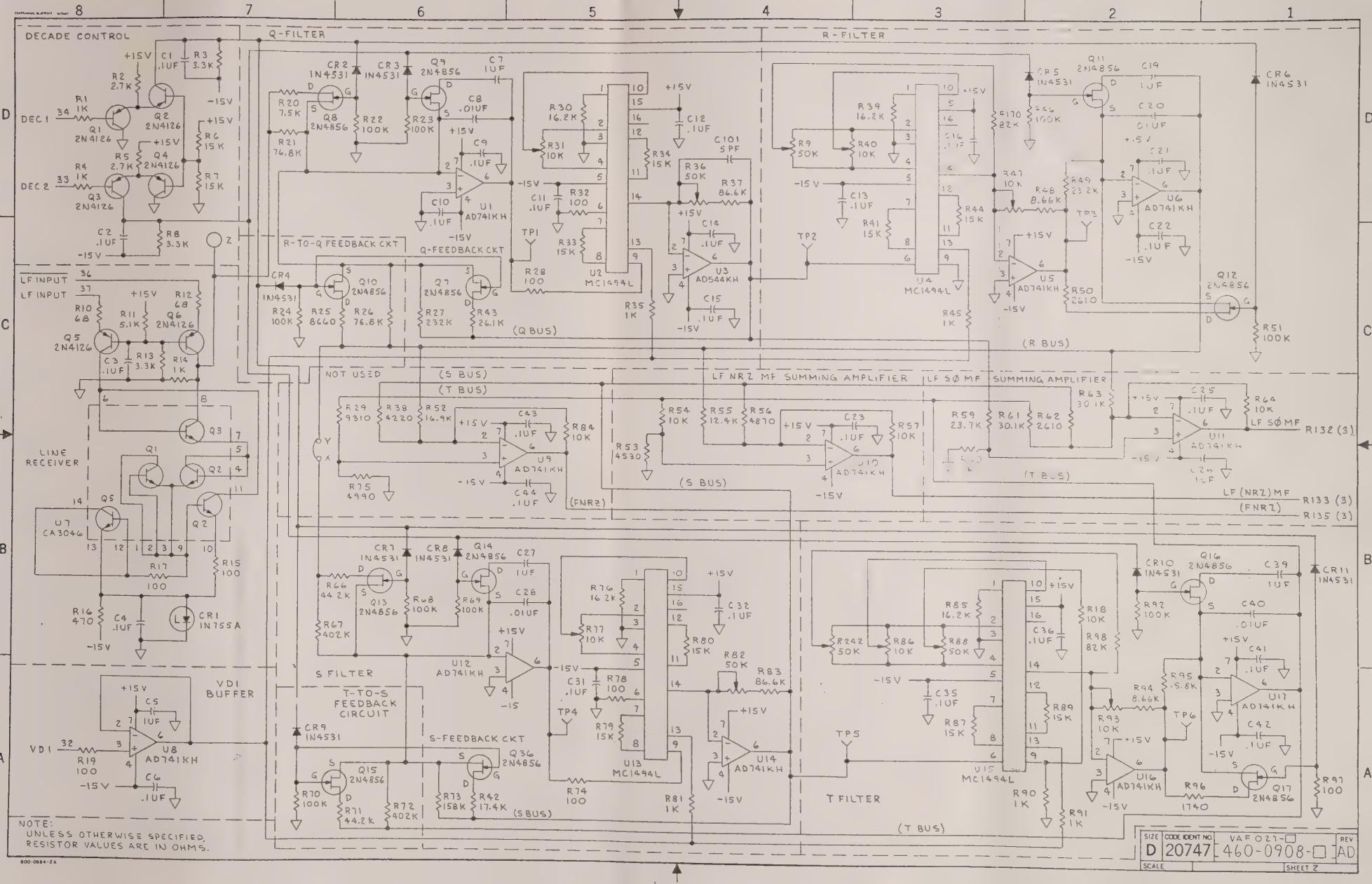
DRAWN	J. WALLACE	DATE 5-12-72
CHECKED	J. HARTZELL	5-23-72
DRAFTING	J. SAMPEDRO	6-5-72
ENGINEER	J. CAMPBELL	5-23-72
MFG	R. HELLER	6-5-72
APPROVED	R. CLEGG	
APPROVED		

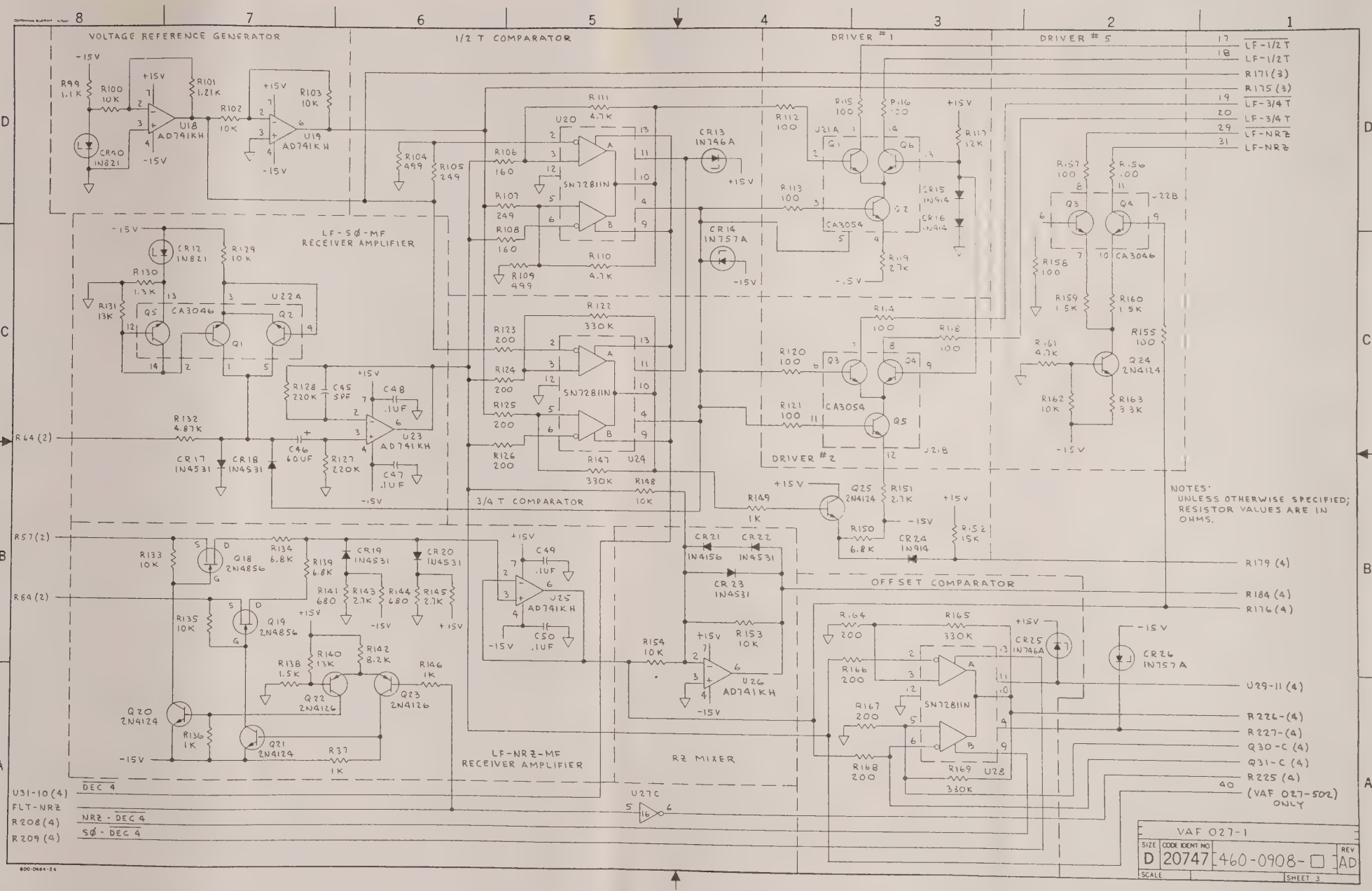
AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

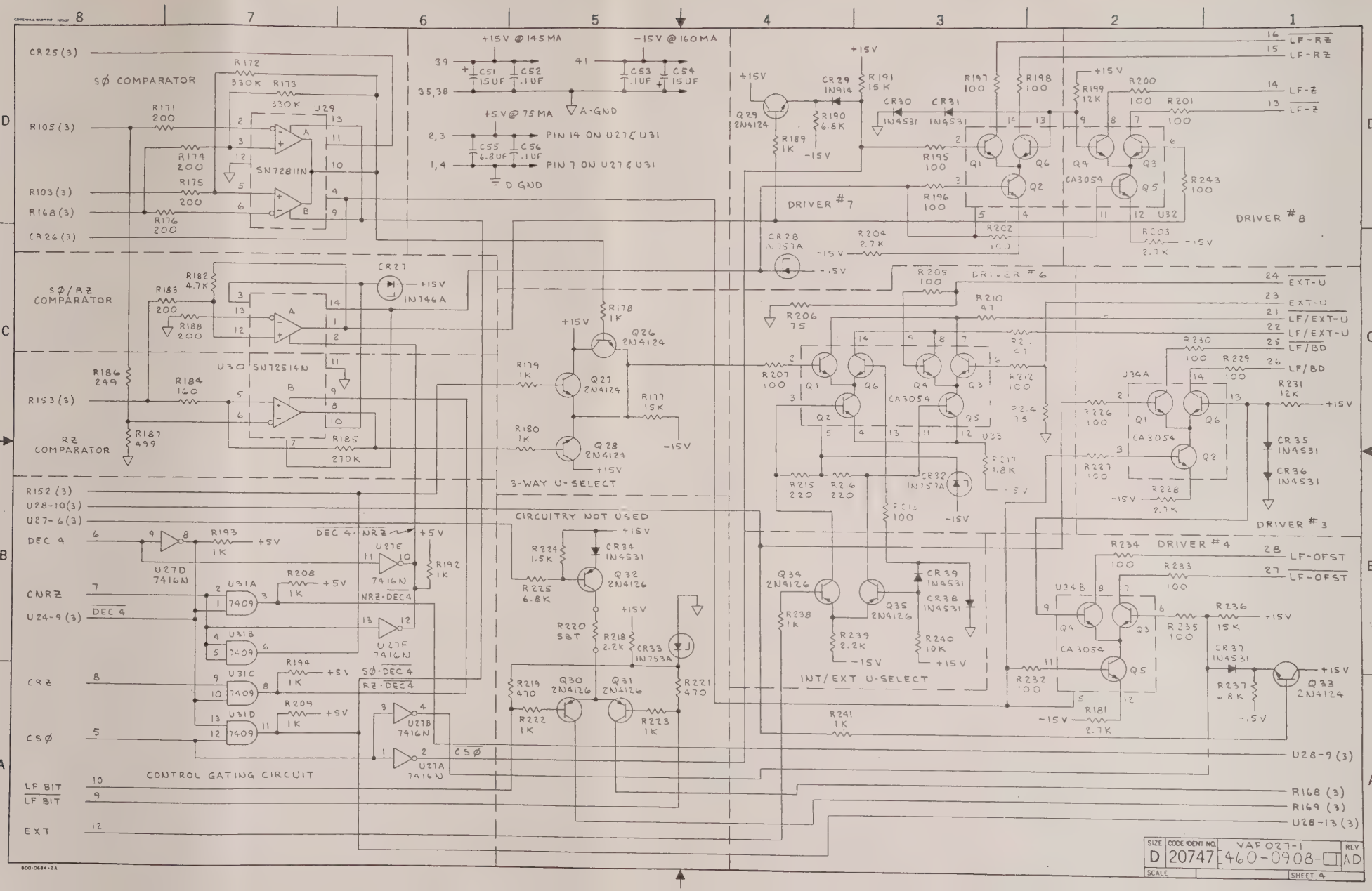
CARD ASSEMBLY
LO FREQ MATCHED FILTER
VAF 027-□

9412		SIZE D	CODE IDENT NO 20747	460-0908-□ REV AD
NEXT ASSY	USED ON	SCALE 2:1		SHEET 1 OF 4
APPLICATION				

800-0684-1A


DECADE CONTROL
Q-FILTER
R-FILTER
LINE RECEIVER
VDI BUFFER
S FILTER
T FILTER
T-TO-S FEEDBACK CIRCUIT
R-TO-Q FEEDBACK CKT
Q-FEEDBACK CKT
S-FEEDBACK CKT
LF NRZ MF SUMMING AMPLIFIER
LF SØ MF SUMMING AMPLIFIER
(Q BUS)
(R BUS)
(S BUS)
(T BUS)
NOT USED
LF INPUT
LF INPUT
DEC 1
DEC 2
LF (NRZ) MF
(FNRZ)
R133 (3)
R135 (3)
R132 (3)
LF SØ MF
NOTE:
UNLESS OTHERWISE SPECIFIED,
RESISTOR VALUES ARE IN OHMS.
SIZE D
CODE IDENT NO. 20747
VAF 027-□ 460-0908-□
REV AD
SCALE
SHEET 2


VOLTAGE REFERENCE GENERATOR
1/2 T COMPARATOR
DRIVER #1
DRIVER #5
LF-SØ-MF RECEIVER AMPLIFIER
3/4 T COMPARATOR
DRIVER #2
OFFSET COMPARATOR
LF-NRZ-MF RECEIVER AMPLIFIER
RZ MIXER
NOTES:
UNLESS OTHERWISE SPECIFIED; RESISTOR VALUES ARE IN OHMS.
VAF 027-1
SIZE D
CODE IDENT NO 20747
460-0908-
REV AD
SCALE
SHEET 3


+15V @ 145 MA
-15V @ 160 MA
+5V @ 75 MA
A-GND
D GND
SØ COMPARATOR
SØ/RZ COMPARATOR
RZ COMPARATOR
SN72811N
SN72514N
3-WAY U-SELECT
CIRCUITRY NOT USED
CONTROL GATING CIRCUIT
INT/EXT U-SELECT
DRIVER #7
DRIVER #8
DRIVER #6
DRIVER #3
DRIVER #4
CR25(3)
R105(3)
R103(3)
R168(3)
CR26(3)
R153(3)
R152(3)
U28-10(3)
U27-6(3)
DEC 4
CNRZ
U24-9(3)
CRZ
CSØ
LF BIT
EXT
U28-9(3)
R169(3)
U28-13(3)
LF-RZ
LF-Z
EXT-U
LF/EXT-U
LF/BD
LF-OFST
SIZE D
CODE IDENT NO. 20747
VAF 027-1
460-0908-
REV AD
SCALE
SHEET 4

REVISIONS

REV	DESCRIPTION		EFFECTIVE ON S/N	DATE	APPROVED
G	REVISED PER ECO 460-0908G	P.A.P.		7-9-73	F. HINKLE
H	REVISED PER ECO 460-0908H			2-11-74	F. HINKLE
J	SEE CO 460-0908J			3-15-74	J. RONEY
K	REVISED PER ECO 00112	P.A.P.		6-19-74	J. RONEY
L	REVISED PER ECO 00807			6-11-75	F. HINKLE
M	REVISED PER ECO 00808	P.A.P.		8-13-75	D. MOUAT
N	REVISED PER ECO 01044	P.A.P.		10-25-75	D. MOUAT
P	REVISED PER ECO 01376	K J M		4-9-76	D. MOUAT
R	REVISED PER ECO 01539	K.J.M		7-13-76	D. MOUAT
S	REVISED PER ECO 02082	K.J.M		7-16-77	J. RONEY
T	REVISED PER ECO 03238	BAKER		5-19-78	D. MOUAT
U	REVISED PER ECO 03321	BAKER		5-24-78	D. MOUAT
V	REVISED PER ECO 03489	BAKER		8-24-78	F. HINKLE
W	REVISED PER ECO 04220	FTB		7-3-79	[illegible]
X	REVISED PER ECO 05688	BAKER 8 NOV 1980		11-10-80	[illegible]
Z	REVISED PER ECO 06790			1-25-81	[illegible]
AA	REVISED PER ECO 06825	A KAYE 4-24-81		7-25-81	[illegible]
AB	REVISED PER ECO 08152	J S 1-8-83		25 JAN 83	RSV 1.2

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	AB	AB	AB	AB	AB	AB	AB	AB	AB														

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
LO FREQ MATCHED FILTER
VAF027-1

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	W. HOUSEAL	5-16-72	ENGINEER	J. CAMPBELL	5-23-72	DWG NO. PL460-0908-501	REV AB
CHECKED	J. HARTZELL	5-[illegible]-72	APPROVED	R. CLEGG	6-6-72		
DRAFTING	J. SAMPEDRO	6-5-72	MFG	R. HELWICK	6-8-72	SHEET 1 OF 9	

800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
		460-0908-501		AB	PARENT VAF027-1	
0		113-001-006	299/1	C	WIRE BUS 26 AWG	
0		114-001-006	SIZE 26 WHITE	J	TUBING TEF 26 AWG WHT	
1	006	400-1099			BOARD P.W. DUMBO	
1	008	108-203-041	7022-041-000001	C	CONN FING BLOC 41 POS	
4	012	102-049-105	625B1A105	A	CAP 1UF 50V 2%	C7 C13 C27 C33
4	013	102-047-103	625B1B103G	A	CAP .01UF 100V 2%	C8 C20 C26 C40
12	015	102-419-104	CY30A104M		CAP .1UF 100V 20%	C14 C15 C21 C23 C31 C32 C35 C47 C48 C49 C50 C56
2	018	102-109-050	DM10/D10		CAP 5PF 500V 5%	C45 C101
1	019	102-370-606	MTP606M020P1B		CAP 60UF 20V 20%	C46
2	020	102-305-156	150D156X0020B2		CAP 15UF 20V 20%	C51 C54
1	021	102-313-685	150D685X0006A2		CAP 6.8UF 6V 20%	C55
1	028	104-056-110	IN755A	P	DIODE ZENER CASE 51	CR1
24	029	104-503-014	1N4531	F	DIODE SIG MINIATURE	CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10 CR11 CR17 CR18 CR19 CR20 CR22 CR23 CR30 CR31 CR34 CR35 CR36 CR37 CR38

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						CR39
2	031	104-308-006	IN821A	D	DILDE ZENER SILICON	CR12
						CR40
3	032	104-056-107	1N746A	P	DIODE ZENER CASE 51	CR13
						CR25
						CR27
4	033	104-056-104	1N757A	P	DIODE ZENER CASE 51	CR14
						CR26
						CR28
						CR32
4	034	104-014-001	1N914	B	DIODE SILICON DO-7	CR15
						CR16
						CR24
						CR29
1	035	104-060-009	IN4156	D	DIODE MULTI-PELLET	CR21
1	036	104-056-105	1N753A	P	DIODE ZENER CASE 51	CR33
13	042	103-304-001	2N4126	D	TRANS SIL PNP TO-92	Q1
						Q2
						Q3
						Q4
						Q5
						Q6
						Q22
						Q23
						Q30
						Q31
						Q32
						Q34
						Q35
14	044	103-350-001	2N4856 OR 2N485	B	TRANS FET TO-18	Q7
						Q8
						Q9
						Q10
						Q11
						Q12
						Q13
						Q14
						Q15
						Q16
						Q17
						Q18
						Q19
						Q36
9	045	103-408-001	2N4124	C	TRANS SIL NPN TO-92	Q20
						Q21
						Q24
						Q25
						Q26
						Q27
						Q28
						Q29
						Q33
24	052	100-017-102	RC05GF102J		RES 1K 1/8W 5%	R1
						R4
						R35

PL460-0908-501 AB
SHEET 3

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						R45 R81 R90 R91 R136 R137 R146 R149 R178 R179 R180 R189 R192 R193 R194 R208 R209 R222 R223 R238 R241
10	056	100-017-272	RC05GF272J		RES 2.7K 1/8W 5%	R2 R5 R119 R143 R145 R151 R181 R203 R204 R228
4	058	100-017-332	RC05GF332J		RES 3.3K 1/8W 5%	R3 R8 R13 R163
5	059	100-017-153	RC05GF153J		RES 15K 1/8W 5%	R6 R152 R177 R191 R236
3	060	100-017-152	RC05GF152J		RES 1.5K 1/8W 5%	R7 R138 R224
5	061	101-130-012	548-00HS-50K	C	POT 50K 1/2W 10%	R9 R36 R82 R88 R242
2	062	100-017-680	RC05GF680J		RES 68 1/8W 5%	R10 R12
1	063	100-017-512	RC05GF512J		RES 5.1K 1/8W 5%	R11
2	064	100-222-1001	RN50C1001F		RES 1K 1/20W 1%	R14 R60
2	065	100-222-1000	RN50C1000F		RES 100 1/20W 1%	R15 R17

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
1	066	100-005-471	RC20	D	RES 470 OHMS 1/2W 5%	R16
5	067	100-017-103	RC05GF103J		RES 10K 1/8W 5%	R18
						R133
						R135
						R162
						R240
37	068	100-017-101	RC05GF101J		RES 100 1/8W 5%	R19
						R28
						R32
						R74
						R78
						R112
						R113
						R114
						R115
						R116
						R118
						R120
						R121
						R155
						R156
						R157
						R158
						R195
						R198
						R196
						R197
						R200
						R201
						R202
						R205
						R207
						R212
						R213
						R226
						R227
						R229
						R230
						R232
						R233
						R234
						R235
						R243
1	073	100-222-7501	RN50C7501F		RES 7.50K 1/20W 1%	R20
2	074	100-222-7682	RN50C7682F		RES 76.8K 1/20W 1%	R21
						R26
10	075	100-017-104	RC05GF104J		RES 100K 1/8W 5%	R22
						R23
						R24
						R43
						R51
						R62
						R69
						R70
						R92

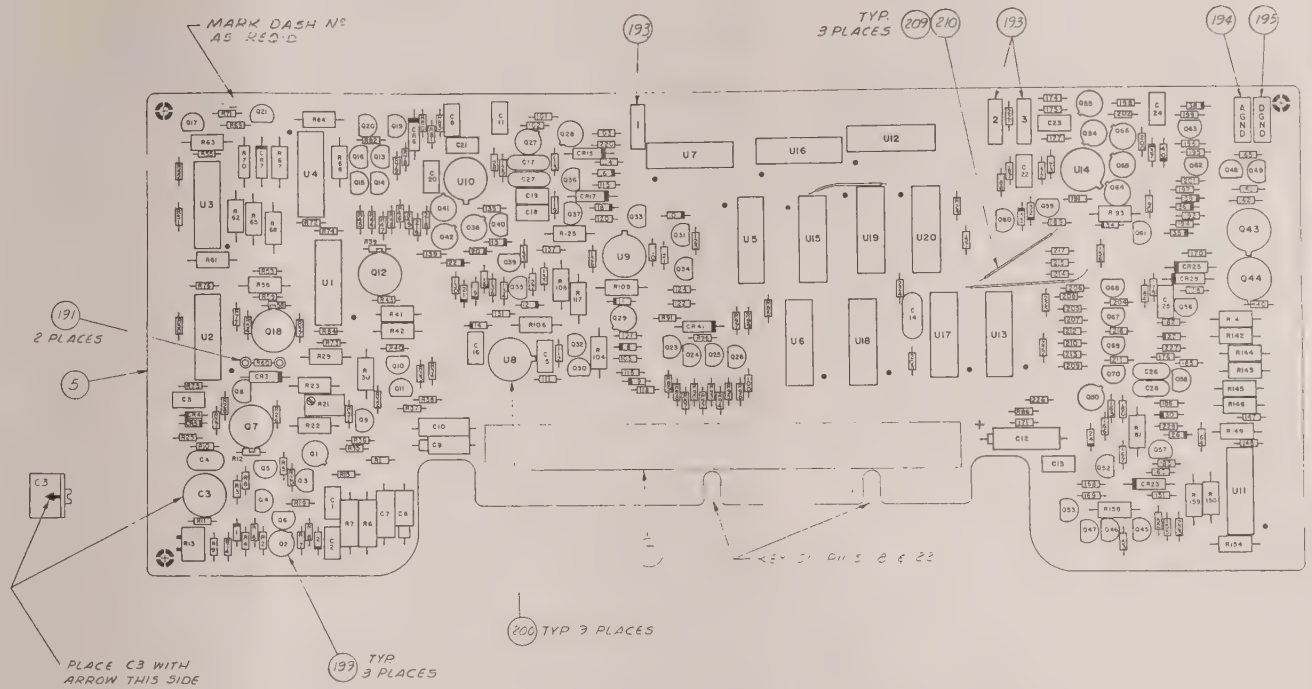
QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
3	077	100-222-8661	RN50C8661F		RES 8.66K 1/20W 1%	R97 R25 R48
1	078	100-215-2323	RN55D2323F		RES 232K 1/8W 1%	R94
1	079	100-222-9311	RN50C9311F		RES 9.31K 1/20W 1%	R27
4	080	100-222-1622	RN50C1622F		RES 16.2K 1/20W 1%	R29 R30 R39 R76
6	081	101-130-010	548-00HS-10K	C	POT 10K 1/2W 10%	R85 R31 R40 R47 R77 R86
8	082	100-222-1502	RN50C1502F		RES 15K 1/20W 1%	R93 R33 R34 R41 R44 R79 R80 R87 R89
2	084	100-222-8662	RN50C8662F		RES 86.6K 1/20W 1%	R37 R8[illegible]
1	085	100-222-4221	RN50C4221F		RES 4.22K 1/20W 1%	R38
1	086	100-222-1742	RN50C1742F		RES 17.4K 1/20W 1%	R42
1	087	100-222-2612	RN50C2612F		RES 26.1K 1/20W 1%	R43
1	088	100-222-2322	RN50C2322F		RES 23.2K 1/20W 1%	R49
2	089	100-222-2611	RN50C2611F		RES 2.61K 1/20W 1%	R50 R62
1	090	100-222-1692	RN50C1692F		RES 16.9K 1/20W 1%	R52
1	091	100-222-4531	RN50C4531F		RES 4.53K 1/20W 1%	R53
11	092	100-222-1002	RN50C1002F		RES 10K 1/20W 1%	R54 R57 R64 R84 R100 R102 R103 R129 R148 R153 R154
1	095	100-222-1242	RN50C1242F		RES 12.4K 1/20W 1%	R55
2	096	100-222-4871	RN50C4871F		RES 4.87K 1/20W 1%	R56 R132
1	097	100-222-2372	RN50C2372F		RES 23.7K 1/20W 1%	R59
2	098	100-222-3012	RN50C3012F		RES 30.1K 1/20W 1%	R61 R63
2	099	100-222-4422	RN50C4422F		RES 44.2K 1/20W 1%	R66 R71
2	100	100-215-4023	RN55D4023F		RES 402K 1/8W 1%	R6[illegible] R72

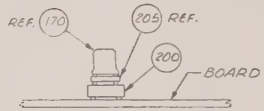
QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
1	101	100-215-1583	RN55D1583F		RES 158K 1/8W 1%	R73
1	102	100-222-4991	RN50C4991F		RES 4.99K 1/20W 1%	R75
1	103	100-222-1582	RN50C1582F		RES 15.8K 1/20W 1%	R95
1	104	100-222-1741	RN50C1741F		RES 1.74K 1/20W 1%	R96
2	105	100-017-823	RC05GF823J		RES 82K 1/8W 5%	R98
						R170
1	106	100-017-112	RC05GF112J		RES 1.1K 1/8W 5%	R99
1	107	100-222-1211	RN50C1211F		RES 1.21K 1/20W 1%	R101
3	108	100-222-4990	RN50C4990F		RES 499 1/20W 1%	R104
						R109
						R187
3	109	100-222-2490	RN50C2490F		RES 249 1/20W 1%	R105
						R107
						R186
3	110	100-017-161	RC05GF161J		RES 160 1/8W 5%	R106
						R108
						R184
4	111	100-017-472	RC05GF472J		RES 4.7K 1/8W 5%	R110
						R111
						R161
						R182
3	112	100-017-123	RC05GF123J		RES 12K 1/8W 5%	R117
						R199
						R231
6	113	100-017-334	RC05GF334J		RES 330K 1/8W 5%	R122
						R147
						R165
						R169
						R172
						R173
14	115	100-017-201	RC05GF201J		RES 200 1/8W 5%	R123
						R124
						R125
						R126
						R164
						R166
						R167
						R168
						R171
						R174
						R175
						R176
						R183
						R188
2	117	100-017-224	RC05GF224J		RES 220K 1/8W 5%	R127
						R128
1	118	100-017-132	RC05GF132J		RES 1.3K 1/8W 5%	R130
2	119	100-017-133	RC05GF133J		RES 13K 1/8W 5%	R131
						R140
6	120	100-017-682	RC05GF682J		RES 6.8K 1/8W 5%	R134
						R139
						R150
						R190
						R225
						R237

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
2	122	100-017-681	RC05GF681J		RES 680 1/8W 5%	R141
						R144
1	123	100-017-822	RC05GF822J		RES 8.2K 1/8W 5%	R142
2	124	100-222-1501	RN50C1501F		RES 1.5K 1/20W 1%	R159
						R160
1	125	100-017-274	RC05GF274J		RES 270K 1/8W 5%	R185
2	126	100-017-750	RC05GF750J		RES 75 1/8W 5%	R206
						R214
2	127	100-017-470	RC05GF470J		RES 47 1/8W 5%	R210
						R211
2	128	100-017-221	RC05GF221J		RES 220 1/8W 5%	R215
						R216
1	129	100-017-182	RC05GF182J		RES 1.8K 1/8W 5%	R217
2	130	100-017-222	RC05GF222J		RES 2.2K 1/8W 5%	R218
						R239
2	131	100-017-471	RC05GF471J		RES 470 1/8W 5%	R219
						R221
1	132	100-017-SBT	RC05		RES SBT 1/8W 5%	R220
16	138	139-141-001	AD741KH	E	IC OP AMP 8 PIN TO-99	U1
						U5
						U6
						U8
						U9
						U10
						U11
						U12
						U14
						U16
						U17
						U18
						U19
						U23
						U25
						U26
4	140	139-098-004	MC1494L	C	IC MULTIPLIER 14 PIN	U2
						U4
						U13
						U15
1	141	139-610-001	AD-544KH		IC OP AMP FET 8 PIN	U3
2	142	139-209-002	CA3046	D	IC	U7
						U22
4	143	139-164-001	TL811CN-10	C	IC DIFF COMP 14 PIN	U20
						U24
						U28
						U29
4	144	139-209-009	CA3054	D	TRANS/DIODE ARRAY	U21
						U32
						U33
						U34
1	145	139-046-416	SN7416N-10	A/P	IC TTL 14 PIN	U27
1	146	139-163-005	TL514C	J	IC OP AMP 14 PIN	U30
1	147	139-046-409	SN7409N-10	A/P	IC TTL 14 PIN	U31
14	151	131-013-001	10047	B	PAD TRANS TO 18 4 PIN	
17	152	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	
6	159	131-207-001	85931-2	B	POST .025 SQ 1.016 LG	1
						2

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						3
						4
						5
						6
3	163	118-005-003	1604-2-05	B	TERMINAL TURRET SLDR	X
						Y
						Z

ZONE	LTR	REVISIONS DESCRIPTION		DATE	APPROVED
		SEE PL460-0921-501			
	P	FOR PREVIOUS ECO'S			
	S	REVISED PER ECO #04220		7-19-79	F HINKLE
	T	REVISED PER ECO #05004	DES	3-18-80	D NOAUT
	U	REVISED PER ECO #06800		9-23-81	ES
	V	REVISED PER ECO #06792		9-28-81	ES
	W	REVISED PER ECO #06907	JSG	10-26-81	RS Vol 2
	X	REVISED PER ECO #08200	JSG	25 Feb 83	RS Vol 2





TYPICAL FOR Q7, Q12, Q18, Q43, Q44
SCALE - NONE

NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. Nº A) 401-0010.

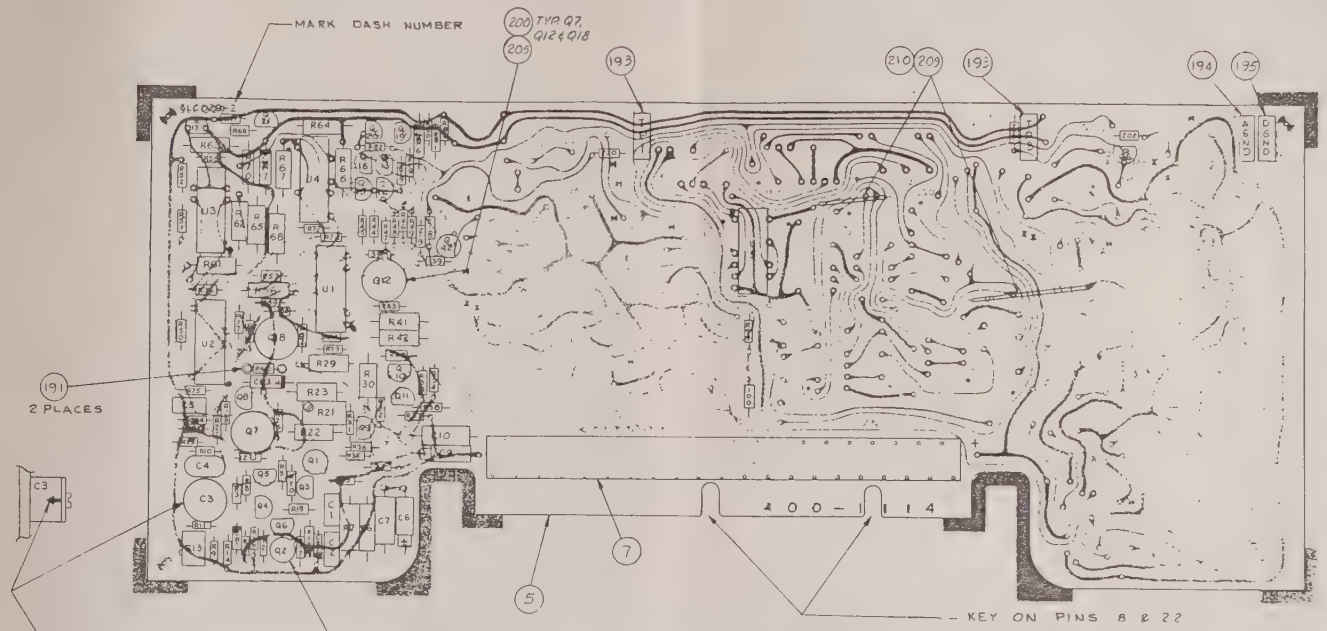
FOR PARTS LIST SEE PL460-0921-□

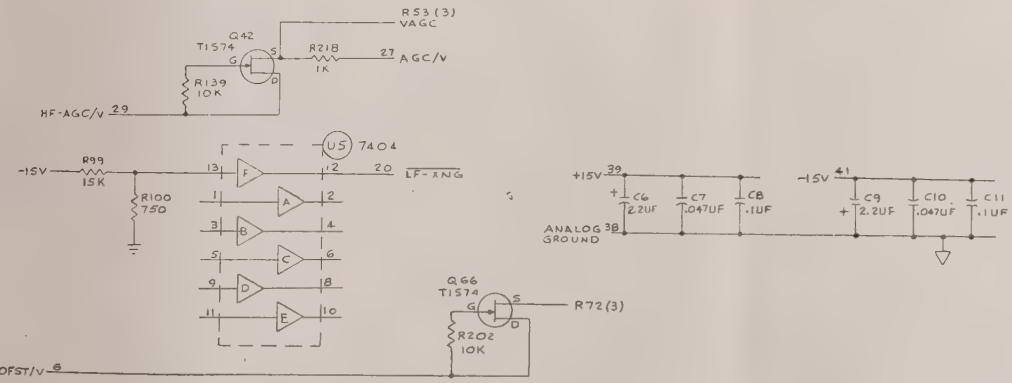
DRAWN	DATE	AYDIN MONITOR SYSTEMS, FORT WASHINGTON PENNA 19034
CHECKED		
DRAFTING		CARD ASSEMBLY SIGNAL LEVEL CONTROL SLC029-1, 3
ENGINEER R. WASSERMAN	3-10-72	
MFG	10-16-72	
APPROVED R. CLEGG	10-25-72	SIZE D · CODE IDENT NO 20747 · 460-0921-501 503 · REV X
APPROVED		SCALE 2:1 · SHEET 1 OF 6

NEXT ASSY	USED ON
APPLICATION	

800-0684-1A

REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED





NOTE
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES, SEE DWG Nr. A) 401-0010.

FOR PARTS LIST SEE PL460-0921-502

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501			LIST OF MATERIALS			

DRAWN	D. MACKLIN	DATE 4-15-76
CHECKED	E S	
DRAFTING	E. STUCKER	5-10-76
ENGINEER	J. BOOTH	4-28-76
MFG	P. HESDON	5-10-76
APPROVED	D. MOUAT	5-10-76
APPROVED	T. JONES	5-10-76

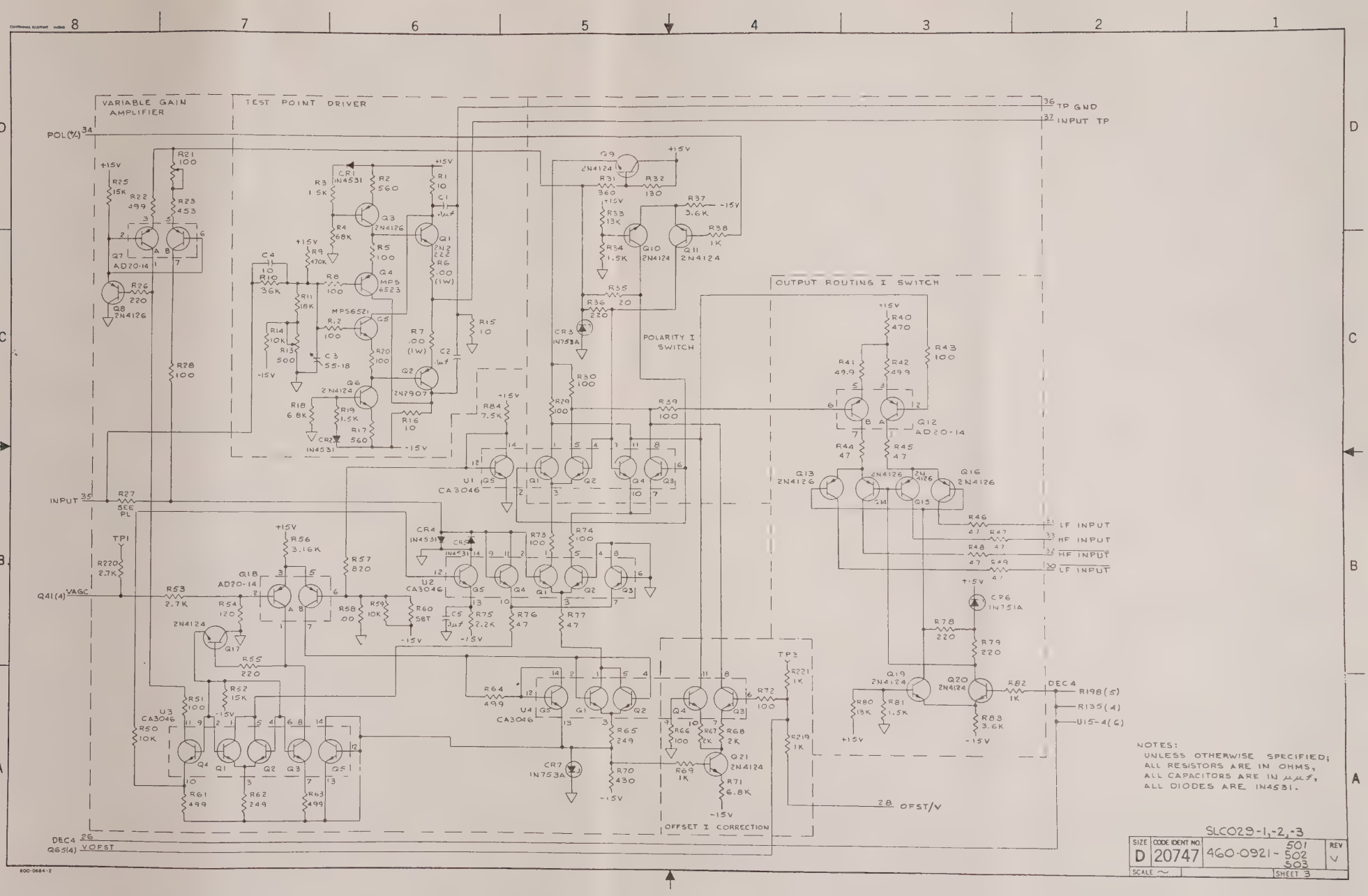
AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNSYLVANIA 19034

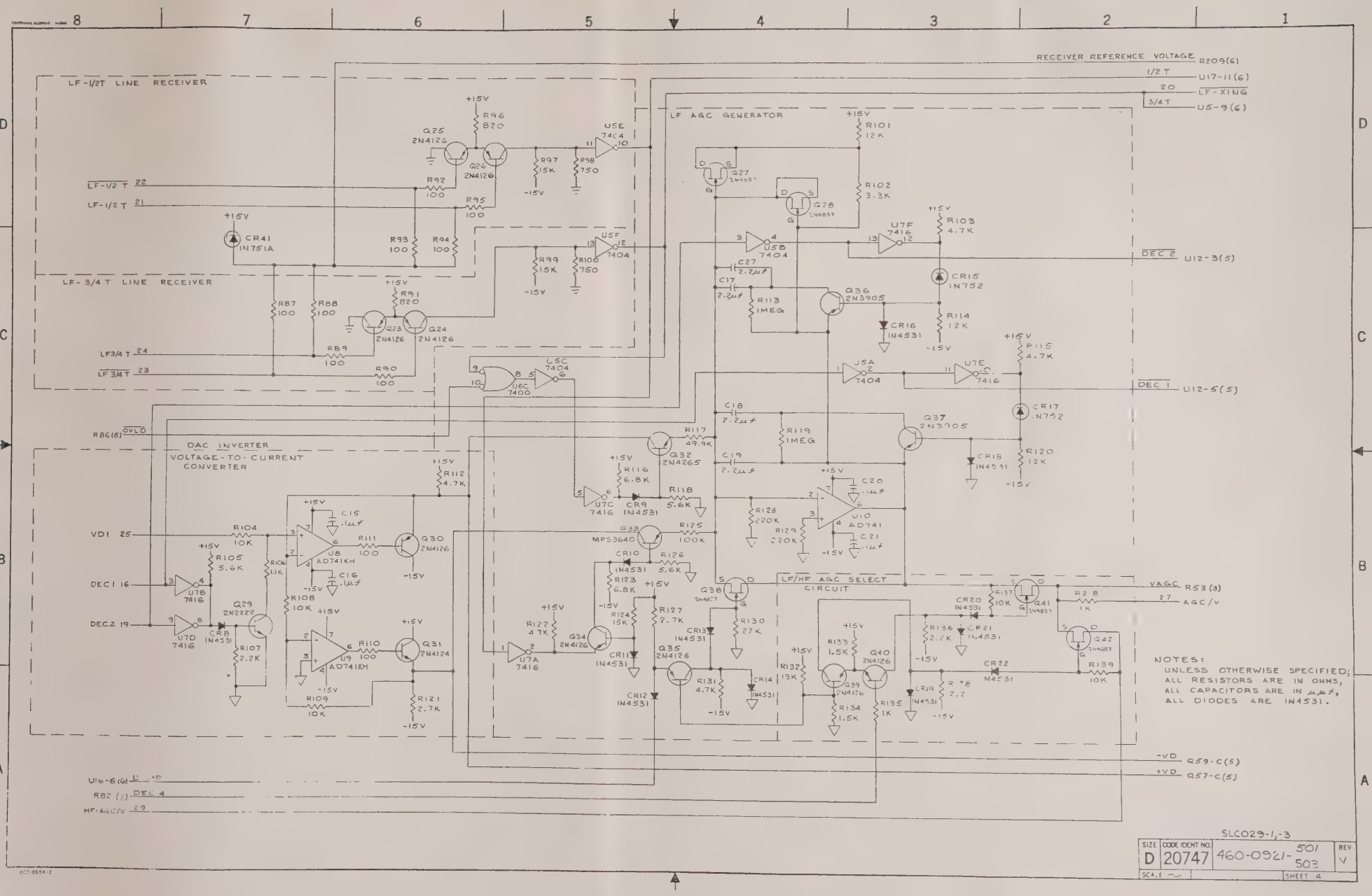
CARD ASSEMBLY
SIGNAL LEVEL CONTROL
SLC 029-2

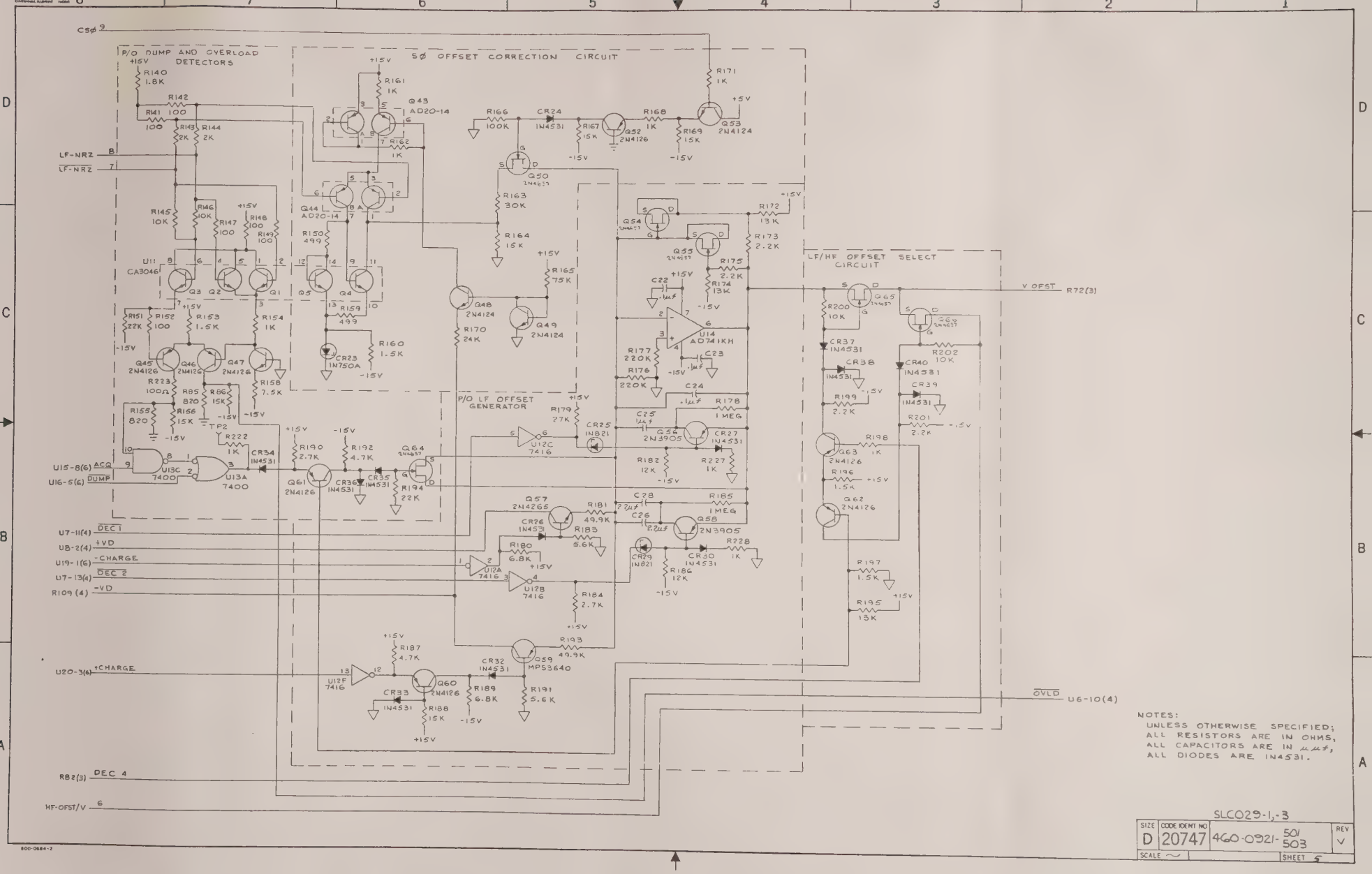
NEXT ASSY	USED ON
	2108
APPLICATION	

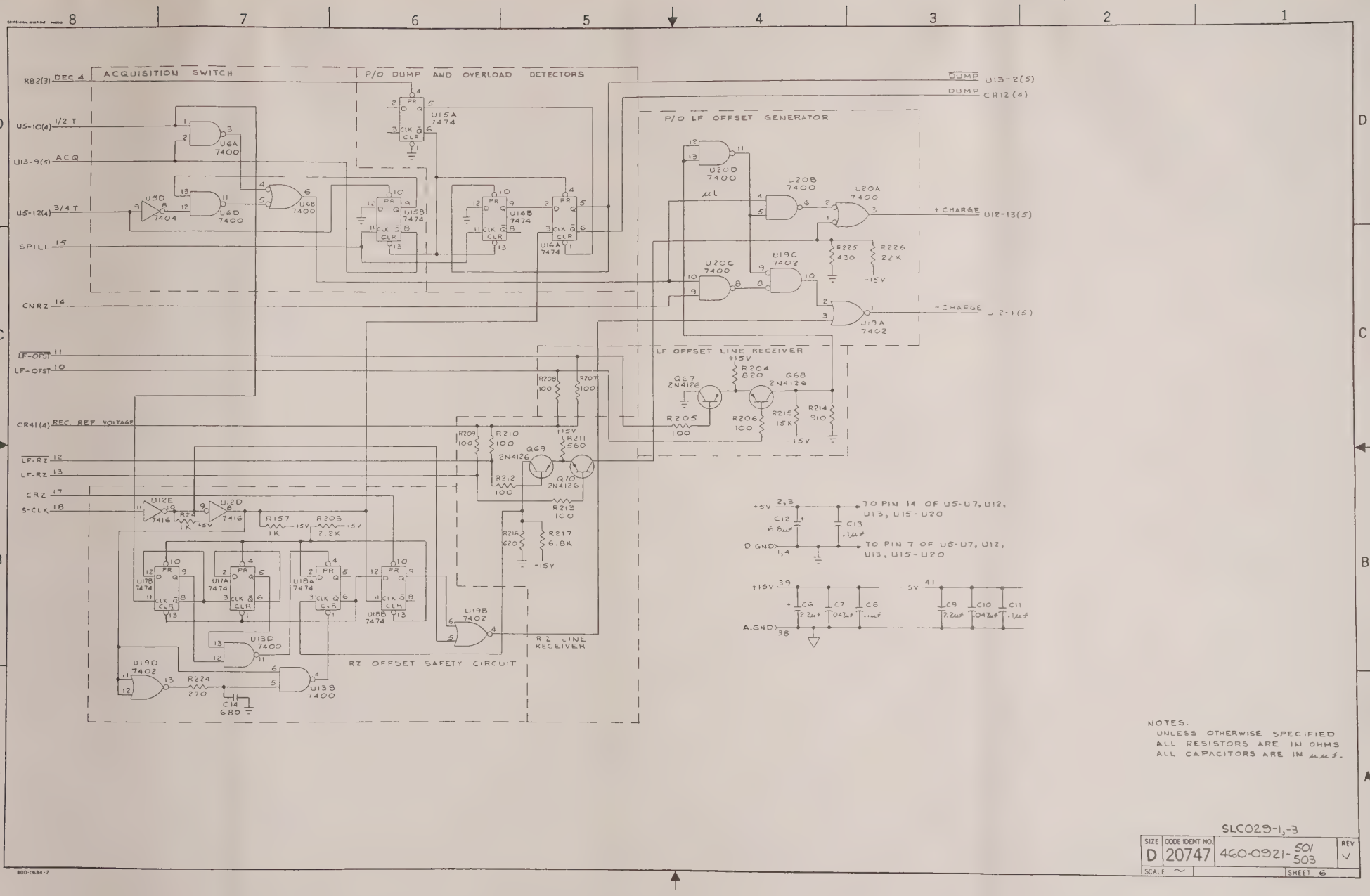
SIZE	CODE IDENT NO		REV
D	20747	460-0921-502	X
SCALE 2:1		SHEET 2	

800-0684-1


VARIABLE GAIN AMPLIFIER
TEST POINT DRIVER
OUTPUT ROUTING I SWITCH
POLARITY I SWITCH
OFFSET I CORRECTION
POL(%) 34
INPUT 35
Q41(4) VAGC
DEC4 Q65(4) VOFST 26
36 TP GND
37 INPUT TP
LF INPUT
HF INPUT
HF INPUT
LF INPUT
DEC4
R198(5)
R135(4)
U15-4(6)
28 OFST/V
U1 CA3046
U2 CA3046
U3 CA3046
U4 CA3046
Q7 AD20-14
Q8 2N4126
Q12 AD20-14
Q18 AD20-14
Q13 2N4126
Q16 2N4126
Q17 2N4124
Q19 2N4124
Q20 2N4124
Q21 2N4124
Q3 2N4126
Q1 2N2222
Q4 MPS6523
Q5 MPS6521
Q6 2N4124
Q2 2N2907
Q9 2N4124
Q10 2N4124
Q11 2N4124
CR1 IN4531
CR2 IN4531
CR3 IN753A
CR4 IN4531
CR5 IN4531
CR6 IN751A
CR7 IN753A
TP1
TP3
NOTES:
UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS ARE IN OHMS,
ALL CAPACITORS ARE IN μμf,
ALL DIODES ARE IN4531.
SLC029-1,-2,-3
SIZE D
CODE IDENT NO. 20747
460-0921-501 502 503
REV V
SCALE ~
SHEET 3


RECEIVER REFERENCE VOLTAGE R209(6)
1/2 T U17-11(6)
20 LF-XING
3/4 T U5-9(6)
LF-1/2T LINE RECEIVER
LF-1/2 T 22
LF-1/2 T 21
LF-3/4 T LINE RECEIVER
LF3/4 T 24
LF 3/4 T 23
LF AGC GENERATOR
DEC 2 U12-3(5)
DEC 1 U12-5(5)
R86(5) OVLD
DAC INVERTER
VOLTAGE-TO-CURRENT CONVERTER
VD1 25
DEC1 16
DEC2 19
LF/HF AGC SELECT CIRCUIT
VAGC R53(3)
27 AGC/V
-VD Q59-C(5)
+VD Q57-C(5)
U16-6(6)
R82 (3) DEC 4
HF-AGC/V 29
NOTES:
UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS ARE IN OHMS,
ALL CAPACITORS ARE IN μμf,
ALL DIODES ARE IN4531.
SLC029-1,-3
SIZE D
CODE IDENT NO. 20747
460-0921-501 503
REV V
SCALE ~
SHEET 4


P/O DUMP AND OVERLOAD DETECTORS
SØ OFFSET CORRECTION CIRCUIT
P/O LF OFFSET GENERATOR
LF/HF OFFSET SELECT CIRCUIT
CSØ 9
LF-NRZ 8
LF-NRZ 7
U15-8(6) ACQ
U16-5(6) DUMP
U7-11(4) DEC 1
U8-2(4) +VD
U19-1(6) -CHARGE
U7-13(4) DEC 2
R109 (4) -VD
U20-3(6) +CHARGE
R82(3) DEC 4
HF-OFST/V 6
V OFST R72(3)
OVLD U6-10(4)
NOTES:
UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS ARE IN OHMS,
ALL CAPACITORS ARE IN μμf,
ALL DIODES ARE IN4531.
SLC029-1,-3
SIZE D
CODE IDENT NO 20747
460-0921-501 503
REV V
SCALE
SHEET 5
800-0684-2



NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE IN OHMS
ALL CAPACITORS ARE IN µµf.

SLC029-1,-3

SIZE	CODE IDENT NO.		REV
D	20747	460-0921-501 503	V
SCALE ~		SHEET 6	

800-0684-2

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
E	REVISED PER ECO 460-0921E		2-6-73	F. HINKLE
F	REVISED PER ECO 460-0921F JCW		3-1-73	F. HINKLE
G	REVISED PER ECO 460-0921G P.A.P.		4-4-73	F. HINKLE
H	REVISED PER ECO 460-0921H P.A.P.		8-27-73	F. HINKLE
L	REVISED PER ECO #00808 P.A.P		8-13-75	J. NEWBY
M	REVISED PER ECO # 01727		10-14-76	D. MOUAT
N	REVISED PER ECO # 02082 JM		7-16-77	J. NEWBY
P	REVISED PER ECO # 02254 JM		5-27-77	J. NEWBY
R	REVISED PER ECO # 03604		11-78	D. MOUAT
S	REVISED PER ECO # 04220 JSG		7-19-79	J Hinkle
T	REVISED PER ECO 05004 DES		3-12-80	D. Mouat
U	REVISED PER ECO 06800		9-28-81	RSVolz
V	REVISED PER ECO 06792		9-28-81	ES
W	REVISED PER ECO 07011 GJM 11-23-81		24NOV81	RS Volz
X	REVISED PER ECO # 07284 JSG		86FEB82	MOISES LEVY PE - [illegible]

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	X	X	X	X	X	X	X	X	X														

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
SIGNAL LEVEL CONTROL
SLC029-1

CODE IDENT 20747
CONTRACT NO. 94 2

DRAWN	J. HARTZELL	3-3-72	ENGINEER	MASSERMAN	3-16-72	DWG NO.	PL460-0921-501	REV X
CHECKED	W. HOUSEAL	9-27-72	APPROVED	R. CLEGG	10-05-72			
DRAFTING	J. SAMPEDRO	10-12-72	MFG	R. HELLER	10-16-72	SHEET 1 OF 9		

800-0066

QPA	ITEM	MONITOR #	MFG PART NUM	REV	DESCRIPTION	REF.DES
		460-0921-501		X	PARENT SLC029-1	
1	005	400-1114			BOARD P.W. DUMBO	
1	007	108-203-341	7022-041-000001	C	CONN FING BLOC 41 POS	
12	010	102-419-104	CY30A104M		CAP .1UF 100V 20%	C1
						C2
						C5
						C8
						C11
						C13
						C15
						C16
						C20
						C21
						C22
						C23
1	013	102-801-002	538-011-A5.5-18	B	CAP 5.5-18PF 350V	C3
1	014	102-109-100	DM10/D10		CAP 10PF 500V 5%	C4
2	015	102-305-225	150D225X0020A2		CAP 2.2UF 20V 20%	C6
						C9
2	016	102-001-473	230B1B473	H	CAP .047UF 100V 20%	C7
						C10
1	017	102-313-685	150D685X0006A2		CAP 6.8UF 6V 20%	C12
1	018	102-121-681	DM15CA681J04CR		CAP 680PF 100V 5%	C14
5	019	102-432-001	CY30C225Z		CAP 2.2UF 50V 20%	C17
						C18
						C26
						C27
						C28
2	020	102-428-104	3420-100C-104K		CAP .01UF 100V 10%	C19
						C24
1	021	102-429-105	3421-100E-105M		CAP 1UF 100V 20%	C25
30	025	104-503-014	1N4531	F	DIODE SIG MINIATURE	CR1
						CR2
						CR4
						CR5
						CR8
						CR9
						CR10
						CR11
						CR12
						CR13
						CR14
						CR16
						CR18
						CR19
						CR20
						CR21
						CR22
						CR24
						CR26
						CR27
						CR30
						CR32
						CR33
						CR34

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						CR35
						CR36
						CR37
						CR38
						CR39
						CR40
2	028	104-056-105	1N753A	P	DIODE ZENER CASE 51	CR3
						CR7
2	029	104-056-106	1N751A	P	DIODE ZENER CASE 51	CR6
						CR41
2	030	104-056-111	1N752A	P	DIODE ZENER CASE 51	CR15
						CR17
1	031	104-056-112	1N750A	P	DIODE ZENER CASE 51	CR23
2	032	104-308-006	IN821A	D	DILDE ZENER SILICON	CR25
						CR39
3	036	100-017-100	RC05GF100J		RES 10 1/8W 5%	R1
						R15
						R16
3	037	100-017-561	RC05GF561J		RES 560 1/8W 5%	R2
						R17
						R211
11	038	100-017-152	RC05GF152J		RES 1.5K 1/8W 5%	R3
						R19
						R34
						R81
						R133
						R134
						R153
						R160
						R164
						R196
						R197
8	042	100-017-682	RC05GF682J		RES 6.8K 1/8W 5%	R4
						R18
						R71
						R116
						R123
						R180
						R189
						R217
34	045	100-017-101	RC05GF101J		RES 100 1/8W 5%	R5
						R8
						R12
						R20
						R28
						R39
						R43
						R51
						R58
						R72
						R73
						R74
						R87
						R88
						R89

QPA	ITEM	MONITOR ...	MFG PART NUM	REV	DESCRIPTION	REF.DES
2	050	100-421-101			RES 100 1W 5%	R6
						R7
1	051	100-017-474	RC05GF474J		RES 470K 1/8W 5%	R9
1	052	100-017-363	RC05GF363J		RES 36K 1/8W 5%	R10
1	053	100-017-183	RC05GF183J		RES 18K 1/8W 5%	R1[illegible]
1	054	101-116-104	502-005-500	C	POT 500 .6W 5%	R1[illegible]
7	055	100-017-103	RC05GF103J		RES 10K 1/8W 5%	R14
						R50
						R59
						R137
						R139
						R200
						R202
1	058	101-101-018	3290W-1-101	H	POT 100 1W 5%	R21
6	059	100-215-4990	RN55D4990F		RES 499 1/8W 1%	R22
						R61
						R63
						R64
						R150
						R179
1	061	100-215-4530	RN55D4530F		RES 453 1/8W 1%	R23
16	062	100-017-102	RC05GF102J		RES 1K 1/8W 5%	R24
						R38
						R67
						R82
						R135
						R157
						R160
						R171
						R198
						R218
						R21
						R220
						R221
						R222
						R227

PL460-0921-501 X
SHEET 4

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						R228
11	067	100-017-153	RC05GF153J		RES 15K 1/8W 5%	R25
						R52
						R86
						R97
						R99
						R124
						R156
						R167
						R169
						R188
						R215
6	071	100-017-221	RC05GF221J		RES 220 1/8W 5%	R26
						R35
						R36
						R55
						R78
						R79
6	073	100-017-123	RC05GF123J		RES 12K 1/8W 5%	R27
						R101
						R114
						R120
						R182
						R186
6	075	100-215-1000	RN55D1000F		RES 100 1/8W 1%	R29
						R30
						R141
						R142
						R66
						R149
1	076	100-017-361	RC05GF361J		RES 360 1/8W 5%	R31
1	077	100-017-131	RC05GF131J		RES 130 1/8W 5%	R32
6	078	100-017-133	RC05GF133J		RES 13K 1/8W 5%	R33
						R80
						R132
						R172
						R174
						R195
2	080	100-017-362	RC05GF362J		RES 3.6K 1/8W 5%	R37
						R83
1	081	100-017-471	RC05GF471J		RES 470 1/8W 5%	R40
2	082	100-215-49R9	RN55D49R9F		RES 49.9 1/8W 1%	R41
						R42
8	083	100-017-470	RC05GF470J		RES 47 1/8W 5%	R44
						R45
						R46
						R47
						R48
						R49
						R76
						R77
6	084	100-017-272	RC05GF272J		RES 2.7K 1/8W 5%	R53
						R121
						R127
						R179

PL460-0921-501 X
SHEET 5

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						R184
						R190
1	086	100-017-121	RC05D...21J		RES 120 1/8W 5%	R54
1	087	100-215-3161	RN55D3161F		RES 3.16K 1/8W 1%	R56
6	089	100-017-821	RC05GF821J		RES 820 1/8W 5%	R57
						R85
						R91
						R96
						R155
						R204
1	091	100-017-SBT	RC05		RES SBT 1/8W 5%	R60
2	092	100-215-2490	RN55D2490F		RES 249 1/8W 1%	R62
						R65
4	094	100-215-2001	RN55D2001F		RES 2K 1/8W 1%	R67
						R68
						R143
						R144
1	095	100-003-431	RC07	D	RES 430 OHMS 1/4W 5%	R70
9	096	100-017-222	RC05GF222J		RES 2.2K 1/8W 5%	R75
						R107
						R136
						R138
						R173
						R17
						R19
						R201
						R203
1	099	100-017-752	RC05GF752J		RES 7.5K 1/8W 5%	R84
2	100	100-017-751	RC05GF751J		RES 750 1/8W 5%	R98
						R100
1	101	100-017-3.2	RC05GF332J		RES 3.3K 1/8W 5%	R102
7	102	100-017-4.2	RC05GF472J		RES 4.7K 1/8W 5%	R103
						R112
						R115
						R122
						R131
						R187
						R192
5	105	100-215-1002	RN55D1002F		RES 10K 1/8W 1%	R104
						R108
						R109
						R145
						R146
5	107	100-017-5.2	RC05GF562J		RES 5.6K 1/8W 5%	R105
						R116
						R126
						R183
						R191
1	109	100-215-1101	RN55D1101F		RES 1.1K 1/8W 1%	R106
4	111	100-017-105	RC05GF105J		RES 1MEG 1/8W 5%	R11
						R11
						R178
						R185
3	113	100-215-4992	RN55D4992F		RES 49.9K 1/8W 1%	R117
						R181

PL460-0921-501 X
SHEET 6

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						R193
1	114	100-215-[illegible]	RN55D1[illegible]		RES 100K 1/8W 1%	R125
4	115	100-017-[illegible]	RC05GF224J		RES 220K 1/8W 5%	R128
						R129
						R176
						R177
4	117	100-017-[illegible]	RC05GF223J		RES 22K 1/8W 5%	R130
						R151
						R194
						R226
1	119	100-017-182	RC05GF182J		RES 1.8K 1/8W 5%	R140
1	120	100-215-1001	RN55D1001F		RES 1K 1/8W 1%	R154
1	121	100-215-7501	RN55D7501F		RES 7.5K 1/8W 1%	R158
2	122	100-222-1001	RN50C1001F		RES 1K 1/20W 1%	R161
						R162
1	123	100-017-303	RC05GF303J		RES 30K 1/8W 5%	R163
1	124	100-017-753	RC05GF753J		RES 75K 1/8W 5%	R165
1	125	100-017-104	RC05GF104J		RES 100K 1/8W 5%	R166
1	126	100-017-242	RC05GF242J		RES 2.4K 1/8W 5%	R170
1	127	100-017-271	RC05GF271J		RES 270 1/8W 5%	R224
1	128	100-017-431	RC05GF431J		RES 430 1/8W 5%	R225
1	129	100-017-621	RC05GF621J		RES 620 1/8W 5%	R216
1	130	100-017-911	RC05GF911J		RES 910 1/8W 5%	R214
2	159	103-019-001	2N2222	B	TRANS SIL NPN TO-18	Q1
						Q29
1	160	103-314-004	JAN2N2907	C	TRANS SIL PNP TO-18	Q2
26	161	103-304-001	2N4126	D	TRANS SIL PNP TO-92	Q3
						Q8
						Q13
						Q14
						Q15
						Q16
						Q23
						Q24
						Q25
						Q26
						Q30
						Q34
						Q35
						Q39
						Q40
						Q45
						Q46
						Q52
						Q60
						Q61
						Q62
						Q63
						Q67
						Q68
						Q69
						Q70
1	165	103-311-006	MPS6523	A	TRANS SIL PNP TO-92	Q4
1	166	103-416-006	MPS6521	B	TRANS SIL NPN TO-92	Q5
13	167	103-408-001	2N4124	C	TRANS SIL NPN TO-92	Q6
						Q9

*** SINGLE LEVEL [illegible] ***
SLB.MFG.ITEM [illegible] JAN 1983 PAGE 8

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						Q10
						Q11
						Q17
						Q19
						Q20
						Q21
						Q31
						Q47
						Q48
						Q49
						Q53
5	170	103-647-008	MPS351	J	TRANS DUAL PNP TO-52	Q7
						Q12
						Q18
						Q43
						Q44
11	172	103-350-002	2N4857	B	TRANS FET TO-18	Q27
						Q28
						Q38
						Q41
						Q42
						Q50
						Q54
						[illegible]
						[illegible]
						Q65
						Q66
2	175	103-403-001	2N4265	A	TRANS SIL NPN TO-92	Q32
						Q57
2	176	103-318-001	MPS3640	A	TRANS SIL PNP TO-92	Q33
						Q59
4	177	103-308-002	2N3905	E	TRANS SIL PNP TO-92	Q36
						Q37
						Q56
						Q58
5	181	139-209-002	CA3046	D	IC	U1
						U2
						U3
						U4
						U11
1	182	139-046-404	SN7404N-10	A/P	IC TTL 14 PIN	U5
3	183	139-046-400	SN7400N-10	A/P	IC TTL 14 PIN	U6
						U13
						U20
2	184	139-046-416	SN7416N-10	A/P	IC TTL 14 PIN	U7
						U12
4	185	139-141-001	AD741KH	E	IC OP AMP 8 PIN TO-99	U8
						U9
						U10
						U[illegible]
4	186	139-046-474	SN7474N-10	A/P	IC TTL 14 PIN	U[illegible]
						U[illegible]
						U[illegible]
						U18
1	187	139-046-402	SN7402N-10	A/P	IC TTL 14 PIN	U19

*** SINGLE LEVEL BILL - BY ITEM ***

SLB.MFG.ITEM 09:42:18 31 JAN 1983 PAGE 9

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
2	191	118-005-003	1604-2-05	B	TERMINAL TURRET SLDR	
3	193	121-202-005	SPCJ-200-05	K	TEST POINT PC GRN	TP1 TP2 TP3
1	194	121-202-009	SPCJ-200-01	K	TEST POINT PC WHT	A GND
1	195	121-202-010	SPCJ-200-03	K	TEST POINT PC BLK	D GND
14	199	131-013-001	10047	B	PAD TRANS TO 18 4 PIN	
9	200	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	
5	205	131-049-001	RC-TO18100-2A	A	PAD TRANS TO18 6PIN	
1	209	113-001-006	29971	C	WIRE BUS 26 AWG	
1	210	114-001-006	SIZE 26 WHITE	J	TUBING TEF 26 AWG WHT	

PL460-0921-501 X
SHEET 9

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO* 460-0903 A → B		7-24-72	F. HINKLE
C	460-0903 C		12-30-72	J. CAMPBELL
D	460-0903 D		3-1-73	F. HINKLE
E	460-0903 E		4-17-73	F. HINKLE
F	460-0903 F		9-9-73	F. HINKLE
G	460-0903 G		9-13-73	F. HINKLE
H	460-0903 H		11-15-73	B. McCLURE
J	460-0903 J		2-14-74	F. HINKLE
K	00931		2-13-75	JRN
L	01124		12-11-75	F. HINKLE
M	02254		6-7-77	J. NENBY
N	REVISED PER ECO # 02831		3-1-78	F. Hinkle
P	REVISED PER ECO 03374 BAKER 6-15-78		6-15-78	F Hinkle
R	REVISED PER ECO 03412 B.R.K. 7-11-78		7-19-78	[illegible]
S	REVISED PER ECO 03553		9/5/ [illegible]	[illegible]
T	REVISED PER ECO 04459 JSG		9-25-79	[illegible]
U	REVISED PER ECO 05520 TJG 7-2-80		15JUL80	RS Vol 2
V	REVISED PER ECO 06398 BAKER 23 MAY 81		26MAY81	RS Vol 2
W	REVISED PER ECO* 07284 JSG		26 FEB 82	MOSES LEVY PE [illegible]

NOTE 4: FOR CAPACITORS C18, C57, C59, C62, & C71, ALTERNATE P/N IS 102-109-☐ (DM10CD___J04CR)

NOTE 5: THE FOLLOWING NUMBERS ARE NOT USED: Q3, Q25, Q28, U4

FOR ASSY DWG SEE 460-0903 ("D" SIZE)
FOR SCHEMATIC SEE 460-0903 ("C" SIZE)

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	W	W	W	W	W	W	W	W															

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE CARD ASSEMBLY
HI-FREQ MATCHED FILTER
VAF026-1,-2

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	THAYNE	4-14-72	ENGINEER	J. CAMPBELL	6-5-72	DWG NO. PL 501 460-0903-502	REV W
CHECKED	R. OLIVIERI	4-25-72	APPROVED	R. CLEARY	6-5-72		
DRAFTING	SAMPEDRO	6-5-72	MANUF	HELLER	6-5-72	SHEET 1 OF 9	

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	1	C	400-1096	————	20747	BOARD, P.W.	
				2						
				3						
		1	1	4	A	108-203-041	7022-041-000-001	91662	CONN., FINGER BLOCK	
				5						
				6						
		23	23	7	A	102-001-473	7FR473-1-A	13934	CAP., .047UF, 100V, 20%	C1, C3, C5, C7 C10, C13, C15 C23, C28, C29 C31, C32, C35 C36, C37, C43 C45, C51, C52 C54, C55, C66, C68
				8						
				9						
				10						
				11						
				12						
		10	10	13	A	102-305-225	150D225X0020A2	56289	2.2 UF, 20V, 20%	C2, C6, C8, C11 C12, C16, C38 C41, C42, C46
				14						
		1	1	15	A	102-109-100	DM10CD100J04CR	72136	10PF, 500V, 5%	C40
		—	5	16	A	102-109-300	DM10CD300J04CR	72136	30PF, 500V, 5%	C4, C9, C14 C39, C44
				17						
		1	1	18	A	102-109-150	DM10CD150J04CR	72136	15PF, 500V, 5%	C17
		1	1	19	A	102-116-101	DM15CA101G04CR	72136	100PF, 100V, 2%	C18 (NOTE 4)
		1	1	20	A	102-118-006	DM15CA102G04CR	72136	1000PF, 100V, 2%	C19 (NOTE 3)
		2	2	21	A	102-109-470	DM10CD470J04CR	72136	47PF, 500V, 5%	C20, C56
		2	2	22	A	102-116-431	DM15CA431G04CR	72136	CAP., 430PF, 100V, 2%	C21, C48 (NOTE 3)

DRAWN DATE	CHECKED DATE	TITLE CARD ASSEMBLY HI-FREQ MATCHED FILTER, VAF026-□	CODE IDENT NO. 20747	DWG NO. 460-0903-□ SHEET 2 OF	REV W

800-04384

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	23	A	102-047-103	625B1B103G	14752	CAP., .01μF, 100V, 2%	C22
		5	5	24	A	102-313-685	150D685X0006A2	56289	6.8μF, 6V, 20%	C30, C34 C50, C53 C69
				25						
		1	1	26	A	102-101-330	DM15CD330J04CR	72136	33PF, 500V, 5%	C33
		1	1	27	A	102-116-620	DM15CA620G04CR	72136	62PF, 100V, 2%	C47
		1	1	28	A	102-047-682	625B1B682G	14752	.0068μF, 100V, 2%	C49
		2	2	29	A	102-116-301	DM15CA301G04CR	72136	300PF, 100V, 2%	C57, C62 (NOTE 3 & 4)
		1	1	30	A	102-047-332	625B1B332G	14752	.0033μF, 100V, 2%	C58
		1	1	31	A	102-116-201	DM15CA201G04CR	72136	200PF, 100V, 2%	C59 (NOTE 3 & 4)
		1	1	32	A	102-116-151	DM15CA151G04CR	72136	150PF, 100V, 2%	C60
		1	1	33	A	102-047-152	625B1B152G	14752	.0015μF, 100V, 2%	C61
		1	1	34	A	102-047-183	625B1B183G	14752	.018μF, 100V, 2%	C63
		1	1	35	A	102-109-201	DM10CD201J04CR	72136	200PF, 500V, 5%	C64 (NOTE 3)
		2	2	36	A	102-305-156	150D156X0020A2	56289	15μF, 20V, 20%	C65, C67
		1	-	37	A	102-109-150	DM10CD150J04CR	72136	15 PF, 500V, 5%	C44
		5	5	38	A	102-419-104	CY30A104M	71590	.1μF, 100V, 20%	C24-C27, C70
		1	1	39	A	102-116-271	DM15CA271G04CR	72136	CAP., 270PF, 100V, 2%	C71
				40						
				41						
		12	12	42	A	104-014-001	1N914	01295	DIODE	CR1-CR12
		1	1	43	A	104-056-110	1N755A	04713	DIODE, ZENER, 7.5V, 5%	CR13
				44						

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		CARD ASSEMBLY HI-FREQ MATCHED FILTER, VAF026-□	20747	460-0903-□ SHEET 3 OF	W

800-0438A

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	45	A	139-046-402	SN7402N-10	01295	I.C., TTL QUAD NOR GATE	U1
		1	1	46	A	139-046-416	SN7416N-10	01295	I.C., TTL HEX INVERTER	U2
		6	6	47	A	139-141-001	AD741KH	24355	I.C., OPAMP	U3, U5-U9
		4	4	48	A	139-209-002	CA3046	02735	I.C., NPN TRANSISTOR ARRAY	U10-U13
				49						
				50						
		6	6	51	A	106-016-002	365-4-1A	20891	RELAY, REED, FORM 1A	K1-K6
		2	2	52	A	106-016-001	365-4-2A	20891	RELAY, REED, FORM 2A	K7, K8
				53						
		4	4	54	A	300-0071-502	———	20747	RAYSISTOR ASSEMBLY	Z1-Z4
				55						
				56						
		1	1	57	A	100-017-512	RC05GF512J	81349	RES, 5.1K, 1/8W, 5%	R1
		1	1	58	A	-017-332	RC05GF332J		3.3K, 1/8W, 5%	R2
		2	2	59	A	-215-1001	RN55C1001F		1K, 1/10W, 1%	R3, R124
		2	2	60	A	-215-1000	RN55C1000F		100Ω, 1/10W, 1%	R4, R5
		1	1	61	A	-215-9091	RN55C9091F		9.09 K, 1/10W, 1%	R6
		2	2	62	A	-215-1002	RN55C1002F		10K, 1/10W, 1%	R7, R28
		1	1	63	A	-215-3241	RN55C3241F		3.24K, 1/10W, 1%	R8
		1	1	64	A	-003-471	RC07GF471J		470Ω, 1/4W, 5%	R9
		6	6	65	A	100-017-681	RC05GF681J	81349	RES, 680Ω, 1/8W, 5%	R10, R18, R21 R29, R45, R48
				66						

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		CARD ASSEMBLY HI-FREQ MATCHED FILTER, VAF026-□	20747	460-0903-□ SHEET 4 OF	W

800-047

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		10	10	67	A	100-017-100	RC05GF100J	81349	RES, 10Ω, 1/8W, 5%	R11, R14, R16, R20 R22, R25, R43 R47, R49, R52
				68						
				69						
		17	17	70	A	-017-101	RC05GF101J		100Ω, 1/8W, 5%	R12, R19, R23 R46, R50, R58 R63, R64, R88 R93, R94, R110 R112, R117, R125 R132, R137
				71						
				72						
				73						
		5	5	74	A	-003-202	RC07GF202J		2K, 1/4W, 5%	R13, R17, R24 R44, R51
				75						
		9	9	76	A	-017-102	RC05GF102J		1K, 1/8W, 5%	R15, R26, R53 R57, R87, R105 R111, R130, R133
				77						
		2	2	78	A	-003-220	RC07GF220J		22Ω, 1/4W, 5%	R27, R30
		7	7	79	A	-017-103	RC05GF103J		10K, 1/8W, 5%	R31, R37, R56 R73, R79, R102 R103
				80						
		4	4	81	A	-003-102	RC07GF102J		1K, 1/4W, 5%	R32, R38 R74, R80
				82						
		8	8	83	A	-215-6040	RN55C6040F		604Ω, 1/10W, 1%	R34, R35, R40 R41, R76, R77 R82, R83
				84						
		3	3	85	A	-017-271	RC05GF271J		270Ω, 1/8W, 5%	R54, R85, R108
		4	4	86	A	100-017-222	RC05GF222J	81349	RES, 2.2K, 1/8W, 5%	R55, R86 R107, R109
				87						
				88						

DRAWN DATE	CHECKED DATE	TITLE CARD ASSEMBLY HI-FREQ MATCHED FILTER, VAF026-0	CODE IDENT NO. 20747	DWG NO. 460-0903-0 SHEET 5 OF	REV W

800-0438A

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		6	6	89	A	100-215-3740	RN55C3740F	81349	RES, 374Ω, 1/10W, 1%	R59, R60, R89
				90						R90, R113, R114
		3	3	91	A	-017-302	RC05GF302J		3K, 1/8W, 5%	R65, R95, R118
		3	3	92	A	-017-362	RC05GF362J		3.6K, 1/8W, 5%	R66, R96, R119
		1	1	93	A	-215-1691	RN55C1691F		1.69K, 1/10W, 1%	R67
		1	1	94	A	-215-2001	RN55C2001F		2K, 1/10W, 1%	R68
		6	6	95	A	-215-3741	RN55C3741F		3.74K, 1/10W, 1%	R69, R70, R98
				96						R99, R121, R122
		1	1	97	A	-215-3011	RN55C3011F		3.01K, 1/10W, 1%	R71
		1	1	98	A	-215-1331	RN55C1331F		1.33K, 1/10W, 1%	R72
		1	1	99	A	-215-2151	RN55C2151F		2.15K, 1/10W, 1%	R97
		1	1	100	A	-215-3401	RN55C3401F		3.4K, 1/10W, 1%	R100
		1	1	101	A	-215-8660	RN558660F		866Ω, 1/10W, 1%	R101
		1	1	102	A	-017-472	RC05GF472J		4.7K, 1/8W, 5%	R104
		1	1	103	A	-017-203	RC05GF203J		20K, 1/8W, 5%	R106
		2	2	104	A	-215-2491	RN55C2491F		2.49K, 1/10W, 1%	R120, R123
		5	5	105	A	-003-122	RC07GF122J		1.2K, 1/4W, 5%	R126-R129, R136
		1	1	106	A	-003-472	RC07GF472J		4.7K, 1/4W, 5%	R131
		2	2	107	A	-017-680	RC05GF680J		68Ω, 1/8W, 5%	R134, R135
		1	1	108	A	100-017-470	RC05GF470J	81349	RES, 47Ω, 1/8W, 5%	R139
		6	6	109	A	100-215-75R0	RN55C75R0F	81349	RES, 75Ω, 1/10W, 1%	R61, R62, R91, R92, R115, R116
		1	1	110	A	100-017-431	RC05GF431J	81349	RES, 430Ω, 1/8W, 5%	R138

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
DATE	DATE	CARD ASSEMBLY HI-FREQ MATCHED FILTER, VAF026-□	20747	460-0903-□ SHEET 6 OF	W

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		5	5	111	A	103-304-001	2N4126	04713	TRANSISTOR, PNP	Q1, Q2, Q23, Q29, Q34
				112						
				113						
		–	3	114	A	103-314-004	2N2907	04713	TRANSISTOR, PNP	Q4, Q10, Q20
		1	–	115	A	103-314-004	2N2907	04713	TRANSISTOR, PNP	Q4
				116						
		–	6	117	A	103-416-006	MPS6521	04713	TRANSISTOR, NPN	Q5, Q6, Q11, Q12, Q21, Q22
				118						
		2	–	119	A	103-416-006	MPS6521	04713	TRANSISTOR, NPN	Q5, Q6
				120						
		–	4	121	A	103-311-006	MPS6523	04713	TRANSISTOR, PNP	Q7, Q8, Q17, Q18
				122						
		6	–	123	A	103-438-001	2N5771	07263	TRANSISTOR, PNP	Q7, Q8, Q10, Q17, Q18, Q20
				124						
				125						
		–	6	126	A	103-019-001	2N2222	04713	TRANSISTOR, NPN	Q9, Q15, Q16, Q19, Q26, Q27
				127						
				128						
		6	–	129	A	103-437-001	2N5770	07263	TRANSISTOR, NPN	Q9, Q11, Q12, Q19, Q21, Q22
				130						
				131						
		1	1	132	A	103-314-202	2N2905	04713	TRANSISTOR, PNP	Q13

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		CARD ASSEMBLY HI-FREQ MATCHED FILTER, VAF026-□	20747	460-0903-□ SHEET 7 OF	W

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	133	A	103-419-002	2N2219	04713	TRANSISTOR, NPN	Q14
				134						
		4	-	135	A	103-019-001	2N2222	04713	TRANSISTOR, NPN	Q15,Q16,Q26,Q27
				136						
		3	3	137	A	103-647-008	AD821	24355	TRANSISTOR, DUAL, PNP	Q24, Q30, Q35
				138						
		3	3	139	A	103-408-001	2N4124	04713	TRANSISTOR, NPN	Q31, Q32, Q33
				140						
				141						
				142						
		-	9	143	A	131-013-001	10047	07047	PAD, TRANSISTOR	USE WITH Q4,9,10,15, Q16,19,20,26,27
		5	1	144	A	131-013-001	10047	07047	PAD, TRANSISTOR	USE WITH Q4,15,16, Q26,27
				145						
		2	2	146	A	131-014-001	10030	07047	PAD, TRANSISTOR	USE WITH Q13, Q14
				147						
		7	7	148	A	131-015-001	10037	07047	PAD, TRANSISTOR	USE WITH Z1-Z4, Q24, Q30, Q35
				149						
		6	6	150	A	131-017-001	10383	07047	PAD, TRANSISTOR	USE WITH U3, U5, U6-U9
				151						
		3	3	152	A	131-049-001	RC-T018100-2A	19080	PAD, TRANSISTOR	USE WITH Q24,30,35
				153						
		5	5	154	A	131-020-001	10284-N	07047	COVER, TO-5	USE WITH Z1-Z4, Q13

DRAWN

DATE

CHECKED

DATE

TITLE CARD ASSEMBLY
HI-FREQ. MATCHED FILTER, VAF026-□

CODE IDENT NO. 20747

DWG NO. 460-0903-□

SHEET 8 OF

REV W

800-0

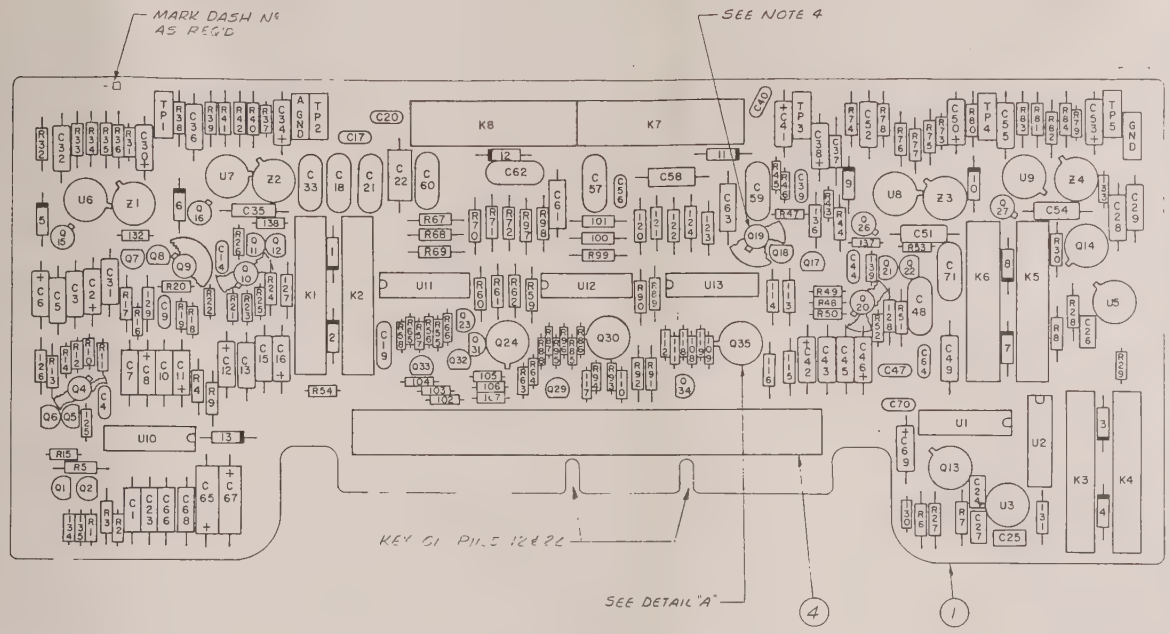
AYDIN MONITOR SYSTEMS

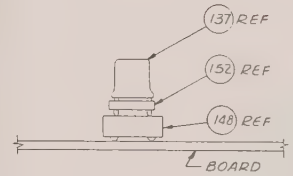
QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
				155						
		-	5	156	A	116-002-004	TXBF-019-025B	98978	HEAT SINK	USE WITH Q4, Q9, Q10, Q19, Q20
		1	-	157	A	116-002-004	TXBF-019-025B	98978	HEAT SINK	USE WITH Q4
				158						
				159						
				160						
		5	5	161	A	121-202-005	8041-1G7	91506	TEST JACK, GRN	TP1 - TP5
		1	1	162	A	121-202-009	8041-1G9	91506	TEST JACK, WHT	A GND
		1	1	163	A	121-202-010	8041-1G6	91506	TEST JACK, BLK	D GND
				164						
				165						
		AR	AR	166	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571
				167						
				168						
				169						
				170						
				171						
				172						
				173						
				174						
				175						
				176						

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		CARD ASSEMBLY HI-FREQ. MATCHED FILTER, VAF026-□	20747	460-0903-□ SHEET 9 OF	W

800-0438A

ZONE	LTR	REVISIONS DESCRIPTION		DATE	APPROVED
		"B" TO "S" SEE P/L FOR ECO Nos			
	T	REVISED PER ECO #04459	JSG	7-25-79	F. Hunter
	U	REVISED PER ECO 06378	BOARD 23 MAY 81	26 MAY 81	RS Volz
	V	REVISED PER ECO #06863	JSG	10-1-81	R. MARSHIFF
	W	REVISED PER ECO #07284	JSG	26 FEB 82	MOISES LOPEZ





DETAIL "A"
(NO SCALE)
TYP. FOR Q24, Q30, Q35

NOTES:

1- FOR GENERAL MANUFACTURING & ENGINEERING NOTES, SEE DWG Nº A)401-0010.

2- RAYSISTORS & SBT RESISTORS (ITEM 54) ARE SUPPLIED AS SETS. SBT RESISTORS ARE IDENTIFIED AS HIGH AND LOW. INSTALL PER TABLE #1.

3.- DO NOT CRIMP LEADS OF C19, C21, C48, C57, C59, C60, C62, C64, C71.

4.- FOR -502 ASSY THE ORIENTATION OF Q9, Q10, Q19, Q20 ARE AS SHOWN. Q9 Q10 Q19 Q20

TABLE 1

	HI	LOW
Z1	R33	R36
Z2	R39	R42
Z3	R75	R78
Z4	R81	R84

FOR PARTS LIST SEE PL 460-0903-☐

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501	LIST OF MATERIALS					

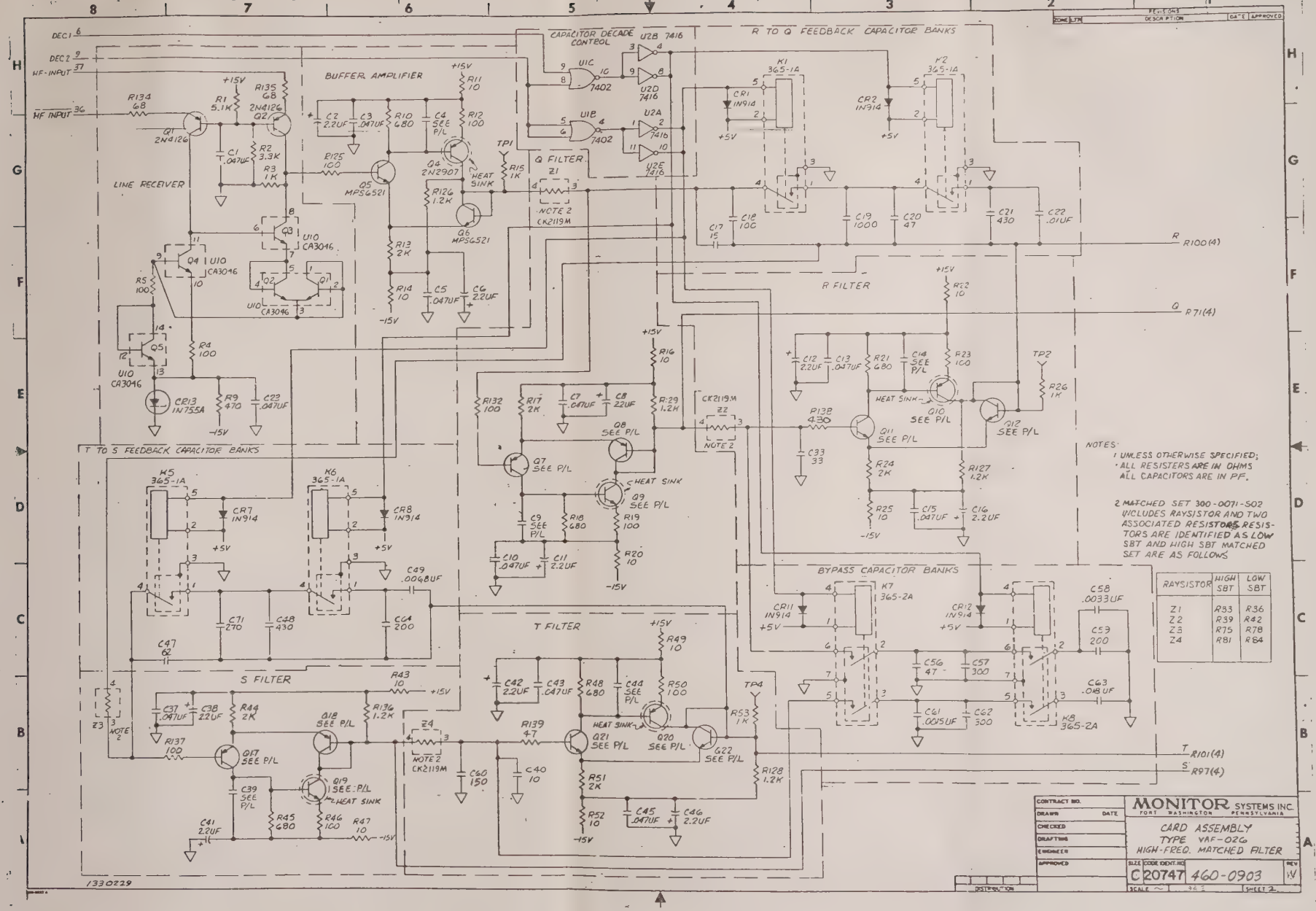
DRAWN A. THAYNE	DATE 4-14-72	AYDIN MONITOR SYSTEMS, FORT WASHINGTON, PENNA. 19034
CHECKED J. SEMTERI	4-25-72	
DRAFTING J. SAMPEDRO	6-5-72	CARD ASSEMBLY HI-FREQ MATCHED FILTER VAF026-1, -2
ENGINEER J. CAMPBELL	6-5-72	
MFG. R. HELLER	6-5-72	
APPROVED R. CLEGG	6-6-72	
APPROVED		

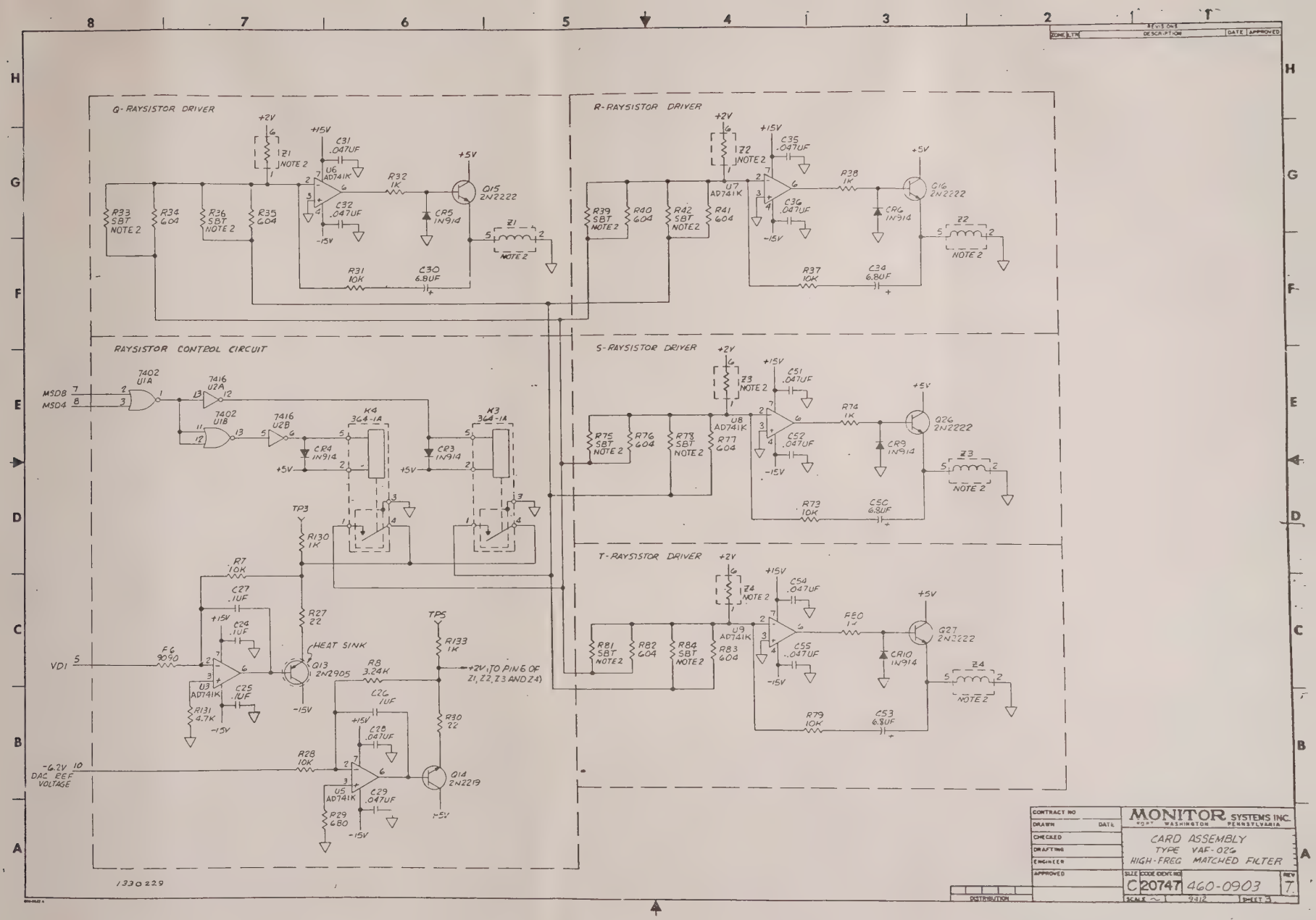
NEXT ASSY	USED ON
	9412
APPLICATION	

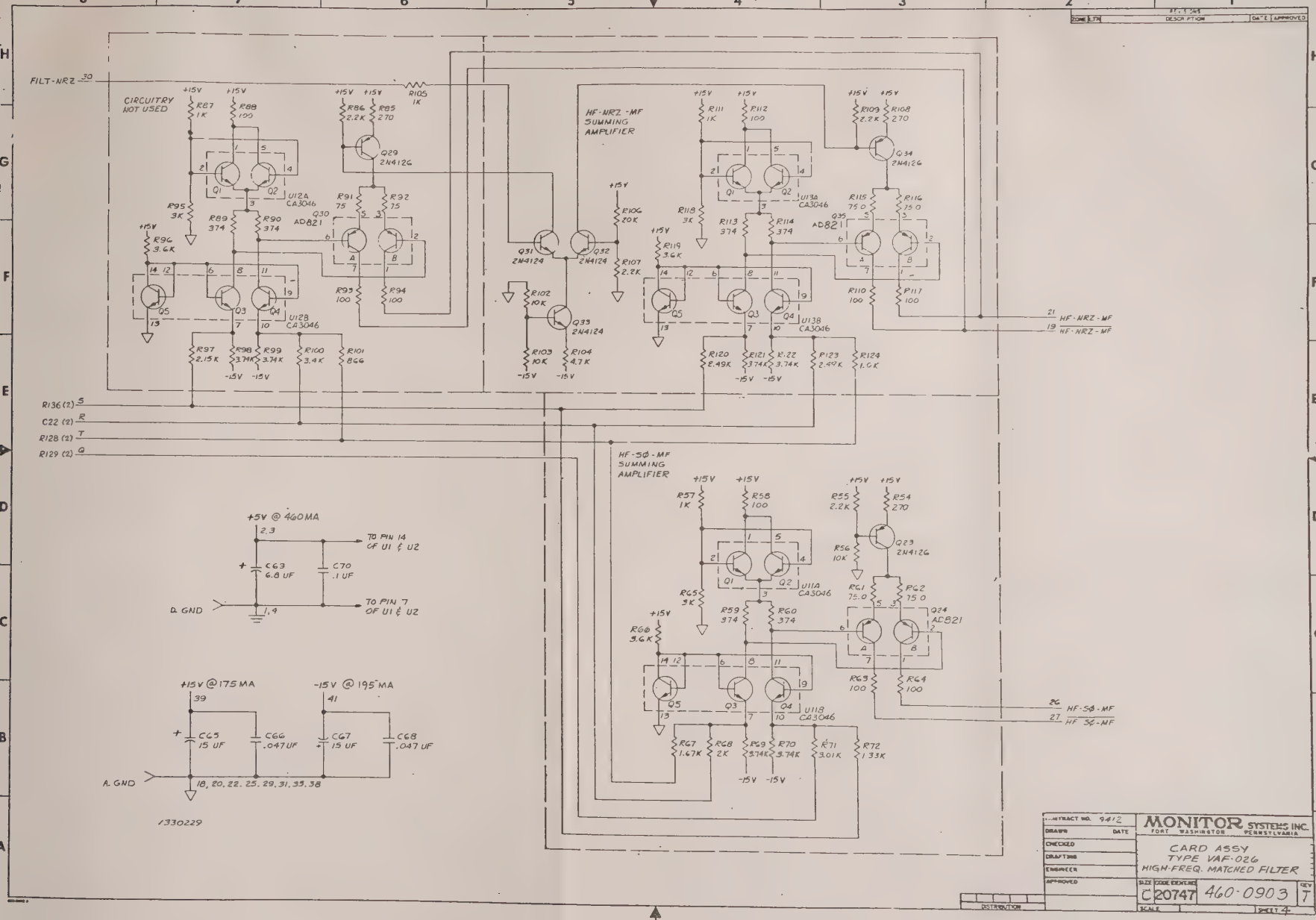
SIZE D | CODE IDENT NO. 20747 | 460-0903-501 502 | REV W

SCALE 2:1 | SHEET 1 OF 4

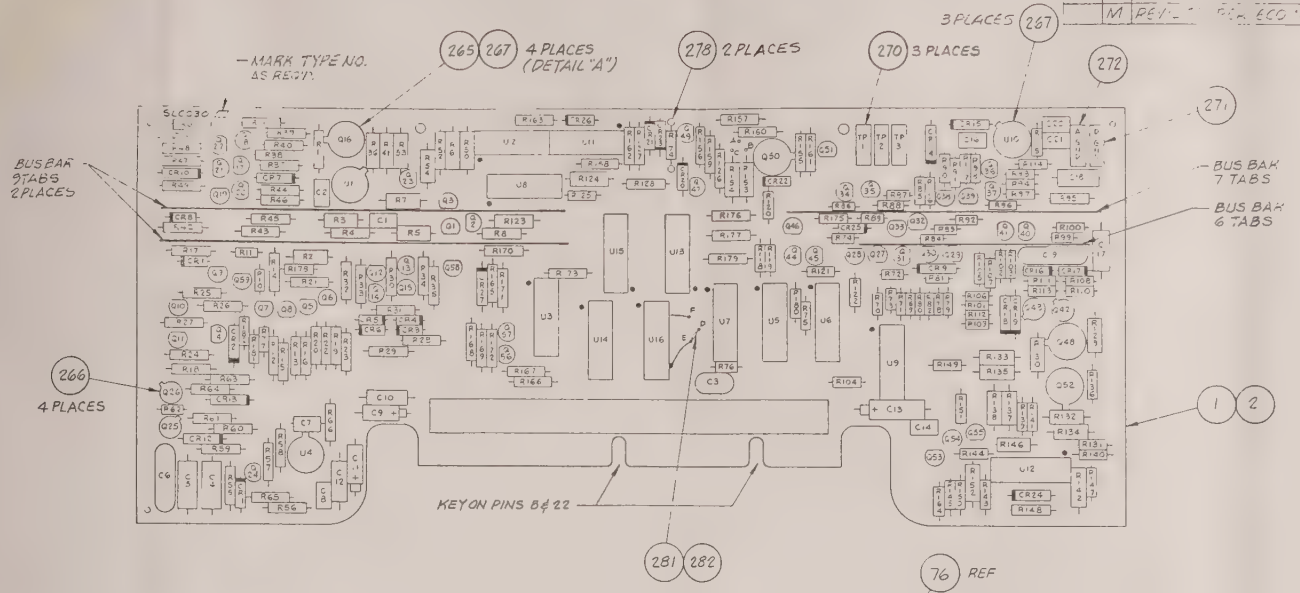
800-0684-1

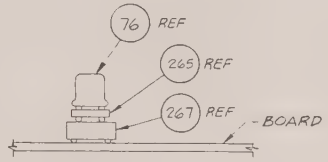

CAPACITOR DECADE CONTROL
R TO Q FEEDBACK CAPACITOR BANKS
BUFFER AMPLIFIER
LINE RECEIVER
Q FILTER
R FILTER
T TO S FEEDBACK CAPACITOR BANKS
BYPASS CAPACITOR BANKS
S FILTER
T FILTER
NOTES:
1 UNLESS OTHERWISE SPECIFIED;
ALL RESISTERS ARE IN OHMS
ALL CAPACITORS ARE IN PF.
2 MATCHED SET 300-0071-502 INCLUDES RAYSISTOR AND TWO ASSOCIATED RESISTORS. RESISTORS ARE IDENTIFIED AS LOW SBT AND HIGH SBT MATCHED SET ARE AS FOLLOWS
RAYSISTOR | HIGH SBT | LOW SBT
Z1 | R33 | R36
Z2 | R39 | R42
Z3 | R75 | R78
Z4 | R81 | R84
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
TYPE VAF-026
HIGH-FREQ. MATCHED FILTER
C 20747 460-0903
1330229


Q-RAYSISTOR DRIVER
R-RAYSISTOR DRIVER
RAYSISTOR CONTROL CIRCUIT
S-RAYSISTOR DRIVER
T-RAYSISTOR DRIVER
MSD8
MSD4
VD1
-6.2V DAC REF VOLTAGE
HEAT SINK
+2V TO PIN 6 OF Z1, Z2, Z3 AND Z4)
1330229
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
TYPE VAF-026
HIGH-FREQ MATCHED FILTER
C 20747 460-0903
SCALE ~ 1 9412 SHEET 3


FILT-NRZ
CIRCUITRY NOT USED
HF-NRZ-MF SUMMING AMPLIFIER
HF-5Ø-MF SUMMING AMPLIFIER
+15V @ 460MA
TO PIN 14 OF U1 & U2
D. GND
TO PIN 7 OF U1 & U2
+15V @ 175 MA
-15V @ 195 MA
A. GND
18, 20, 22, 25, 29, 31, 33, 38
1330229
R136 (2)
C22 (2)
R128 (2)
R129 (2)
HF-NRZ-MF
HF-5Ø-MF
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSY
TYPE VAF-026
HIGH-FREQ. MATCHED FILTER
C20747
460-0903
REV 7
SHEET 4

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
		B TO [illegible]		
	M	REV [illegible] ECO 104459 JSG		





DETAIL "A"
(NO SCALE)

NOTES:-

1. FOR GENERAL ENGINEERING & MANUFACTURING NOTES SEE DWG 401-0010.

FOR PARTS LIST SEE PL 460-0927-□

QTY	ITEM	FSCM	MONITOR P/N	MFR P/N	DESCRIPTION	NOTES
001						

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND APPLY BEFORE FINISH
SURFACE ROUGHNESS 125√
TOLERANCE ON
FRACTIONS ± 1/64 | DECIMALS ± .XX=.02 .XXX=.005 | ANGLES ± 1/2°

MATERIAL

FINISH

DRAWN	J. HARTZELL	DATE 3-15-72
CHECKED	J. GOODOLF	7-14-72
DRAFTING	J SAMPEDRO	12-6-72
ENGINEER	R. WASSERMAN	12-6-72
MFG		
APPROVED	R. CLEGG	12-7-72

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 18034

CARD ASSEMBLY
TYPE SLC030-1-2
SIGNAL LEVEL CONTROL BD#2

SIZE	CODE IDENT NO.		REV
C	20747	460-0927 -501 -502	M

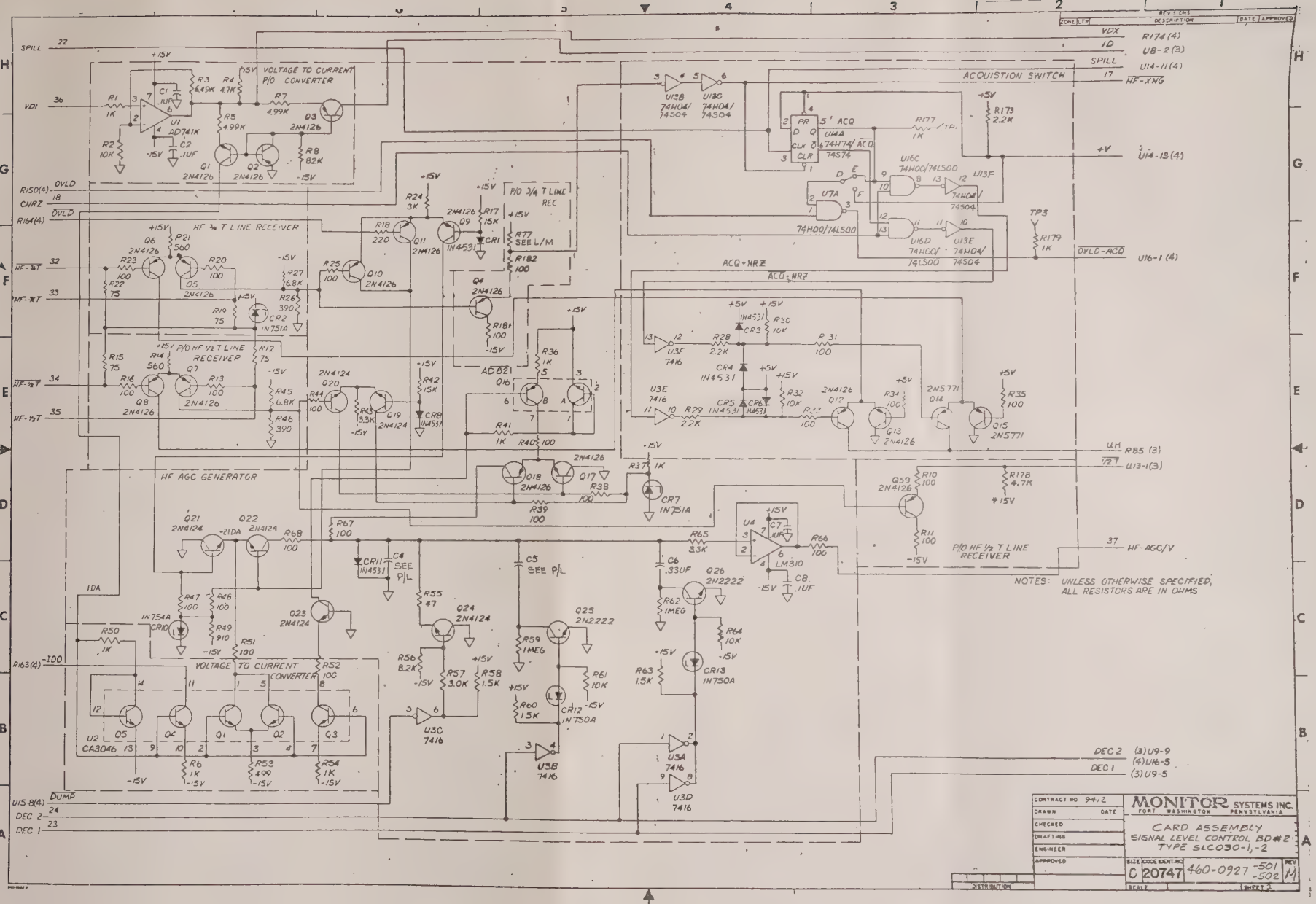
SCALE 2:1 SHEET 1 OF 4

MONITOR SHOP STANDARDS ARE AN INTEGRAL PART OF THIS DRAWING (296-0077)

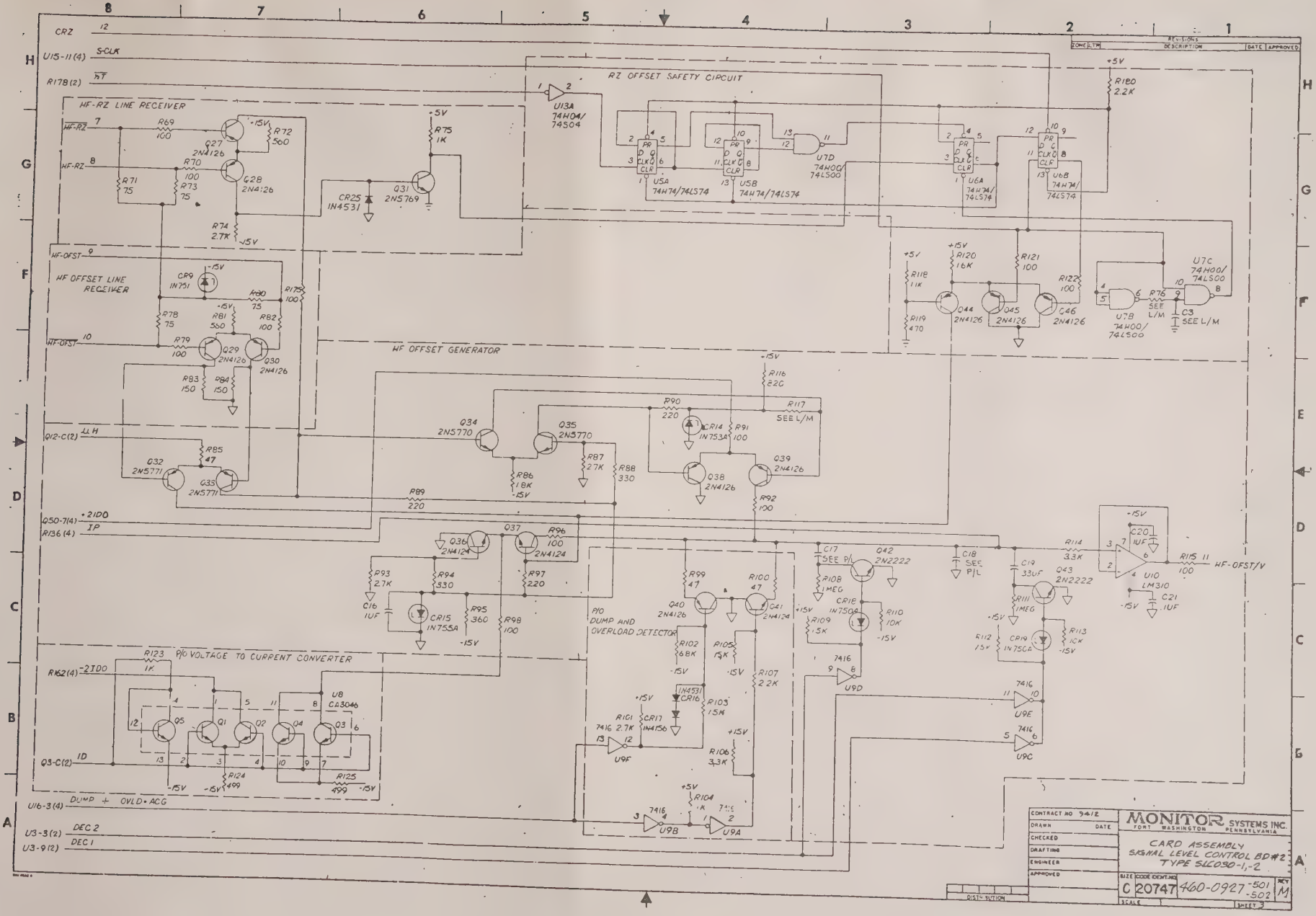
NEXT ASSY	USED ON
	9412

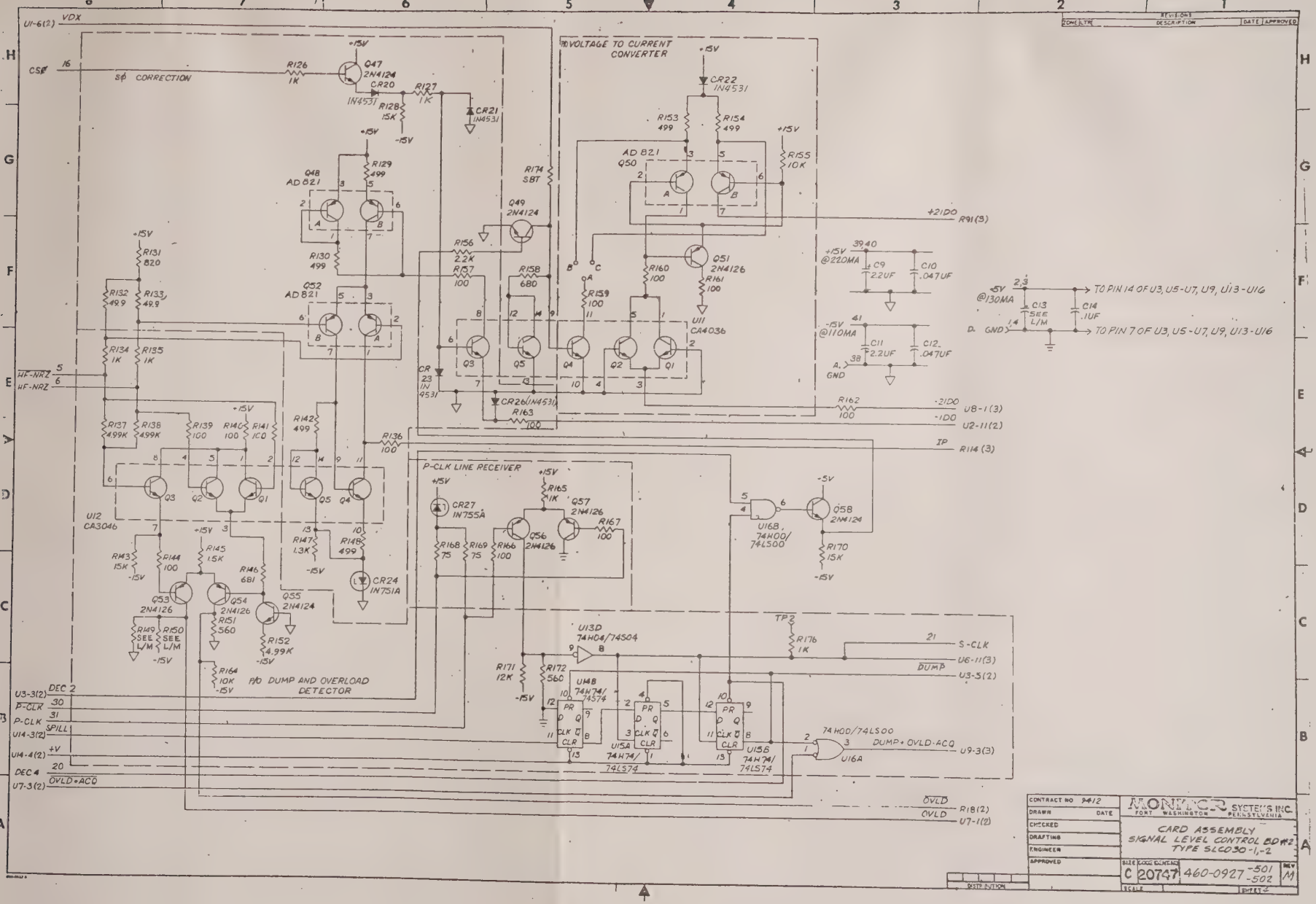
APPLICATION

800-0187C



VOLTAGE TO CURRENT P/O CONVERTER
HF ¾ T LINE RECEIVER
P/O HF ½ T LINE RECEIVER
HF AGC GENERATOR
VOLTAGE TO CURRENT CONVERTER
ACQUISTION SWITCH
P/O 3/4 T LINE REC
P/O HF ½ T LINE RECEIVER
NOTES: UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
SIGNAL LEVEL CONTROL BD#2
TYPE SLC030-1,-2
CONTRACT NO 94-12
SIZE C
CODE IDENT NO 20747
460-0927 -501 -502
REV M
SCALE
SHEET 2


HF-RZ LINE RECEIVER
RZ OFFSET SAFETY CIRCUIT
HF OFFSET LINE RECEIVER
HF OFFSET GENERATOR
P/O VOLTAGE TO CURRENT CONVERTER
P/O DUMP AND OVERLOAD DETECTOR
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
SIGNAL LEVEL CONTROL BD#2
TYPE SLC030-1,-2
460-0927-501
460-0927-502



VOLTAGE TO CURRENT CONVERTER
SØ CORRECTION
P-CLK LINE RECEIVER
P/O DUMP AND OVERLOAD DETECTOR
TO PIN 14 OF U3, U5-U7, U9, U13-U16
TO PIN 7 OF U3, U5-U7, U9, U13-U16
CONTRACT NO 9412
DRAWN
DATE
CHECKED
DRAFTING
ENGINEER
APPROVED
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
SIGNAL LEVEL CONTROL BD#2
TYPE SLC030-1,-2
SIZE C
CODE IDENT 20747
460-0927 -501 -502
REV M
SCALE
SHEET 2

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-0927 B		2-6-73	F. HINKLE
C	REVISED PER ECO 460-0927 C		6-27-73	F. HINKLE
D	REVISED PER ECO 460-0927 D		7-15-74	B. BICKEL
E	REVISED PER ECO 00772		5-14-75	J. RONEY
F	REVISED PER ECO 00808		7-12-75	J. NEWBY
G	REVISED PER ECO 02082		7-18-77	J. MATHER
H	REVISED PER ECO 02254		4-4-78	
J	REVISED PER ECO 03441		7/21/78	R. Wasserman
K	REVISED PER ECO 03687 BAKER 11-6-78		11/6/78	R Wasserman
L	REVISED PER ECO 04061 BAKER 4-27-79		4/30/79	DR Kennedy
M	REVISED PER ECO 04459 JSG		9-25-79	J Hinkle
N	REVISED PER ECO 05520 TJG 7.2.80		15JUL80	RS Vol 2
P	REVISED PER ECO 05868 JSG		6JAN81	RS Vol 2
R	REVISED PER ECO 06742 CMT 16OCT81		19OCT81	RS Vol 2

NOTE 2: THE FOLLOWING NUMBERS ARE NOT USED: R9

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	R	N	M	M	P	M	M	M	M	M	M	M	M	M									

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE CARD ASSEMBLY
TYPE SLC030-1,-2
SIGNAL LEVEL CONTROL BD #2

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	J. HARTZELL		ENGINEER	R. WASSERMAN		DWG NO. PL 501 460-0927-502 REV R
CHECKED	J. GOODOLF		APPROVED	R. CLEGG	12-7-72	
DRAFTING	J. SAMPEDRO					SHEET 1 OF 14

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	1		400-1121	——	20747	BOARD, PRINTED WIRING	
		1	1	2	A	108-203-041	7022-041-000-001	91662	CONN, FINGER BLOCK	
				3						
				4						
				5						
				6						
				7						
				8						
				9						
				10						
				11						
				12						
				13						
				14						
				15						
				16						
		8	8	17	A	102-419-104	CY30A10M	71590	CAP, .1UF, 100V, 20%	C1, C2, C7, C8, C14, C16, C20, C21
				18						
				19						
				20						
				21						
				22						

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		CARD ASSEMBLY TYPE SLC030-1,-2	20747	PL 460-0927-☐	N
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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		–	1	23	A	102-109-201	DM10CD201J04CR	72136	CAP, 200PF, 500V, 5%	C3
		1	–	24	A	102-109-101	DM10CD101J04CR	72136	CAP, 100PF, 500V, 5%	C3
				25						
				26						
				27						
				28						
		–	2	29	A	102-001-332	230B1E332	14752	CAP, .0033UF, 100V, 20%	C4, C18
		–	2	30	A	102-001-333	230B1B333	14752	CAP, .033UF, 100V, 20%	C5, C17
		2	2	31	A	102-016-334	X663FR3349.5W18	84411	CAP, .33UF, 50V, 10%	C6, C19
		2	2	32	A	102-305-225	150D225X0020A2	56289	CAP, 2.2UF, 20V, 20%	C9, C11
		2	2	33	A	102-001-473	230B1B473	14752	CAP, .047UF, 100V, 20%	C10, C12
		2	–	34	A	102-003-682	230B1E682	14752	CAP, .0068 UF, 100V, 20%	C4, C18
		2	–	35	A	102-001-683	230B1E683	14752	CAP, .068 UF, 100V, 10%	C5, C17
				36						
				37						
		–	1	38	A	102-313-685	150D685X0006A2	56289	CAP, 6.8UF, 6V, 20%	C13
		1	–	39	A	102-306-475	150D475X0010A2	56289	CAP, 4.7UF, 10V, 20%	C13
				40						
				41						
				42						
				43						
				44						

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		CARD ASSEMBLY TYPE SLC030-1,-2	20747	PL 460-0927-□ SHEET 3 OF	M

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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		14	14	45	A	104-503-014	IN4531	01295	DIODE	CR1, CR3-CR5, CR6, CR8, CR11, CR16, CR20-CR23, CR25, CR26
				46						
				47						
				48						
				49						
				50						
		4	4	51	A	104-056-106	IN751A	04713	DIODE, ZENER, 5.1V, 5%	CR2, CR7, CR9, CR24
				52						
				53						
		1	1	54	A	104-056-113	IN754A	04713	DIODE, ZENER, 6.8V, 5%	CR10
				55						
				56						
		4	4	57	A	104-056-112	IN750A	04713	DIODE, ZENER, 4.7V, 5%	CR12, CR13, CR18, CR19
				58						
				59						
		1	1	60	A	104-056-105	IN753A	04713	DIODE, ZENER, 6.2V, 5%	CR14
		2	2	61	A	104-056-110	IN755A	04713	DIODE, ZENER, 7.5V, 5%	CR15, CR27
		1	1	62	A	104-060-009	IN4156	03508	DIODE, MULTI-JUNCTION	CR17
				63						
				64						
				65						
				66						

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		CARD ASSEMBLY TYPE SI C030-1,-2	20747	PL 460-0927-☐	M
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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		31	31	67	A	103-304-001	2N4126	04713	TRANS., PNP	Q1-Q13, Q17, Q18, Q27-Q30, Q38-Q40, Q44-Q46, Q51, Q53 Q54, Q56, Q57, Q59
				68						
				69						
				70						
				71						
				72						
		4	4	73	A	103-438-001	2N5771	07263	TRANS., PNP	Q14, Q15, Q32, Q33
				74						
				75						
		4	4	76	A	103-647-008	AD821	24355	TRANS., DUAL PNP	Q16, Q48, Q50, Q52
				77						
				78						
		13	13	79	A	103-408-001	2N4124	04713	TRANS, NPN	Q19-Q24, Q36, Q37, Q41, Q47, Q49, Q55, Q58
				80						
				81						
				82						
		4	4	83	A	103-019-001	2N2222	04713	TRANS., NPN	Q25, Q26, Q42, Q43
		1	1	84	A	103-440-001	2N5769	07263	TRANS., NPN	Q31
		2	2	85	A	103-437-001	2N5770	07263	TRANS., NPN	Q34, Q35
				86						
				87						
				88						

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		CARD ASSEMBLY TYPE SLC030-1,-2	20747	PL 460-0927-□ SHEET 5 OF	P

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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		8	8	89	A	100-003-102	RC07GF102J	81349	RES., 1K, 1/4W, 5%	R1, R37, R126, R127, R165, R176, R177, R179
				90						
				91						
				92						
		1	1	93	A	100-215-1002	RN55D1002F	81349	RES, 10K, 1/10W, 1%	R2
		1	1	94	A	100-215-6491	RN55D6491F	81349	RES, 6.49K, 1/10W, 1%	R3
		1	1	95	A	100-003-472	RC07GF472J	81349	RES, 4.7K, 1/4W, 5%	R4
				96						
				97						
		5	5	98	A	100-215-4991	RN55D4991F	81349	RES, 4.99K, 1/10W, 1%	R5, R7, R137, R138, R152
				99						
				100						
		8	8	101	A	100-215-1001	RN55D1001F	81349	RES, 1K, 1/10W, 1%	R6, R36, R41, R50, R54, R123, R134, R135
				102						
				103						
				104						
		1	1	105	A	100-003-823	RC07GF823J	81349	RES, 82K, 1/4W, 5%	R8
				106						
				107						
				108						
				109						
				110						

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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		21	21	111	A	100-017-101	RC05GF101J	81349	RES, 100Ω, 1/8W, 5%	R10, R11, R69, R70, R79, R82, R91, R92, R96, R98, R115, R121, R122, R136, R139-R141, R144, R175, R181, R182
				112						
				113						
				114						
				115						
				116						
		6	6	117	A	100-003-750	RC07GF750J	81349	RES, 75Ω, 1/4W, 5%	R12, R15, R19, R22, R168, R169
				118						
				119						
				120						
				121						
		28	28	122	A	100-003-101	RC07GF101J	81349	RES, 100Ω, 1/4W, 5%	R13, R16, R20, R23, R25, R31, R33-R35, R38-R40, R44, R47 R48, R51, R52, R66-R68, R157, R159-R163 R166, R167
				123						
				124						
				125						
				126						
		3	3	127	A	100-003-561	RC07GF561J	81349	RES, 560Ω, 1/4W, 5%	R14, R21, R172
		4	4	128	A	100-003-153	RC07GF153J	81349	RES, 15K, 1/4W, 5%	R17, R42, R128, R170
				129						
				130						
				131						
				132						

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		CARD ASSEMBLY TYPE SLC030-1,-2	20747	PL 460-0927-☐ SHEET 7 OF	M

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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	133	A	100-003-221	RC07GF221J	81349	RES, 220Ω, ¼W, 5%	R18
		2	2	134	A	100-003-302	RC07GF302J	81349	RES, 3K, ¼W, 5%	R24, R57
		2	2	135	A	100-003-391	RC07GF391J	81349	RES, 390Ω, ¼W, 5%	R26, R46
				136						
				137						
		2	2	138	A	100-003-682	RC07GF682J	81349	RES, 6.8K, ¼W, 5%	R27, R45
		4	4	139	A	100-003-222	RC07GF222J	81349	RES, 2.2K, ¼W, 5%	R28, R29, R156, R173
				140						
				141						
		5	5	142	A	100-003-103	RC07GF103J	81349	RES, 10K, ¼W, 5%	R30, R32, R61, R64, R155
		2	2	143	A	100-003-332	RC07GF332J	81349	RES, 3.3K, ¼W, 5%	R43, R65
		1	1	144	A	100-003-911	RC07GF911J	81349	RES, 910Ω, ¼W, 5%	R49
				145						
				146						
		8	8	147	A	100-215-4990	RN55D4990F	81349	RES, 499Ω, 1/10W, 1%	R53, R124, R129, R130, R142, R148, R153, R154
				148						
				149						
				150						
		1	1	151	A	100-003-470	RC07GF470J	81349	RES, 47Ω, ¼W, 5%	R55
		1	1	152	A	100-003-822	RC07GF822J	81349	RES, 8.2K, ¼W, 5%	R56
				153						
				154						

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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
				155						
		3	3	156	A	100-003-152	RC07GF152J	81349	RES, 1.5K, 1/4W, 5%	R58, R60, R63
		1	1	157	A	100-003-105	RC07GF105J	81349	RES, 1MEG, 1/4W, 5%	R59
		3	3	158	A	100-017-105	RC05GF105J	81349	RES, 1MEG, 1/8W, 5%	R62, R108, R111
				159						
				160						
				161						
				162						
		4	4	163	A	100-017-750	RC05GF750J	81349	RES, 75Ω, 1/8W, 5%	R71, R73, R78, R80
		3	3	164	A	100-017-561	RC05GF561J	81349	RES, 560Ω, 1/8W, 5%	R72, R81, R151
		4	4	165	A	100-017-272	RC05GF272J	81349	RES, 2.7K, 1/8W, 5%	R74, R87, R93, R101
		2	2	166	A	100-017-102	RC05GF102J	81349	RES, 1K, 1/8W, 5%	R75, R104
				167						
				168						
		-	1	169	A	100-017-201	RC05GF201J	81349	RES, 200Ω, 1/8W, 5%	R76
		1	-	170	A	100-017-391	RC05GF391J	81349	RES, 390Ω, 1/8W, 5%	R76
				171						
		-	4	172	A	100-017-103	RC05GF103J	81349	RES, 10K, 1/8W, 5%	R77, R110, R113, R164
		2	-	173	A	100-017-472	RC05GF472J	81349	RES, 4.7K, 1/8W, 5%	R77, R178
				174						
				175						
				176						

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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		2	2	177	A	100-017-151	RC05GF151J	81349	RES, 150Ω, 1/8W, 5%	R83, R84
		3	3	178	A	100-017-470	RC05GF470J	81349	RES, 47Ω, 1/8W, 5%	R85, R99, R100
		1	1	179	A	100-017-182	RC05GF182J	81349	RES, 1.8K, 1/8W, 5%	R86
		2	2	180	A	100-017-331	RC05GF331J	81349	RES, 330Ω, 1/8W, 5%	R88, R94
				181						
				182						
		3	3	183	A	100-017-221	RC05GF221J	81349	RES, 220Ω, 1/8W, 5%	R89, R90, R97
		1	1	184	A	100-003-361	RC07GF361J	81349	RES, 360Ω, 1/4W, 5%	R95
		1	1	185	A	100-017-682	RC05GF682J	81349	RES, 6.8K, 1/8W, 5%	R102
		4	4	186	A	100-017-152	RC05GF152J	81349	RES, 1.5K, 1/8W, 5%	R103, R109, R112, R145
				187						
				188						
				189						
				190						
		2	2	191	A	100-017-153	RC05GF153J	81349	RES, 15K, 1/8W, 5%	R105, R143
		2	2	192	A	100-017-332	RC05GF332J	81349	RES, 3.3K, 1/8W, 5%	R106, R114
		2	2	193	A	100-017-222	RC05G222J	81349	RES, 2.2K, 1/8W, 5%	R107, R180
		3	–	194	A	100-017-103	RC05G103J	81349	RES, 10K, 1/8W, 5%	R110, R113, R164
				195						
				196						
				197						
				198						

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		CARD ASSEMBLY TYPE SLC030-1,-2	20747	PL 460-0927-☐ SHEET 10 OF	M

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QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		2	2	199	A	100-017-821	RC05GF821J	81349	RES, 820Ω, 1/8W, 5%	R116, R131
				200						
				201						
		-	1	202	A	100-017-391	RC05GF391J	81349	RES, 390Ω, 1/8W, 5%	R117
		1	-	203	A	100-017-241	RC05GF241J	81349	RES, 240Ω, 1/8W, 5%	R117
				204						
				205						
		1	1	206	A	100-017-112	RC05GF112J	81349	RES, 1.1K, 1/8W, 5%	R118
		1	1	207	A	100-017-471	RC05GF471J	81349	RES, 470Ω, 1/8W, 5%	R119
		1	1	208	A	100-017-162	RC05GF162J	81349	RES, 1.6K, 1/8W, 5%	R120
		1	1	209	A	100-222-4990	RN50C4990F	81349	RES, 499Ω, 1/20W, 1%	R125
				210						
				211						
				212						
				213						
		2	2	214	A	100-215-49R9	RN55D49R9F	81349	RES, 49.9Ω, 1/10W, 1%	R132, R133
		1	1	215	A	100-215-6810	RN55D6810F	81349	RES, 681Ω, 1/10W, 1%	R146
		1	1	216	A	100-017-132	RC05GF132J	81349	RES, 1.3Ω, 1/8W, 5%	R147
				217						
				218						
				219						
				220						

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		CARD ASSEMBLY TYPE SLC030-1,-2	20747	PL 460-0927-□ SHEET 11 OF	M

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		-	1	221	A	100-017-911	RC05GF911J	81349	RES, 910Ω, 1/8W, 5%	R149
		1	-	222	A	100-017-681	RC05GF681J	81349	RES, 680Ω, 1/8W, 5%	R149
				223						
				224						
				225						
				226						
		-	1	227	A	100-017-113	RC05GF113J	81349	RES, 11K, 1/8W, 5%	R150
		1	-	228	A	100-017-683	RC05GF683J	81349	RES, 68K, 1/8W, 5%	R150
				229						
				230						
				231						
				232						
		1	1	233	A	100-003-681	RC07GF681J	81349	RES, 680Ω, 1/4W, 5%	R158
		1	1	234	A	100-003-123	RC07GF123J	81349	RES, 12K, 1/4W, 5%	R171
		1	1	235	A	100-003-SBT	RC07GFSBTJ	81349	RES, SBT, 1/4W, 5%	R174
		-	1	236	A	100-017-472	RC05GF472J	81349	RES, 4.7K, 1/8W, 5%	R178
				237						
				238						
				239						
				240						
				241						
				242						

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TITLE CARD ASSEMBLY
TYPE SI C030-1,-2

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AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	243	A	139-141-001	AD741KH	24355	I.C., OP AMP	U1
		4	4	244	A	139-209-002	CA3046	02735	I.C., NPN TRANS. ARRAY	U2, U8, U11, U12
		2	2	245	A	139-046-416	SN7416N-10	01295	I.C., TTL HEX INVERTER	U3, U9
		2	2	246	A	139-144-001	LM310H	27014	I.C., AMP	U4, U10
				247						
				248						
		-	4	249	A	139-051-474	SN74H74N-10	01295	I.C., TTL DUAL D FLIP-FLOP	U5, U6, U14, U15
		3	-	250	A	139-198-474	SN74LS74N	01295	I.C., TTL DUAL D FLIP-FLOP	U5, U6, U15
				251						
				252						
		-	2	253	A	139-051-400	SN74H00N-10	01295	I.C., TTL QUAD NAND GATE	U7, U16
		2	-	254	A	139-198-400	SN74LS00	01295	I.C., TTL QUAD NAND GATE	U7, U16
				255						
				256						
		-	1	257	A	139-051-404	SN74H04N-10	01295	I.C., TTL HEX INVERTER	U13
		1	-	258	A	139-152-404	SN74S04N-10	01295	I.C., TTL HEX INVERTER	U13
				259						
				260						
		1	-	261	A	139-152-474	SN74S74N-10	01295	I.C., TTL DUAL D FLIP-FLOP	U14
				262						
				263						
				264						

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QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		4	4	265	A	131-049-001	RC-T018100-2A	19080	PAD, INSULATOR	USE WITH ITEM 76
		4	4	266	A	131-013-001	10047	07047	PAD, INSULATOR	USE WITH ITEM 83
		7	7	267	A	131-017-001	10383	07047	PAD, INSULATOR	USE WITH ITEMS 76, 243, 246
				268						
				269						
		3	3	270	A	121-202-005	8041-1G7	91506	TEST JACK, GREEN	TP1 - TP3
		1	1	271	A	121-202-010	8041-1G6	91506	TEST JACK, BLACK	D GND
		1	1	272	A	121-202-009	8041-1G9	91506	TEST JACK, WHITE	A. GND
				273						
				274						
		2	2	275	B	217-0312-001	——	20747	BUS BAR, 9 TABS	
		1	1	276	B	217-0312-001	——	20747	BUS BAR, 7 TABS	
		1	1	277	B	217-0312-001	——	20747	BUS BAR, 6 TABS	
		2	2	278	A	118-005-003	1604-2-05	71279	TERMINAL, TURRET	
				279						
				280						
		1/2"	1/2"	281	A	113-001-006	299/1	92194	WIRE, BUS #26 AWG	
		1/4"	1/4"	282	A	114-001-006	——	03890	TUBING, TEFLON, #26	
				283						
				284						
		AR	AR	285	A	120-101-001	SN63BS	81348	SOLDER, QQ-S-571	
				286						

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		CARD ASSEMBLY TYPE SLC030-1,-2	20747	PL460-0927-☐ SHEET 14 OF	M

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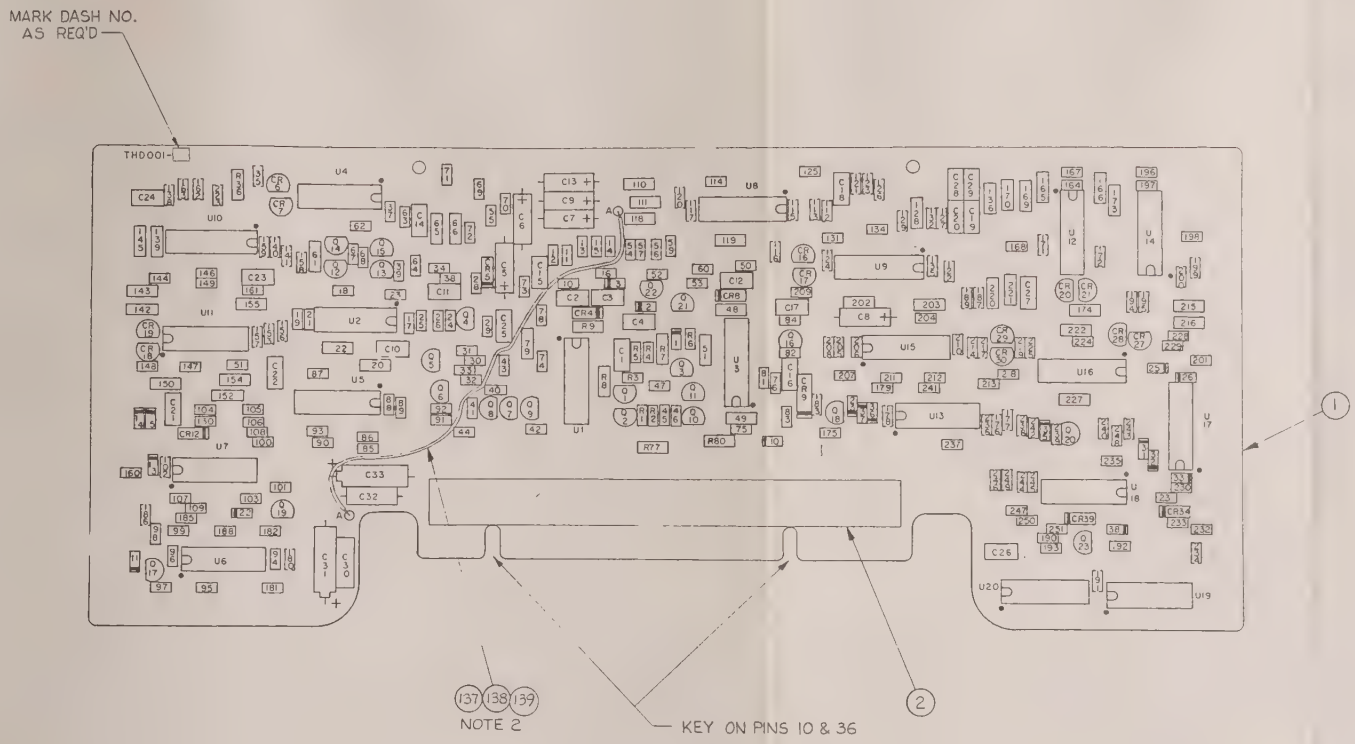
ZONE	LTR	REVISIONS DESCRIPTION		DATE	APPROVED
		"B" TO "L" SEE P/L FOR ECO NO.			
	M	REVISED PER ECO # 04459	J.S.G.	9-25-79	F. HINKLE
	N	REVISED PER ECO # 07095	WKH 1-17-82	1-22-82	ES
	P	REVISED PER ECO # 08082	JSG	1 Jun 72	RSVJ2



NOTES:

1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DRAWING NO. 401-0010.
2. INSTALL JUMPER FROM "A" TO "A" AS SHOWN FOR -503 ASSY. ONLY.

FOR PARTS LIST SEE PL 460-0906-▱

DRAWN	J. HARTZELL DATE 1-6-72
CHECKED	R. OLIVIERI 4-26-72
DRAFTING	J. SAMPEDRO 10-12-72
ENGINEER	R. WASSERMAN 8-1-72
MFG	R. HELLER 10-16-72
APPROVED	R. CLEGG 10-25-72
APPROVED	

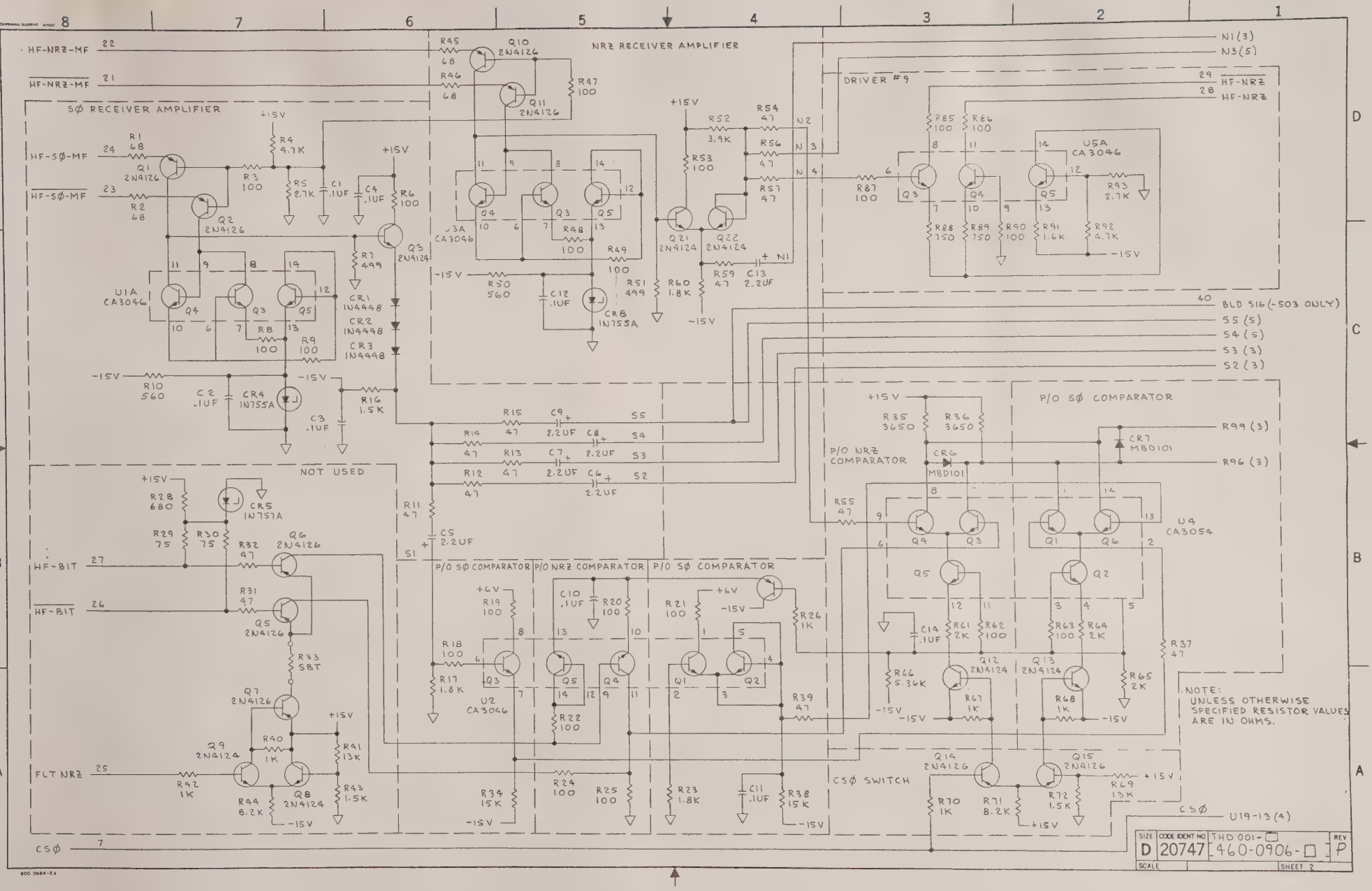
AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA 19034

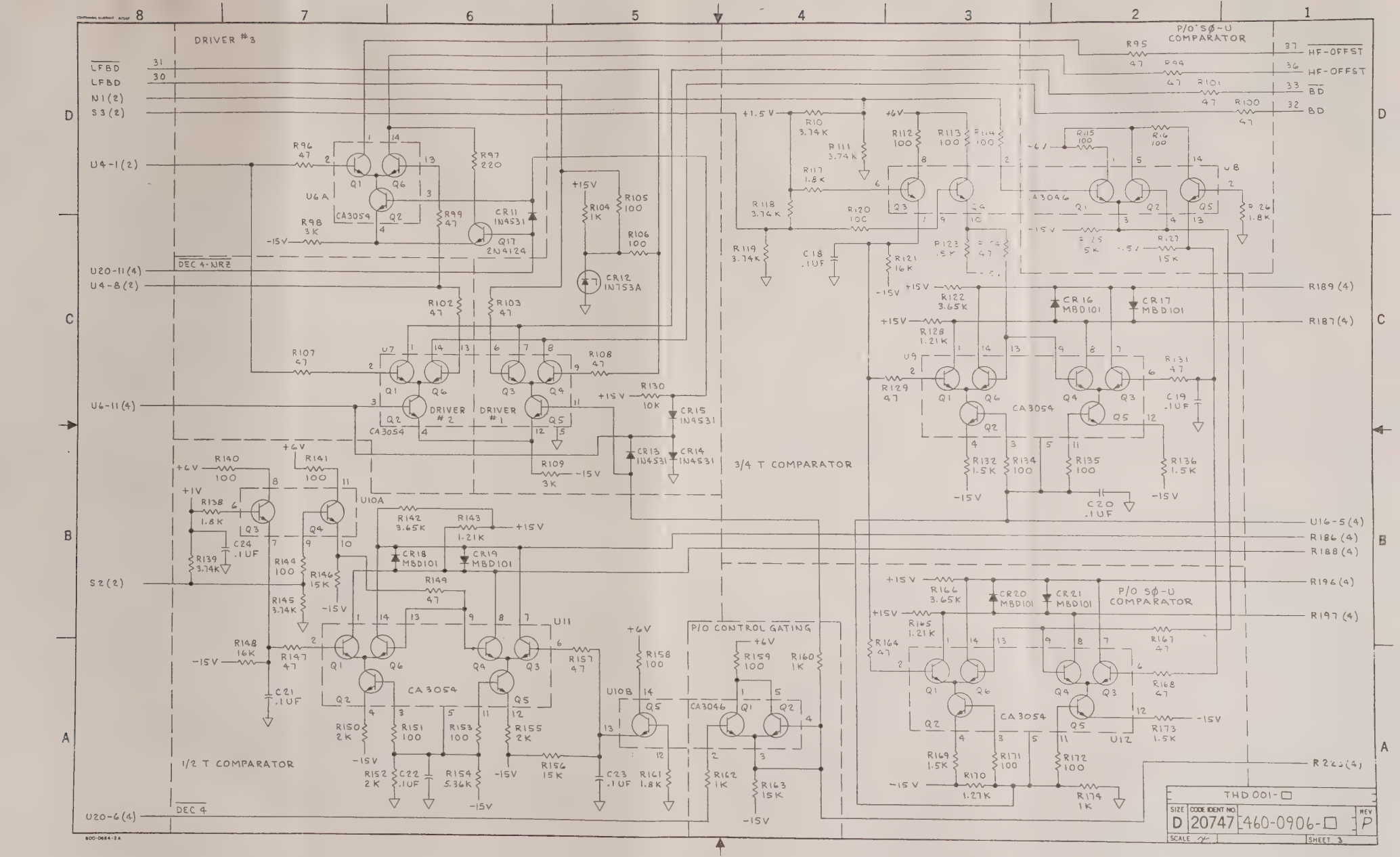
CARD ASSEMBLY
THRESHOLD DETECTORS
THD001-□

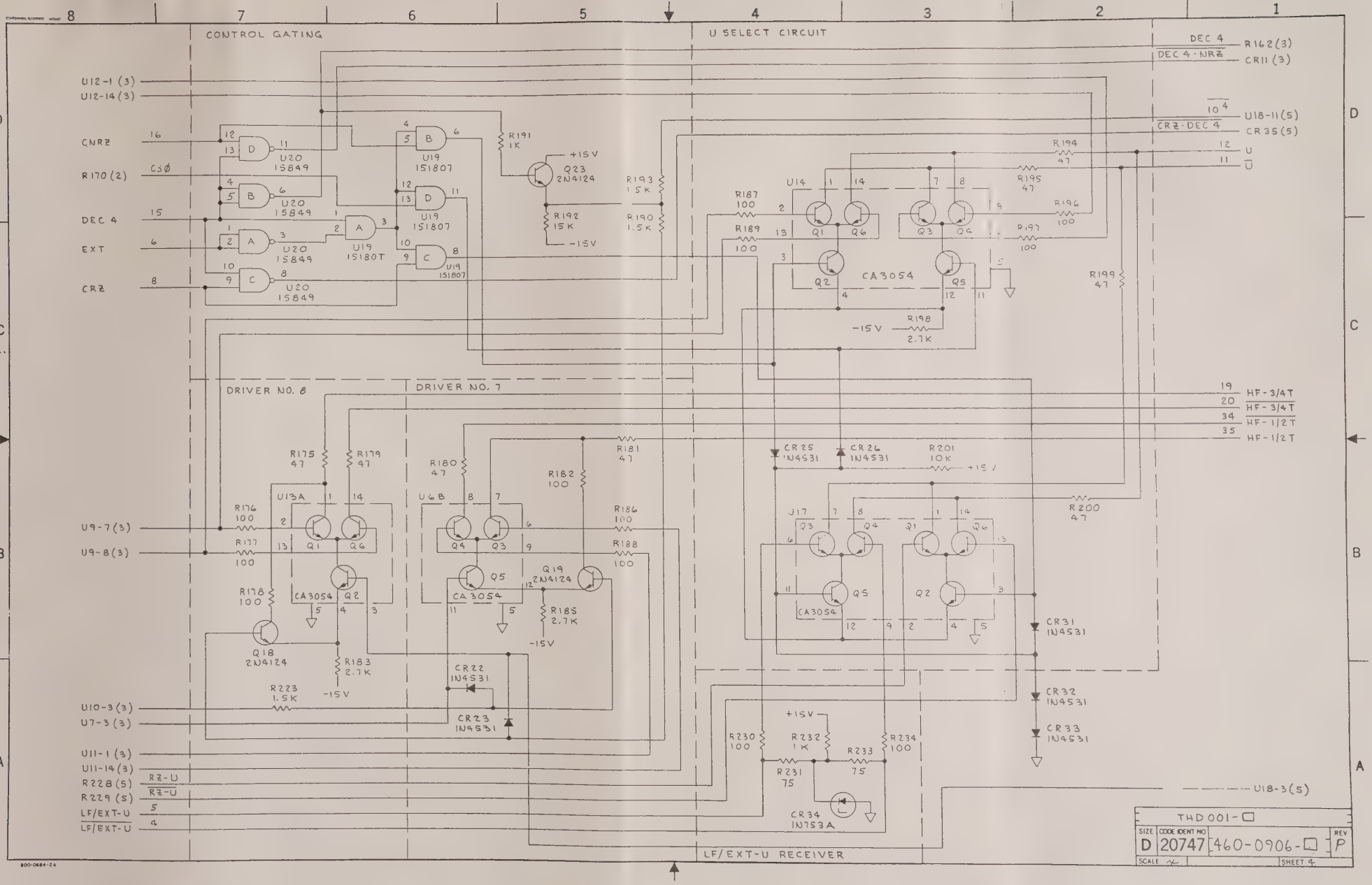
NEXT ASSY	USED ON
	9412
APPLICATION	

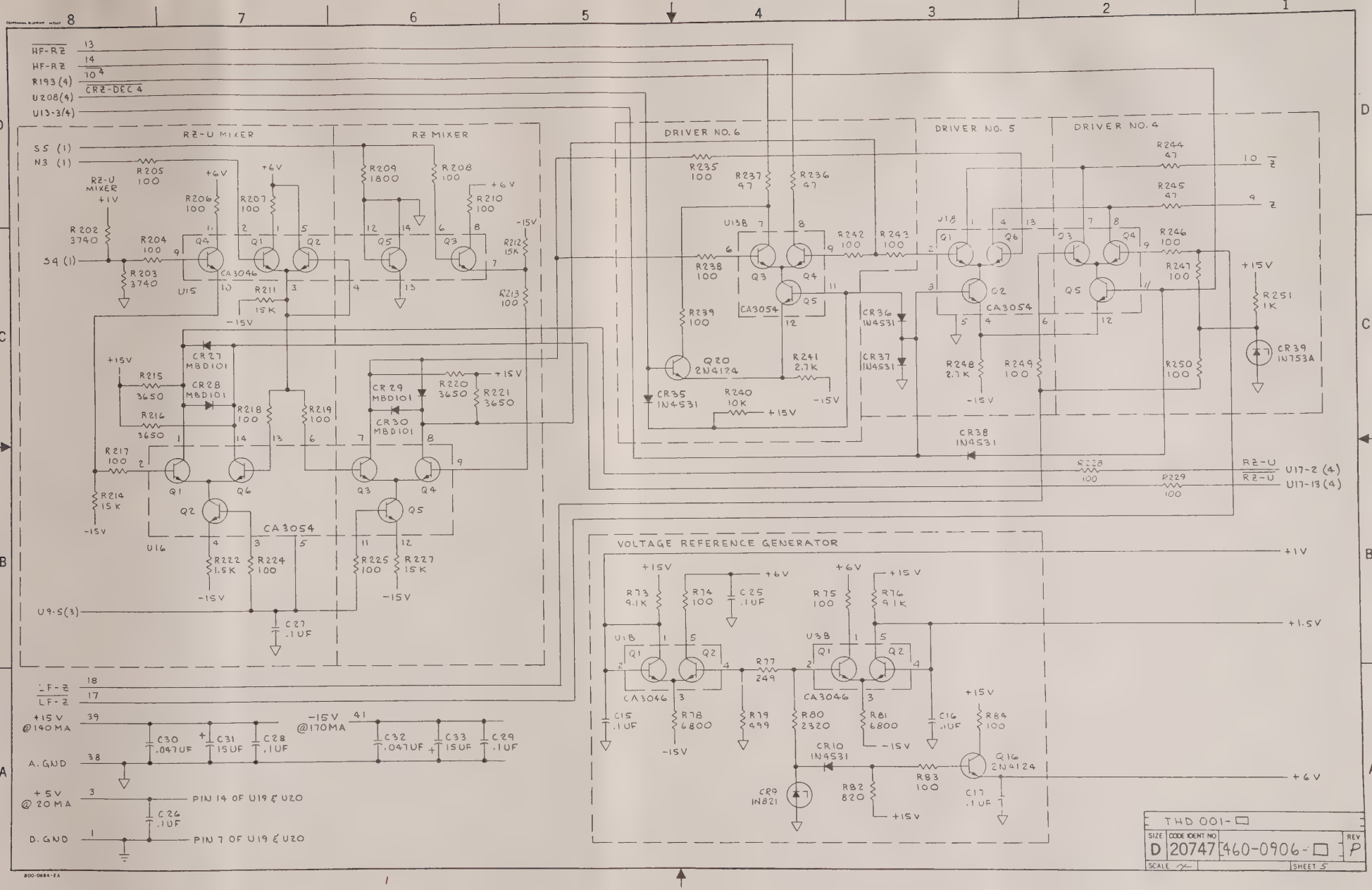
SIZE	CODE IDENT NO.		REV
D	20747	460-0906-□	P
SCALE 2/1		SHEET 1 OF 5	

600-C684 A


SØ RECEIVER AMPLIFIER
NRZ RECEIVER AMPLIFIER
DRIVER #9
NOT USED
P/O SØ COMPARATOR
P/O NRZ COMPARATOR
P/O SØ COMPARATOR
P/O SØ COMPARATOR
P/O NRZ COMPARATOR
P/O SØ COMPARATOR
CSØ SWITCH
HF-NRZ-MF
HF-SØ-MF
HF-BIT
FLT NRZ
CSØ
N1(3)
N3(5)
HF-NRZ
HF-NRZ
BLD S16(-503 ONLY)
S5 (5)
S4 (5)
S3 (3)
S2 (3)
R99 (3)
R96 (3)
CSØ U19-13 (4)
U1A CA3046
U2 CA3046
U3A CA3046
U4 CA3054
U5A CA3046
Q1 2N4126
Q2 2N4126
Q3 2N4126
Q4 2N4126
Q5 2N4126
Q6 2N4126
Q7 2N4126
Q8 2N4124
Q9 2N4124
Q10 2N4126
Q11 2N4126
Q12 2N4124
Q13 2N4124
Q14 2N4126
Q15 2N4126
Q21 2N4124
Q22 2N4124
CR1 IN4448
CR2 IN4448
CR3 IN4448
CR4 IN755A
CR5 IN757A
CR6 MBD101
CR7 MBD101
CR8 IN755A
+15V
-15V
+6V
NOTE:
UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS.
SIZE D
CODE IDENT NO 20747
THD 001-□
460-0906-□
REV P
SCALE
SHEET 2


DRIVER #3
LFBD
LFBD
N1(2)
S3(2)
U4-1(2)
U20-11(4)
U4-8(2)
U6-11(4)
S2(2)
U20-6(4)
DEC 4-NRZ
DEC 4
DRIVER #2
DRIVER #1
CA3054
CA3046
U6A
U7
U8
U9
U10A
U10B
U11
U12
Q17 2N4124
CR11 1N4531
CR12 1N753A
CR13 1N4531
CR14 1N4531
CR15 1N4531
CR16 MBD101
CR17 MBD101
CR18 MBD101
CR19 MBD101
CR20 MBD101
CR21 MBD101
3/4 T COMPARATOR
1/2 T COMPARATOR
P/O CONTROL GATING
P/O SØ-U COMPARATOR
HF-OFFST
HF-OFFST
BD
BD
R189(4)
R187(4)
U16-5(4)
R186(4)
R188(4)
R196(4)
R197(4)
R223(4)
THD 001-□
SIZE D
CODE IDENT NO. 20747
460-0906-□
REV P
SCALE
SHEET 3


CONTROL GATING
U SELECT CIRCUIT
DRIVER NO. 8
DRIVER NO. 7
LF/EXT-U RECEIVER
U12-1 (3)
U12-14 (3)
CNRZ
R170 (2)
CSØ
DEC 4
EXT
CRZ
U20 15849
U19 151807
U19 15180T
R191 1K
Q23 2N4124
R192 15K
R193 1.5K
R190 1.5K
+15V
-15V
DEC 4
DEC 4 · NRZ
R162(3)
CR11(3)
10 4
U18-11(5)
CRZ · DEC 4
CR35(5)
U
Ū
R194 47
R195 47
R196 100
R197 100
R187 100
R189 100
U14
Q1
Q6
Q3
Q4
Q2
Q5
CA3054
R198 2.7K
R199 47
R200 47
R201 10K
CR25 1N4531
CR26 1N4531
U17
CR31 1N4531
CR32 1N4531
CR33 1N4531
R230 100
R232 1K
R233 75
R234 100
R231 75
CR34 1N753A
U18-3(5)
19 HF-3/4T
20 HF-3/4T
34 HF-1/2T
35 HF-1/2T
U9-7(3)
U9-8(3)
R175 47
R179 47
R180 47
R181 47
R182 100
R176 100
R177 100
R186 100
R188 100
U13A
U6B
R178 100
Q18 2N4124
Q19 2N4124
R185 2.7K
R183 2.7K
R223 1.5K
CR22 1N4531
CR23 1N4531
U10-3(3)
U7-3(3)
U11-1(3)
U11-14(3)
R228(5) RZ-U
R229(5) RZ-U
LF/EXT-U 5
LF/EXT-U 4
THD 001-□
SIZE D
CODE IDENT NO 20747
460-0906-□
REV P
SCALE
SHEET 4
800-0684-2A


HF-RZ
HF-RZ
R193(4)
U208(4)
U13-3/4
CRZ-DEC 4
RZ-U MIXER
RZ MIXER
SS (1)
N3 (1)
S4 (1)
U15
CA3046
CA3054
U16
U9-5(3)
DRIVER NO. 6
DRIVER NO. 5
DRIVER NO. 4
Q20 2N4124
CR35 IN4531
CR36 IN4531
CR37 IN4531
CR38 IN4531
CR39 IN753A
RZ-U U17-2 (4)
RZ-U U17-13 (4)
VOLTAGE REFERENCE GENERATOR
+1V
+1.5V
+6V
CR9 IN821
CR10 IN4531
Q16 2N4124
LF-Z
LF-Z
+15V @140MA
-15V @170MA
A. GND
+5V @ 20MA
D. GND
PIN 14 OF U19 & U20
PIN 7 OF U19 & U20
THD 001-□
SIZE D
CODE IDENT NO 20747
460-0906-□
REV P
SCALE
SHEET 5

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISE. PER ECO 460-0906B		3-1-73	[illegible]
C	" 460-0906C		10-25-73	[illegible]
D	" 00807		6-11-75	[illegible]
E	" 00808		8-12-75	[illegible]
F	" 01572		8-25-76	[illegible]
G	" 02082		7-10-77	[illegible]
H	" 03464 G.D.H. 7-25-78		7-25-78	J. Mather
J	REVISED PER ECO 03536 BAKER 8-28-78		8/29/78	R. Wasserman
K	REVISED PER ECO 03687 BAKER 11-6-78		11/6/78	R. Wasserman
L	ADDED -503 PER ECO 03884 BAKER 1-31-79		2/13/79	[illegible]
M	REVISED PER ECO 04459 JSG		9-25-79	F. Hinkle
N	REVISED PER ECO 05041 JSG		28 MAR 80	Malcolm [illegible]

THE FOLLOWING NUMBERS ARE NOT USED:
CR24, R27, R58, R133, R137, R184, R226.

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	N	N	N	N	N	N	N	N															

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE CARD ASSEMBLY THRESHOLD DETECTORS THD001-1

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	J. HARTZELL	1-6 72	ENGINEER	R. WASSERMAN	8-1 72	DWG NO. PL 460-0906-501	REV N
CHECKED	R. OLIVIERI	4-26 72	APPROVED	R. CLEGG	10-25 72		
DRAFTING	SAMPEDRO	10-12 72	MANUF	HELLER	10-16 72	SHEET 1 OF 8	

800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. D
		460-0906-501		N	PARENT THD001-1	
1	001	400-1098			BOARD P.W. DUMBO	
1	002	108-203-041	7022-041-000001	C	CONN FING BLOC 41 POS	
12	007	102-422-104	CY20G104M		CAP .1UF 50V 20%	C1 C11 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23
6	011	102-305-225	150D225X0020A2		CAP 2.2UF 20V 20%	C5 C6 C7 C8 C9 C13
2	013	102-001-473	230B1B473		CAP .047UF 100V 20%	C30 C32
2	014	102-305-156	150D156X0020B2		CAP 15UF 20V 20%	C31 C3[illegible]
3	019	104-503-012		F	DIODE SIG MINIATURE	CR[illegible] CR[illegible] CR3
2	020	104-056-110	IN755A	P	DIODE ZENER CASE 51	CR4 CR8
1	021	104-056-104	1N757A	P	DIODE ZENER CASE 51	CR5
12	022	104-061-001	MBD101	A	DIODE MOT-CARRIER	CR6 CR7 CR16 CR17 CR18 CR19 CR20 CR21 CR27 CR28 CR29 CR30
1	025	104-308-006	IN821A	D	DILDE ZENER SILICON	CR9
16	026	104-503-014	1N4531	F	DIODE SIG MINIATURE	CR10 CR11 CR13 CR14 CR15 CR22 CR23 CR[illegible] CR26 CR3[illegible] CR3[illegible]

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						CR33
						CR35
						CR36
						CR37
						CR38
3	031	104-056-105	1N753A	P	DIODE ZENER CASE 51	CR12
						CR34
						CR39
10	035	103-304-001	2N4126	D	TRANS SIL PNP TO-92	Q1
						Q?
						Q4
						Q5
						Q6
						Q7
						Q10
						Q11
						Q14
						Q15
13	037	103-408-001	2N4124	C	TRANS SIL NPN TO-92	Q3
						Q8
						Q9
						Q12
						Q13
						Q16
						Q17
						Q18
						Q19
						Q20
						Q21
						Q22
						Q23
4	041	100-017-680	RC05GF680J		RES 68 1/8W 5%	R1
						R2
						R45
						R46
71	042	100-017-101	RC05GF101J		RES 100 1/8W 5%	R3
						R6
						R18
						R19
						R21
						R24
						R25
						R47
						R53
						R62
						R63
						R74
						R75
						R83
						R84
						R85
						R86
						R87
						R90
						R105

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
						R106
						R112
						R113
						R114
						R115
						R116
						R120
						R134
						R135
						R141
						R140
						R144
						R151
						R153
						R158
						R159
						R171
						R172
						R176
						R177
						R178
						R182
						R186
						R187
						R188
						R189
						R196
						R197
						R204
						R205
						R206
						R207
						R208
						R210
						R213
						R218
						R219
						R224
						R225
						R228
						R229
						R230
						R234
						R235
						R238
						R239
						R242
						R243
						R246
						R247
						R249
						R250
						R217
2	058	100-017-472	RC05GF472J		RES 4.7K 1/8W 5%	R4
						R92

PL460-0906-501 N
SHEET 4

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
7	059	100-0.7-272	RC05GF272J		RES 2.7K 1/8W 5%	R5
						R93
						R183
						R185
						R198
						R241
						R248
3	061	100-215-4990	RN55D4990F		RES 499 1/8W 1%	R7
						R51
						R79
6	063	100-215-1000	RN55D1000F		RES 100 1/8W 1%	R8
						R9
						R20
						R22
						R49
						R48
2	065	100-017-561	RC05GF561J		RES 560 1/8W 5%	R10
						R50
45	066	100-017-470	RC05GF470J		RES 47 1/8W 5%	R11
						R12
						R13
						R14
						R15
						R31
						R32
						R37
						R39
						R54
						R55
						R56
						R57
						R59
						R94
						R95
						R96
						R99
						R100
						R101
						R102
						R103
						R107
						R108
						R124
						R129
						R131
						R147
						R149
						R157
						R164
						R167
						R168
						R175
						R179
						R180
						R181

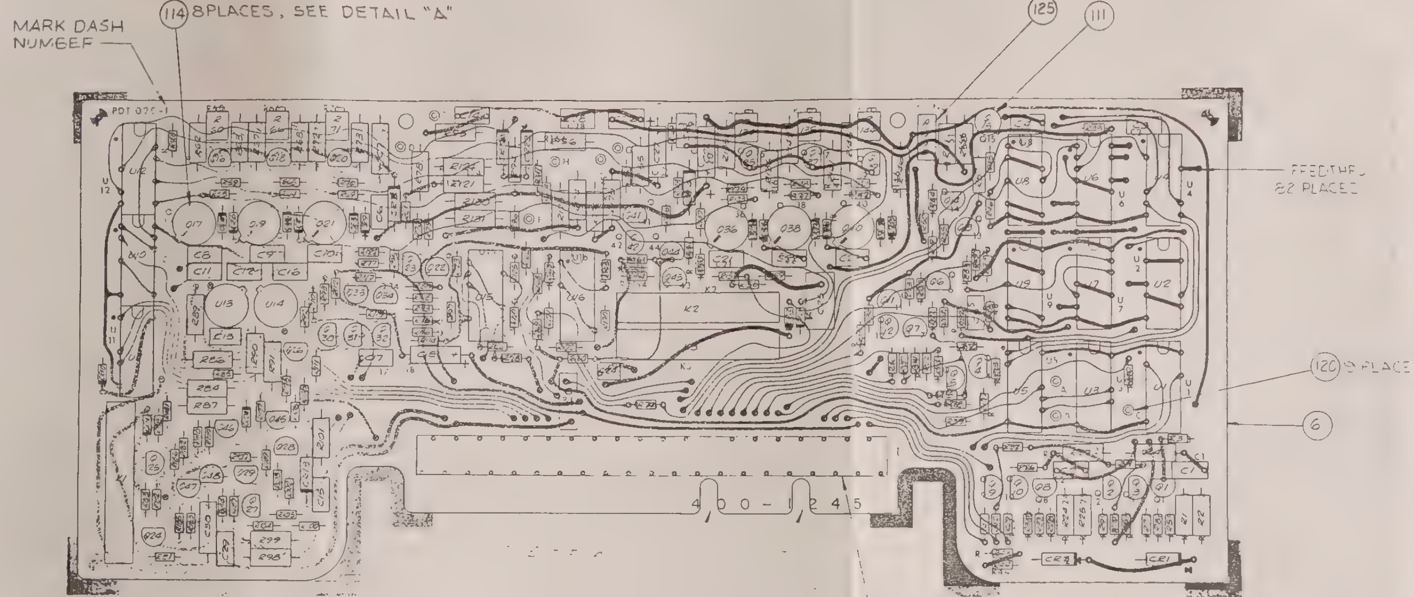
QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DE
						R194
						R195
						R199
						R200
						R236
						R237
						R244
						R245
7	075	100-017-152	RC05GF152J		RES 1.5K 1/8W 5%	R16
						R43
						R72
						R132
						R190
						R193
						R223
8	077	100-017-182	RC05GF182J		RES 1.8K 1/8W 5%	R17
						R23
						R60
						R117
						R126
						R138
						R161
						R209
12	080	100-017-102	RC05GF102J		RES 1K 1/8W 5%	R26
						R40
						R42
						R67
						R68
						R70
						R104
						R160
						R162
						R191
						R232
						R251
1	085	100-017-681	RC05GF681J		RES 680 1/8W 5%	R28
4	086	100-017-750	RC05GF750J		RES 75 1/8W 5%	R29
						R30
						R231
						R233
1	088	100-017-SBT	RC05		RES SBT 1/8W 5%	R33
12	090	100-017-153	RC05GF153J		RES 15K 1/8W 5%	R34
						R38
						R123
						R125
						R127
						R146
						R156
						R163
						R192
						R211
						R212
						R214
2	094	100-222-3651	RN50C3651F		RES 3.65K 1/20W 1%	R35
						R122

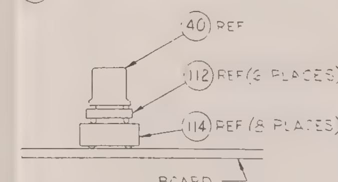
PL460-0906-501 N
SHEET 6

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
7	095	100-215-3651	RN55D3651F		RES 3.65K 1/8W 1%	R36
						R142
						R166
						R215
						R216
						R220
						R221
2	098	100-017-133	RC05GF133J		RES 13K 1/8W 5%	R47
						R69
2	099	100-017-822	RC05GF822J		RES 8.2K 1/8W 5%	R44
						R71
1	100	100-017-392	RC05GF392J		RES 3.9K 1/8W 5%	R53
5	101	100-215-2001	RN55D2001F		RES 2K 1/8W 1%	R61
						R65
						R150
						R152
						R155
1	103	100-222-2001	RN50C2001F		RES 2K 1/20W 1%	R64
2	104	100-215-5361	RN55D5361F		RES 5.36K 1/8W 1%	R66
						R154
2	105	100-017-912	RC05GF912J		RES 9.1K 1/8W 5%	R73
						R76
1	106	100-215-2490	RN55D2490F		RES 249 1/8W 1%	R77
2	107	100-017-682	RC05GF682J		RES 6.8K 1/8W 5%	R78
						R81
1	108	100-215-2321	RN55D2321F		RES 2.32K 1/8W 1%	R80
1	109	100-017-821	RC05GF821J		RES 820 1/8W 5%	R82
2	110	100-222-7500	RN50C7500F		RES 750 1/20W 1%	R88
						R89
1	111	100-017-162	RC05GF162J		RES 1.6K 1/8W 5%	R91
1	112	100-017-221	RC05GF221J		RES 220 1/8W 5%	R97
2	113	100-017-302	RC05GF302J		RES 3K 1/8W 5%	R98
						R109
8	114	100-215-3741	RN55D3741F		RES 3.74K 1/8W 1%	R110
						R111
						R118
						R119
						R139
						R145
						R202
						R203
2	116	100-017-163	RC05GF163J		RES 16K 1/8W 5%	R121
						R148
3	117	100-215-1211	RN55D1211F		RES 1.21K 1/8W 1%	R128
						R143
						R165
3	118	100-017-103	RC05GF103J		RES 10K 1/8W 5%	R130
						R201
						R240
5	122	100-215-1501	RN55D1501F		RES 1.5K 1/8W 1%	R136
						R169
						R173
						R222
						R227
1	125	100-215-1271	RN55D1271F		RES 1.27K 1/8W 1%	R170

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DE
1	126	100-215-1001	RN55D1001F		RES 1K 1/8W 1%	R174
7	129	139-209-002	CA3046	D	IC	U1
						U2
						U3
						U5
						U8
						U10
						U15
11	132	139-209-009	CA3054	D	TRANS/DIODE ARRAY	U4
						U6
						U7
						U9
						U11
						U12
						U13
						U14
						U16
						U17
						U18
1	134	139-045-807	SN151807N-10	E	IC DTL 14 PIN	U19
1	135	139-045-849	SN15849N-10	E	IC DTL 14 PIN	U20

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 460-1058 JCW	3-1-73	F HINKLE
	C	REVISED PER ECO 460-1058B-C WGS	4-2-73	R VOLZ
	D	REVISED PER ECO 460-1058D PAV	6-21-73	F HINKLE
	E	REVISED PER ECO [illegible] TMC	[illegible]	[illegible]
	F	REVISED PER ECO [illegible]	[illegible]	[illegible]
	G	REVISED PER ECO [illegible]	[illegible]	[illegible]
	H	REVISED PER ECO [illegible]	[illegible]	[illegible]
	J	REVISED PER ECO [illegible]	[illegible]	[illegible]
	K	REVISED PER ECO [illegible]	7-16-77	J. MATHER
	L	REVISED PER ECO [illegible]	7-27-7[illegible]	[illegible]
	M	REVISED PER ECO [illegible]	7-2-79	F Hinkle
	N	REVISED PER ECO C5414 RG	[illegible]	[illegible]





DETAIL "A"
(SCALE NONE)

NOTES:-
1.- FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG NO. A) 401-0010.
2.- MAXIMUM COMPONENT PROFILE IS .437.

FOR SCHEMATIC : SEE 430-1053 "C" SIZE
FOR PARTS LIST SEE PL 460-1058-501 & 502

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501	LIST OF MATERIALS					

	DATE
DRAWN F.J.T	2-5-73
CHECKED [illegible]	2-9-73
DRAFTING J. SAMPEDRO	3-1-73
ENGINEER R CLEGG	2-9-73
MFG R HELLER	2-21-73
APPROVED R CLEGG	2-9-73
APPROVED	

NEXT ASSY	USED ON
	9412

APPLICATION

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA 19034

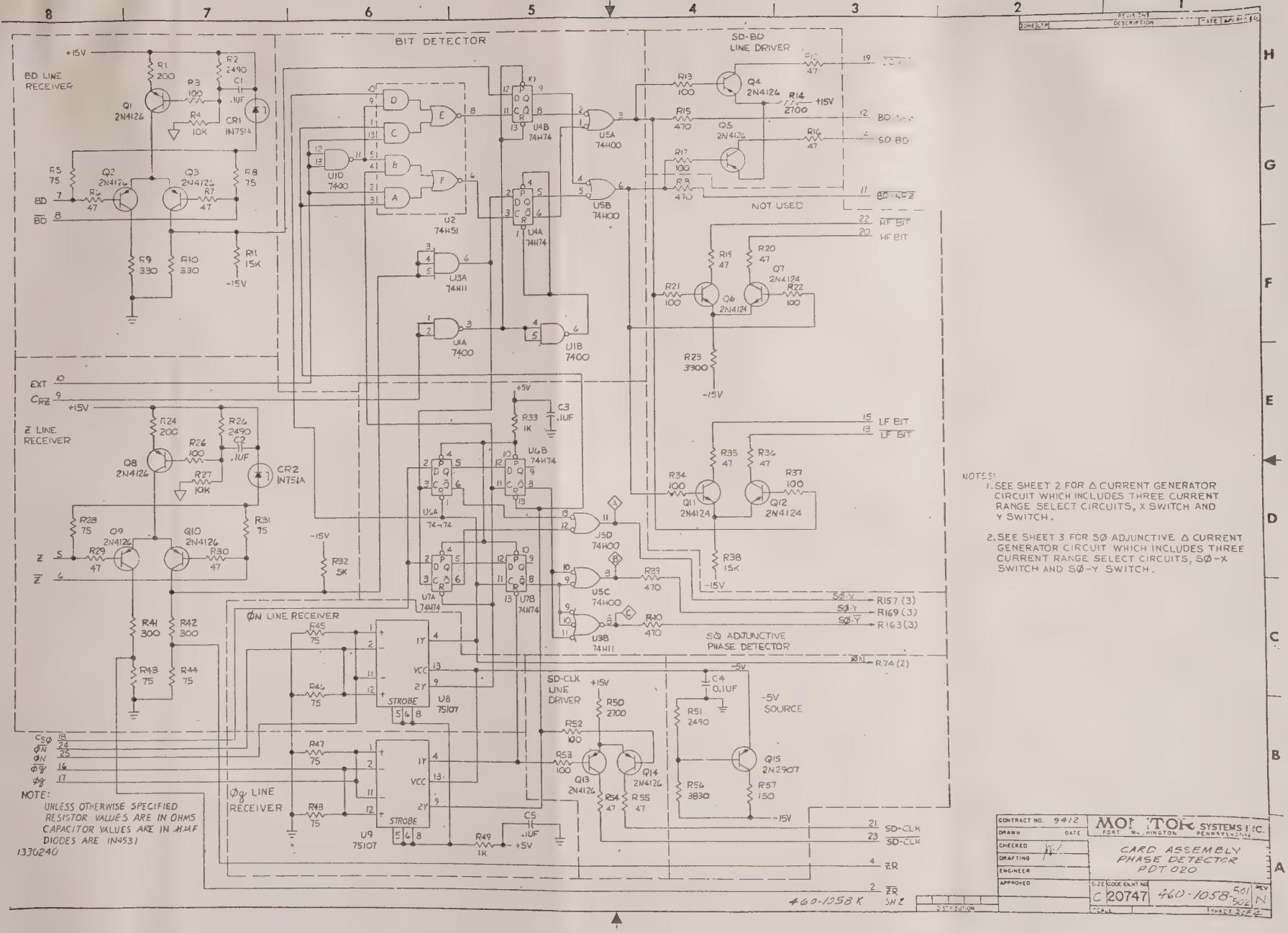
CARD ASSEMBLY
PHASE DETECTOR
PDT020-1-2

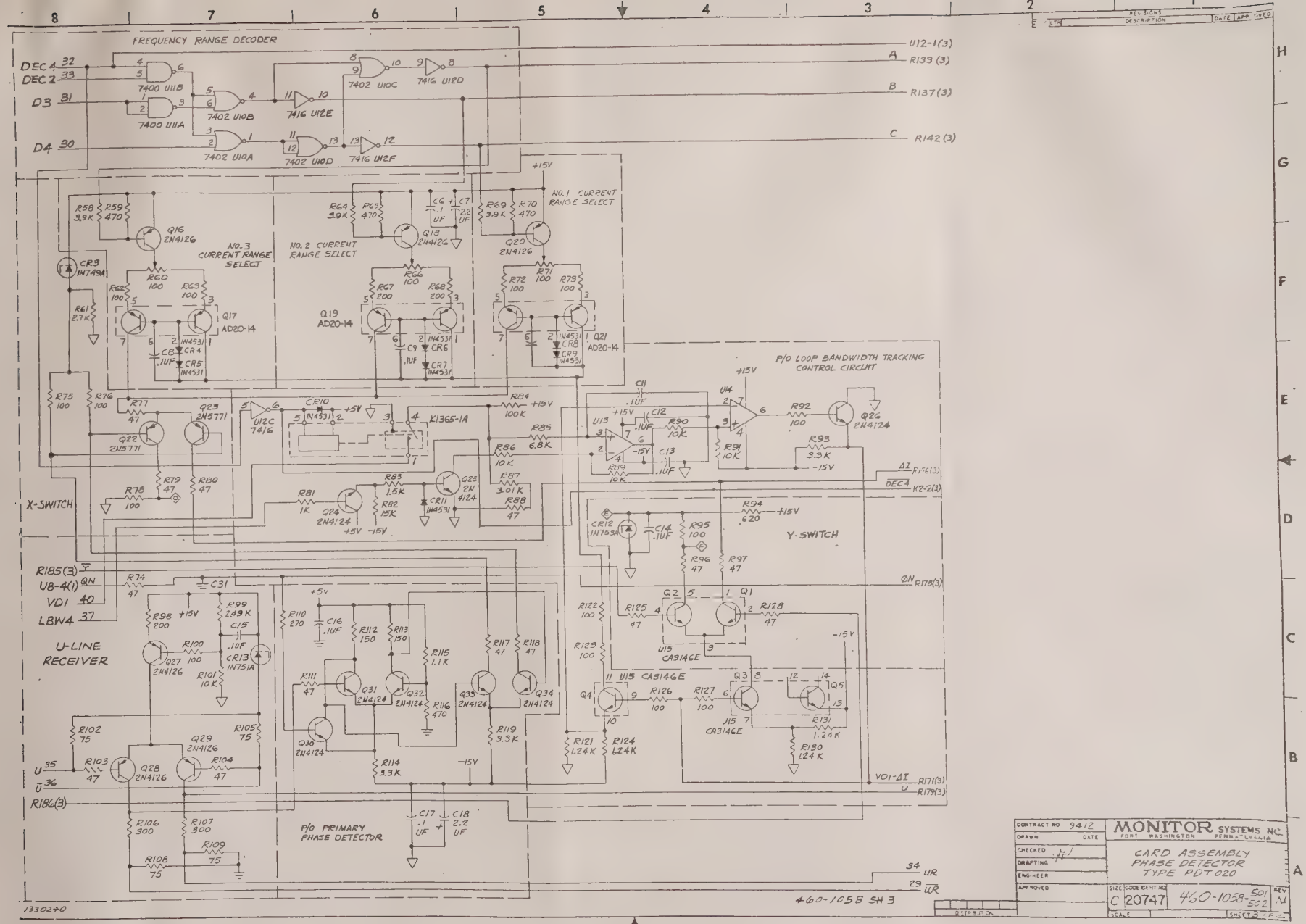
SIZE	CODE IDENT NO.		REV
D	20747	460-1058-▭	N

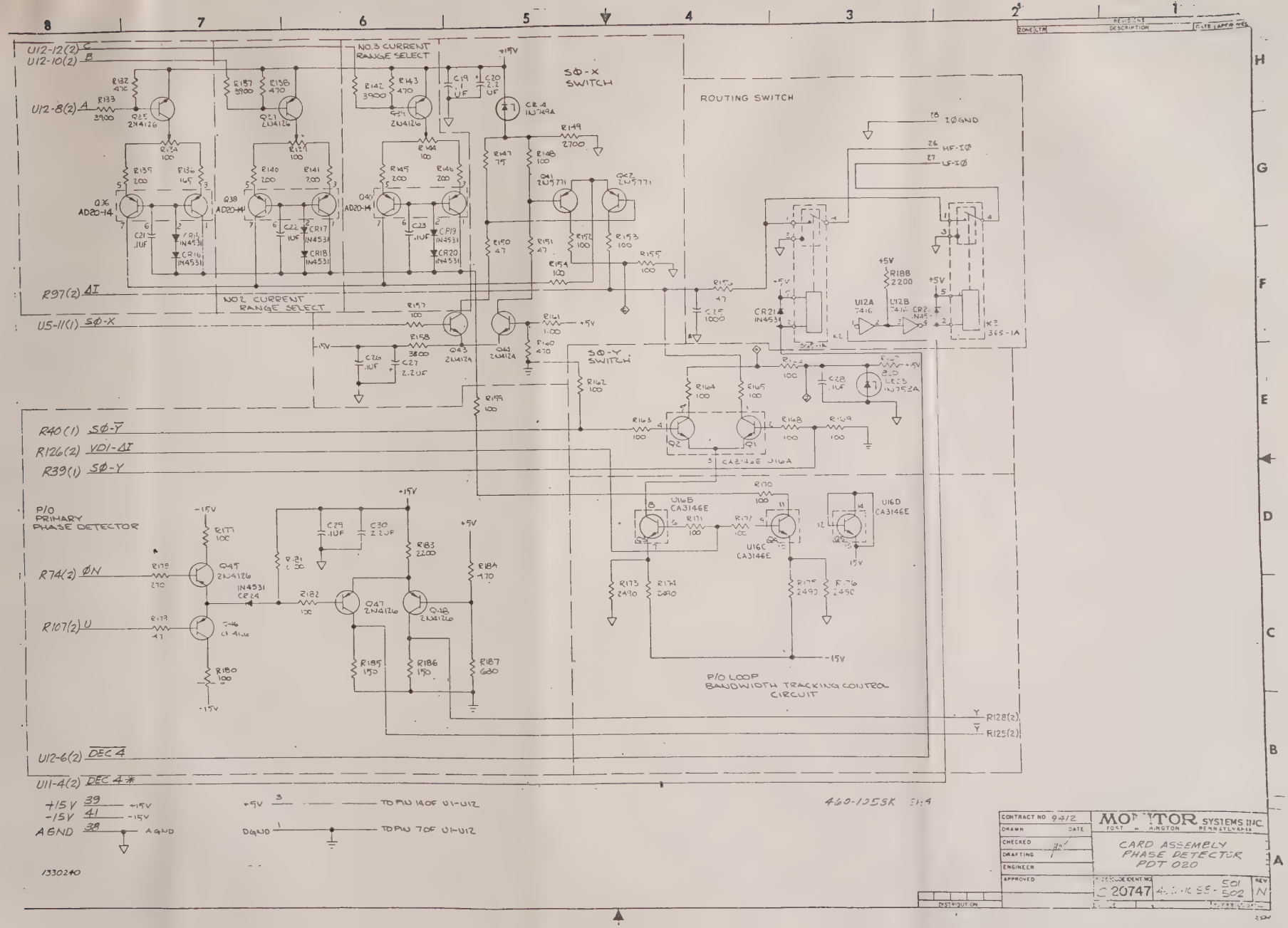
SCALE 2/1 — SHEET 1 OF 4

SHEETS 2,3,4 ARE "C" SIZE

800-0684-1


BIT DETECTOR
SD-BD LINE DRIVER
BD LINE RECEIVER
Z LINE RECEIVER
ØN LINE RECEIVER
Øg LINE RECEIVER
SØ ADJUNCTIVE PHASE DETECTOR
SD-CLK LINE DRIVER
-5V SOURCE
NOT USED
NOTES:
1. SEE SHEET 2 FOR Δ CURRENT GENERATOR CIRCUIT WHICH INCLUDES THREE CURRENT RANGE SELECT CIRCUITS, X SWITCH AND Y SWITCH.
2. SEE SHEET 3 FOR SØ ADJUNCTIVE Δ CURRENT GENERATOR CIRCUIT WHICH INCLUDES THREE CURRENT RANGE SELECT CIRCUITS, SØ-X SWITCH AND SØ-Y SWITCH.
NOTE: UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS CAPACITOR VALUES ARE IN MMF DIODES ARE IN4531
1330240
460-1058 K SH 2
CONTRACT NO. 9412
DRAWN
CHECKED
DRAFTING
ENGINEER
APPROVED
MOHTOK SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY PHASE DETECTOR PDT 020
SIZE C
CODE IDENT NO 20747
460-1058-501/502
REV N
SCALE
SHEET 2 OF 4


FREQUENCY RANGE DECODER
DEC 4 32
DEC 2 33
D3 31
D4 30
7400 U11B
7400 U11A
7402 U10B
7402 U10A
7402 U10C
7402 U10D
7416 U12E
7416 U12F
7416 U12D
U12-1(3)
R133 (3)
R137(3)
R142 (3)
NO.3 CURRENT RANGE SELECT
NO.2 CURRENT RANGE SELECT
NO.1 CURRENT RANGE SELECT
Q16 2N4126
Q18 2N4126
Q20 2N4126
Q17 AD20-14
Q19 AD20-14
Q21 AD20-14
CR3 IN749A
CR4 IN4531
CR5 IN4531
CR6 IN4531
CR7 IN4531
CR8 IN4531
CR9 IN4531
P/O LOOP BANDWIDTH TRACKING CONTROL CIRCUIT
U12C 7416
K1365-1A
Q22 2N5771
Q23 2N5771
Q24 2N4124
Q25 2N4124
Q26 2N4124
CR10 IN4531
CR11 IN4531
CR12 IN753A
X-SWITCH
Y-SWITCH
ΔI F1F6(3)
DEC 4 K2-2(3)
ØN R178(3)
VD1-ΔI R171(3)
U R179(3)
R185(3)
U8-4(1) ØN
VD1 40
LBW4 37
U-LINE RECEIVER
Q27 2N4126
Q28 2N4126
Q29 2N4126
U 35
Ū 36
R186(3)
Q31 2N4124
Q32 2N4124
Q33 2N4124
Q34 2N4124
Q30 2N4124
U15 CA3146E
Q1
Q2
Q3
Q4
Q5
P/O PRIMARY PHASE DETECTOR
34 UR
29 UR
460-1058 SH 3
13302+0
CONTRACT NO 9412
DRAWN
CHECKED
DRAFTING
ENGINEER
APPROVED
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
PHASE DETECTOR
TYPE PDT020
SIZE C
CODE IDENT NO 20747
460-1058-501/502
REV N
SCALE
SHEET 3 OF 3


U12-12(2) C
U12-10(2) B
U12-8(2) A
R97(2) ΔI
U5-11(1) SØ-X
R40(1) SØ-Ȳ
R126(2) VDI-ΔI
R39(1) SØ-Y
R74(2) ØN
R107(2) U
U12-6(2) DEC 4
U11-4(2) DEC 4*
NO.3 CURRENT RANGE SELECT
NO.2 CURRENT RANGE SELECT
SØ-X SWITCH
SØ-Y SWITCH
ROUTING SWITCH
P/O PRIMARY PHASE DETECTOR
P/O LOOP BANDWIDTH TRACKING CONTROL CIRCUIT
+15V 39 +15V
-15V 41 -15V
AGND 38 AGND
+5V 3 TO PIN 14 OF U1-U12
DGND 1 TO PIN 7 OF U1-U12
460-1255K
1330240
MONITOR SYSTEMS INC.
CARD ASSEMBLY PHASE DETECTOR PDT 020
C 20747
501
502
N

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-1058 JCW		3-1-73	F. HINKLE
C	REVISED PER ECO 460-1058B-C NES		4-2-73	R. VOLZ
D	REVISED PER ECO 460-1058D PAP		6-26-73	F. HINKLE
E	REVISED PER ECO 460-1058E TMB		1-15-74	R. VOLZ
F	REVISED PER ECO 460-1058F TMB		2-15-74	B. BICKEL
G	REVISED PER ECO 460-1058 PLS		4-5-74	R. VOLZ
H	REVISED PER ECO 00224 PAP		8-7-74	R. VOLZ
J	REVISED PER ECO 00491 TQ		1-10-75	J. COAKLEY
K	REVISED PER ECO 02082 JJM		7-16-77	J. MATHER
L	REVISED PER ECO 02254 JJM		6-7-77	J. NEWBY
M	REVISED PER ECO 04220 FTB		7-3-79	F. Hejibel
N	REVISED PER ECO 05414 RG		10-28-80	[illegible]
P	REVISED PER ECO 05727		26NOV80	RSVd2

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	P	P	N	N	N	N	N																

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
PHASE DETECTOR
PDT 020-1

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	F. J. T.	2-5-73	ENGINEER	R. CLEGG	2-9-73	DWG NO. PL460-1058-501 502	REV P
CHECKED	F. T. B.	2-9-73	APPROVED	R. CLEGG	2-9-73		
DRAFTING	J. SAMPEDRO	3-1-73	MFG	R. HELLER	2-21-73	SHEET 1 OF 7	

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		—	REF	1	D	460-1058-501	———	20747	CARD ASS'Y & SCHEM.	
		REF	—	2	D	460-1058-502	———	20747	CARD ASSY & SCHEM.	
				3						
				4						
				5						
		1	1	6	C	400-1245	———	20747	BD, PRINTED WIRING	
		1	—	7	A	297-0536				
		1	1	8	A	108-203-041	7022-041-000-001	91662	CONN. FINGER BLOCK	
				9						
				10						
				11						
		23	23	12	A	102-419-104	8131M10065 1104M	72982	CAP., .1UF, 100V, 20%	C1-6, 8-17, 19, 21-23,
				13						C26, 28, 29
		5	5	14	A	102-305-225	150D225X0020A2	56289	CAP., 2.2UF, 20V, 20%	C7, 18, 20, 27, 30
		1	1	15	A	102-419-SBT	8121M10065 1SBTM	72982	CAP., SBT, 100V, 20%	C24
		1	1	16	A	102-121-102	DM15C102J0100WV4CR	72136	CAP., 1000PF, 100V, 5%	C25
		1	—	17	A	102-101-SBT	DM15 SBT	72136	CAP., SBT, 100V, 5%	C31
				18						
				19						
				20						
				21						
		3	3	22	A	104-056-106	IN751A	04713	DIODE, ZENER	CR1, 2, 13

DRAWN
DATE
BOC 1A

CHECKED
DATE

TITLE PARTS LIST
PHASE DETECTOR, PDT020

CODE IDENT NO. 20747

DWG NO. PL 460-1058-501
SHEET 2 OF 7

REV P

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		2	2	23	A	104-056-102	IN749A	04713	DIODE, ZENER	CR3, CR14
		17	17	24	A	104-503-014	IN4531	07263	DIODE	CR4-11,15-22,24
		2	2	25	A	104-056-105	IN753A	04713	DIODE, ZENER	CR12, CR23
				26						
				27						
				28						
				29						
		3	3	30	A	106-016-002	365-1A	20891	RELAY	K1, K2, K3
				31						
				32						
				33						
		23	23	34	A	103-304-001	2N4126	04713	TRANSISTOR	Q1-5,8-10,13,14,16,18,
				35						Q20,27-29,35,37,
				36						Q39,45-48
		14	14	37	A	103-408-001	2N4124	04713	TRANSISTOR	Q6,7,11,12,24-26,
				38						Q30-34,43,44
		1	1	39	A	103-314-004	2N2907	12040	TRANSISTOR	Q15
		6	6	40	A	103-647-008	AD821	24355	TRANSISTOR, DUAL, PNP	Q17,19,21,36,38,40
		4	4	41	A	103-438-001	2N5771	07263	TRANSISTOR	Q22,23,41,42
				42						
				43						
				44						

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST PHASE DETECTOR, PDT020	20747	PL 460-1058-501 SHEET 3 OF 7	N

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
				45						
				46						
		10	10	47	A	100-215-2000	RN55D2000F	81349	RES., 200Ω, 1/10W, 1%	R1,24,67,68,98,135,
				48						R140,141,145,146
		4	4	49	A	100-215-2491	RN55D2491F	81349	RES., 2.49K, 1/10W, 1%	R2,25,51,99
		36	36	50	A	100-017-101	RC05GF101J	81349	RES., 100Ω, 1/8W, 5%	R3,13,17,21,22,26,
				51						R34,37,52,53,75,
				52						R76,92,100,122,123,
				53						R126,127,148,152-154,
				54						R157,159,162-165,
										R168-172,177,180,182
		7	7	55	A	100-215-1002	RN55D1002F	81349	RES., 10K, 1/10W, 1%	R4,27,86,89-91,101
		15	15	56	A	100-017-750	RC05GF750J	81349	RES., 75Ω, 1/8W, 5%	R5,8,28,31,43-48,
				57						R102,105,108,109,147
		29	30	58	A	100-017-470	RC05GF470J	81349	RES., 47Ω, 1/8W, 5%	R6,7,12,16,19,20,29,
				59					(OMIT R74 ON 502)	R30,35,36,54,55,
				60						R74,77,79,80,88,96,
				61						R97,103,104,111,117,118,
										R125,128,150,151,156,179
		2	2	62	A	100-017-331	RC05GF331J	81349	RES., 330Ω, 1/8W, 5%	R9, R10
		4	4	63	A	100-017-153	RC05GF153J	81349	RES., 15K, 1/8W, 5%	R11,32,38,82
		5	5	64	A	100-017-272	RC05GF272J	81349	RES., 2.7K, 1/8W, 5%	R14,50,61,149,181
		13	13	65	A	100-017-471	RC05GF471J	81349	RES., 470Ω, 1/8W, 5%	R15,18,39,40,59,65,70,
				66						R116,132,138,143,160,184

DRAWN
DATE

CHECKED
DATE

TITLE PARTS LIST
PHASE DETECTOR PDT020

CODE IDENT NO. 20747

DWG NO. PL460-1058-501

SHEET 4 OF 7

REV N

800 VA

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		5	5	67	A	100-017-332	RC05GF332J	81349	RES., 3.3K, 1/8W, 5%	R23,93,114,119,158
		3	3	68	A	100-017-102	RC05GF102J	81349	RES., 1K, 1/8W, 5%	R33,49,81
		4	4	69	A	100-017-301	RC05GF301J	81349	RES., 300Ω, 1/8W, 5%	R41,42,106,107
		1	1	70	A	100-215-3831	RN55D3831F	81349	RES., 3.83K, 1/10W, 1%	R56
		1	1	71	A	100-003-151	RC07GF151J	81349	RES., 150Ω, 1/4W, 5%	R57
		6	6	72	A	100-017-392	RC05GF392J	81349	RES., 3.9K, 1/8W, 5%	R58,64,69,133,137,142
		6	6	73	A	101-124-101	562-72HS	65092	RES., VAR., 100Ω, .2W, 5%	R60,66,71,134,139,144
		8	8	74	A	100-215-1000	RN55D1000F	81349	RES., 100Ω, 1/10W, 1%	R62,63,72,73,78,
				75						R95,155,166
		1	1	76	A	100-017-152	RC05GF152J	81349	RES., 1.5K, 1/8W, 5%	R83
		1	1	77	A	100-215-1003	RN55D1003F	81349	RES., 100K, 1/10W, 1%	R84
		1	1	78	A	100-017-682	RC05GF682J	81349	RES., 6.8K, 1/8W, 5%	R85
		1	1	79	A	100-215-3011	RN55D3011F	81349	RES., 3.01K, 1/10W, 1%	R87
		1	1	80	A	100-003-621	RC07GF621J	81349	RES., 620Ω, 1/4W, 5%	R94
		2	2	81	A	100-017-271	RC05GF271J	81349	RES., 270Ω, 1/8W, 5%	R110, R178
		4	4	82	A	100-017-151	RC05GF151J	81349	RES., 150Ω, 1/8W, 5%	R112,113,185,186
		2	2	83	A	100-017-112	RC05GF112J	81349	RES., 1.1K, 1/8W, 5%	R115, R161
		1 SET	1SET	84	A	100-021-003	SEE SPEC	81349	RES., MATCHED SET, 1.24K, 1/10W, 0.1%	R121&124, 130&131
		1	1	85	A	100-215-1650	RN55D1650F	81349	RES., 165Ω, 1/10W, 1%	R136
		1	1	86	A	100-017-821	RC05GF821J	81349	RES., 820Ω, 1/8W, 5%	R167
		1 SET	1SET	87	A	100-021-004	SEE SPEC	81349	RES., MATCHED SET, 2.49K, 1/10W, 0.1%	R173&176, 174&175
		2	2	88	A	100-017-222	RC05GF222J	81349	RES., 2.2K, 1/8W, 5%	R183, R188

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST PHASE DETECTOR, PDT020	20747	PL 460-1058-501 SHEET 5 OF 7	N

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	89	A	100-017-681	RC05GF681J	81349	RES., 680Ω, 1/8W, 5%	R187
		1	–	90	A	100-017-5BT	RC05GF5BTJ	81349	RES., 5BT, 1/8W, 5%	R74
				91						
				92						
				93						
				94						
				95						
				96						
		2	2	97	A	139-046-400	SN7400N	01295	IC, TTL	U1, U11
		1	1	98	A	139-051-451	SN74H51N	01295	IC, TTL	U2
		1	1	99	A	139-051-411	SN74H11N	01295	IC, TTL	U3
		3	3	100	A	139-051-474	SN74H74N	01295	IC, TTL	U4, U6, U7
		1	1	101	A	139-051-400	SN74H00N	01295	IC, TTL	U5
		2	2	102	A	139-232-001	NE521A	18324	IC,	U8, U9
		1	1	103	A	139-046-402	SN7402N	01295	IC, TTL	U10
		1	1	104	A	139-046-416	SN7416N	01295	IC, TTL	U12
		2	2	105	A	139-141-001	AD741KH	24355	IC	U13, U14
		2	2	106	A	139-209-013	CA3146E	86684	IC	U15, U16
				107						
				108						
				109						
				110						

DRAWN
DATE

CHECKED
DATE

TITLE PARTS LIST
PHASE DETECTOF PDT020

CODE IDENT NO. 20747

DWG NO. PL 460-1058-501

SHEET 6 OF 7

REV N

BCO 58A

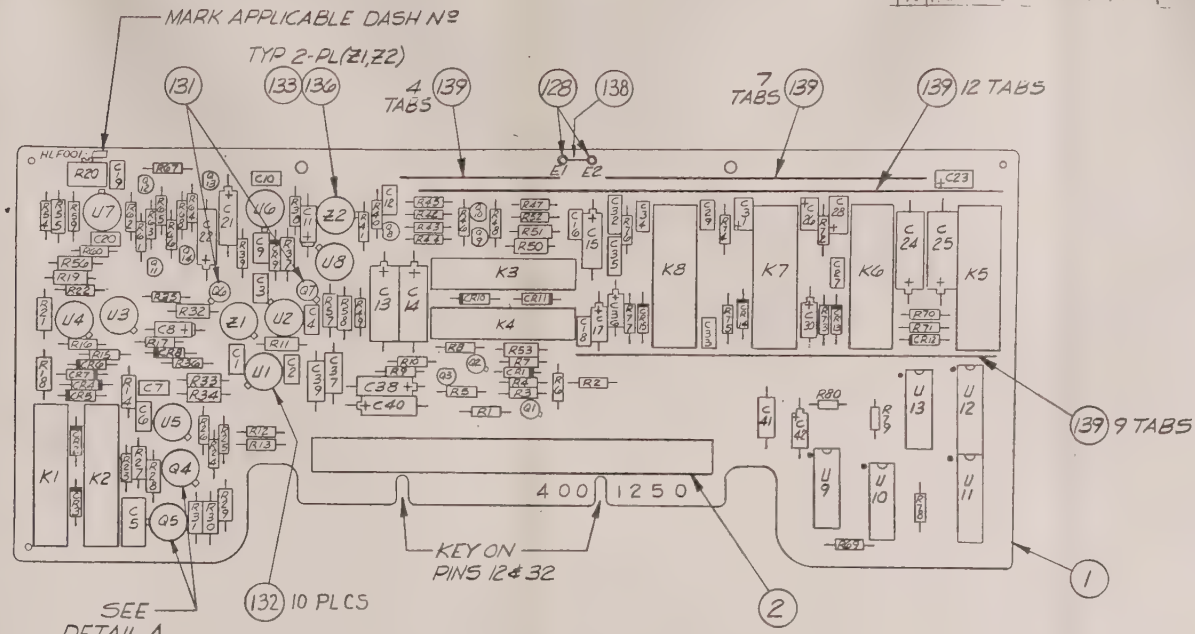
AYDIN MONITOR SYSTEMS

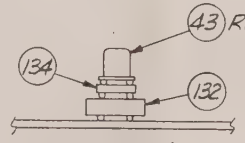
QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	111	A	131-013-001	10047	07047	PAD, TRANS., TO-18	USE WITH Q15
		6	6	112	A	131-049-001	RC-T018100-2A	19080	INSULATOR, PAD, TRANS.	USE WITH Q17,19
				113						Q21,36,38,40
		8	8	114	A	131-017-001	10229	07047	PAD, TRANS.	USE WITH Q17,19
				115						Q21,36,38,40,U13,14
				116						
				117						
				118						
				119						
		9	9	120	A	118-005-003	1604205	71279	TERMINAL, TURRET	A,B,C,D,E,F,G,H,J
				121						
				122						
				123						
				124						
		1	1	125	A	121-202-010	8041-G6	91506	TEST JACK, BLACK	A GND
				126						
				127						
				128						
				129						
		AR	AR	130	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571
				131						
				132						

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST PHASE DETECTOR, PDT 020	20747	PL460-1058-501 SHEET 7 OF 7	N

800-0438A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		B TO R SEE WL FOR ECO NOS		
	S	REVISED PER ECO [illegible]	JSG	
	U	[illegible]		





DETAIL A
NO SCALE

NOTES:

1- FOR GENERAL ENGINEERING & MANUFACTURING INFO, SEE DWG A) 401-0010.

2- MAXIMUM COMPONENT PROFILE IS .437

3- DO NOT CRIMP LEADS ON C5, C29, C32, C34, C35.

FOR PARTS LIST SEE PL 460-1065-☐

QTY	ITEM	FSCM	MONITOR P/N	MFR P/N	DESCRIPTION	NOTES
001					LIST OF MATERIALS	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND APPLY BEFORE FINISH
SURFACE ROUGHNESS 125/
TOLERANCE ON FRACTIONS ± 1/64 | DECIMALS .XX ± .02, .XXX ± .005 | ANGLES ± 1/2°
MATERIAL
FINISH

DRAWN F.T.B. DATE 1-17-73
CHECKED R.H. 2-9-73
DRAFTING SAMPEDRO 3-2-73
ENGINEER R. CLEGG 2-9-73
MFG R. HELLER 2-21-73
APPROVED R. CLEGG 2-9-73

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

CARD ASSEMBLY
HIGH-FREQ LOOP FILTER
HLF001-1, -2, -3

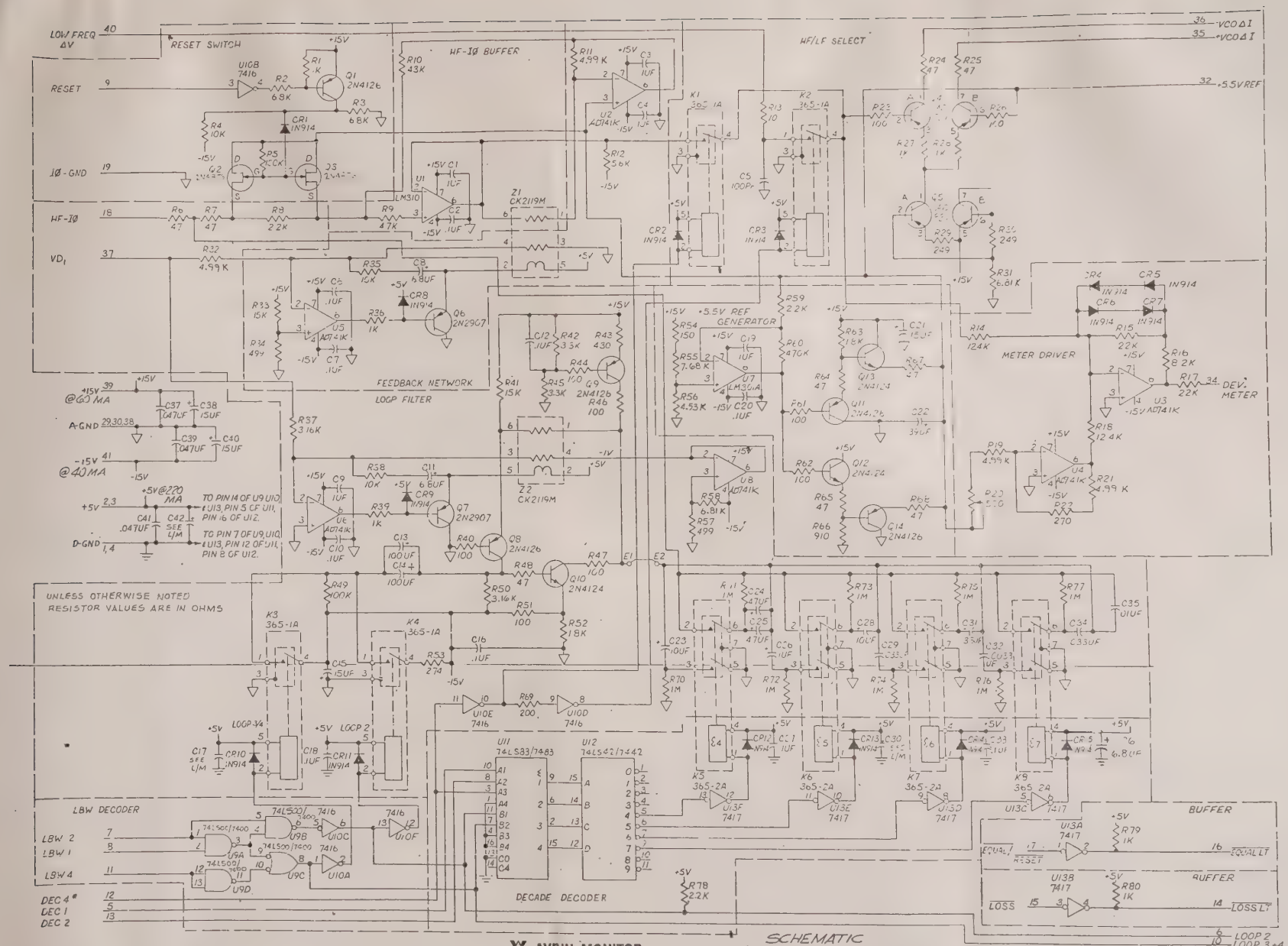
SIZE	CODE IDENT NO.		REV
C	20747	460-1065-501/502/503	W

SCALE ~ SHEET 1 OF 2

	9412
NEXT ASSY	USED ON
APPLICATION	

MONITOR SHOP STANDARDS ARE AN INTEGRAL PART OF THIS DRAWING (296-0077)

800-0187C


LOW FREQ ΔV
RESET
IØ-GND
HF-IØ
VD1
RESET SWITCH
HF-IØ BUFFER
HF/LF SELECT
FEEDBACK NETWORK
LOOP FILTER
+5.5V REF GENERATOR
METER DRIVER
DEV. METER
UNLESS OTHERWISE NOTED RESISTOR VALUES ARE IN OHMS
LBW DECODER
DECADE DECODER
BUFFER
LOOP 2
LOOP 3+4
AYDIN MONITOR SYSTEMS
FSCM 20747
SCHEMATIC HI-FREQ LOOP FILTER HLF001-□
460-1005-□ REV W
SHEET 2

REVISIONS

REV	DESCRIPTION		EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-1065			3-1-73	F. HINKLE
C	460-1065C			4-2-73	R. VOLZ
D	460-1065D			5-1-73	F. HINKLE
E	460-1065E			5-25-73	F. HINKLE
F	460-1065F			6-27-73	F. HINKLE
G	460-1065G			7-9-73	F. HINKLE
H	460-1065H			2-14-74	J. RONEY
J	00772			5-12-75	J. RONEY
K	01495			6-15-76	D. MOUAT
L	02254			6-7-77	J. NEWBY
M	REVISED PER ECO 03465			8-7-78	J. MATHER
N	REVISED PER ECO 03537	BAKER 8-29-78		8/30/78	K Wasserman
P	REVISED PER ECO 03604	BAKER 9-26-78		11/10/78	D D Mouat
R	REVISED PER ECO 03587	JST		3/6/79	F. Hinkle
S	REVISED PER ECO 04459	JSG		9-25-79	F Hinkle
T	REVISED PER ECO 05520	TJG 7-2-80		15 Jul 80	RS Volz
U	REVISED PER ECO 05420	RV 8-13-80		14 Aug 80	RS Volz
V	REVISED PER ECO 05567	BAKER 10 OCT 1980		10/[illegible]	[illegible]
W	REVISED PER ECO 06784				

THE FOLLOWING NUMBERS ARE NOT USED:
CR4-CR7, -502 ASSY
C33-C36, -503 ASSY

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	W	T	V	W	S	S	U	W															

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 18034

TITLE CARD ASSEMBLY HI-FREQ LOOP FILTER HLF001-1, -2, -3

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	F.T.B.	1-17-73	ENGINEER	R. CLEGG	2-9-73	DWG NO. PL 460-1065-501 502 503	REV W
CHECKED	R.H.	2-9-73	APPROVED	R. CLEGG	2-9-73		
DRAFTING	SAMPEDRO	3-2-73	MANUF.	R. HELLER	2-21-73	SHEET 1 OF 8	

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			X		C				ASSY, HLF001-1	
		X			C				ASSY, HLF001-2	
	X				C				ASSY, HLF001-3	
	1	1	1	1	C	400-1250	———	20747	BD, PRINTED WIRING	
	1	1	1	2	A	108-203-041	7022-041-000-001	91662	CONN, FINGER BLOCK	
				3						
				4						
				5						
				6						
	14	15	15	7	A	102-419-104	CY30A104M	71590	CAP., .1μF, 100V, 20%	C1-C4, C6, C7, C9, C10, C12, C16 C18-C20, C27, C33
				8						
				9						
	1	1	1	10	A	102-121-101	DM15CA101J04CR	72136	100pF, 100V, 5%	C5 (NOTE 3)
	2	2	2	11	A	102-313-685	150D685X0006A2	56289	6.8μF, 6V, 20%	C8, C11
	2	2	2	12	A	102-306-107	150D107X0010R2	56289	100μF, 10V, 20%	C13, C14
	4	4	4	13	A	102-305-156	150D156X0020B2	56289	15μF, 20V, 20%	C15, C21, C38, C40
				14						
	—	4	4	15	A	102-313-685	150D685X0006A2	56289	6.8μF, 6V, 20%	C17, C30, C36, C42
				16	A					
	3	—	—	17	A	102-306-475	150D475X0010A2	56289	CAP., 4.7μF, 10V, 20%	C17, C30, C42

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
F.T.B.	R.H.	CARD ASSEMBLY	20747	460-1065-□	1
DATE 1-17-73	DATE 2-9-73	HLF001-□		SHEET 2 OF	

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
	1	1	1	18	A	102-304-396	150D396X9010B2	56289	CAP., 39 µF, 10V, 10%	C 22
	2	2	2	19	A	102-369-106	T330B106M035AS	31433	10µF, 35V, 20%	C23, C28
	2	2	2	20	A	102-305-476	150D476X0020R2	56289	47µF, 20V, 20%	C24, C25
	1	1	1	21	A	102-369-105	T330B105M035AS	31433	1 µF, 35V, 20%	C26
	2	2	2	22	A	102-428-333	3420-100C-333K	04222	.033µF, 100V, 10%	C29, C34 (NOTE 3)
	1	1	1	23	A	102-366-004	T330B334K035AS	31433	.33µF, 35V, 10%	C31
	1	1	1	24	A	102-417-332	3420-100A-332K	04222	.0033µF, 100V, 10%	C32 (NOTE 3)
	1	1	1	25	A	102-417-103	3421-100A-103K	04222	.01µF, 100V, 10%	C35 (NOTE 3)
	3	3	3	26	A	102-001-473	CW1473M	96733	CAP., .047µF, 100V, 20%	C37, C39, C41
				27						
	15	–	15	28	A	104-014-001	IN914	01295	DIODE	CR1-CR15
	–	11	–	29	A	104-014-001	IN914	01295	DIODE	CR1-CR3 CR8-CR15
				30						
				31						
				32						
	4	4	4	33	A	106-016-002	365-4-1A	20891	RELAY	K1-K4
	4	4	4	34	A	106-016-001	365-4-2A	20891	RELAY	K5-K8
				35						
				36						
				37						
				38						
				39						

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
F.T.B.	R.H.	CARD ASSEMBLY HLF001-□	20747	460-1065-□	V
DATE 1-17-73	DATE 2-9-73			SHEET 3 OF	

800-0438A

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
	5	5	5	40	A	103-304-001	2N4126	04713	TRANSISTOR, PNP	Q1, Q8, Q9 Q11, Q14
				41						
	2	2	2	42	A	103-350-001	2N4856	01295	N-FET	Q2, Q3
	2	2	2	43	A	103-647-008	AD821	24355	DUAL PNP	Q4, Q5
	–	2	2	44	A	103-314-004	2N2907	12040	PNP	Q6, Q7
				45						
	2	–	–	46	A	103-314-204	2N2907	04713	PNP	Q6, Q7
	3	3	3	47	A	103-408-001	2N4124	04713	TRANSISTOR, NPN	Q10, Q12, Q13
				48						
				49						
				50						
	3	3	3	51	A	100-003-102	RC07GF102J	81349	RES, 1K, 1/4W, 5%	R1, R36, R39
	2	2	2	52	A	100-003-682	RC07GF682J	81349	6.8K, 1/4W, 5%	R2, R3
	3	3	3	53	A	100-003-103	RC07GF103J	81349	10K, 1/4W, 5%	R4, R35, R38
	2	2	2	54	A	100-003-104	RC07GF104J	81349	100K, 1/4W, 5%	R5, R49
	9	9	9	55	A	100-003-470	RC07GF470J	81349	47Ω, 1/4W, 5%	R6, R7, R24 R25, R48, R64 R65, R67, R68
				56						
				57						
	3	3	3	58	A	100-003-222	RC07GF222J	81349	2.2K, 1/4W, 5%	R8, R59, R78
	1	1	1	59	A	100-003-472	RC07GF472J	81349	4.7K, 1/4W, 5%	R9
	1	1	1	60	A	100-003-433	RC07GF433J	81349	RES, 43K, 1/4W, 5%	R10
				61						

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
F.T.B. DATE 1-17-73	R.H. DATE 2-9-73	CARD ASSEMBLY HLF001-□	20747	460-1065-□ SHEET 4 OF	W

800-0438A

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
	4	4	4	62	A	100-215-4991	RN55D4991F	81349	RES, 4.99 K, 1/10W, 1%	R11, R19
				63						R21, R32
	1	1	1	64	A	100-003-562	RC07GF562J		5.6K, 1/4W, 5%	R12
	1	1	1	65	A	100-003-100	RC07GF100J		10Ω, 1/4W, 5%	R13
	2	2	2	66	A	100-215-1242	RN55D1242F		12.4K, 1/10W, 1%	R14, R18
	2	2	2	67	A	100-003-223	RC07GF223J		22K, 1/4W, 5%	R15, R17
	1	1	1	68	A	100-003-822	RC07GF822J	81349	8.2K, 1/4W, 5%	R16
	1	1	1	69	A	101-116-204	502-T2S-500Ω	94271	VAR, 500Ω, .6W, 5%	R20
	1	1	1	70	A	100-003-271	RC07GF271J	81349	270Ω, 1/4W, 5%	R22
	8	8	8	71	A	100-003-101	RC07GF101J		100Ω, 1/4W, 5%	R23, R26, R40
				72						R44, R46, R47
				73						R61, R62
	2	2	2	74	A	100-215-1001	RN55D1001F		1K, 1/10W, 1%	R27, R28
	2	2	2	75	A	100-215-2490	RN55D2490F		249Ω, 1/10W, 1%	R29, R30
	2	2	2	76	A	100-215-6811	RN55D6811F		6.81K, 1/10W, 1%	R31, R58
	1	1	1	77	A	100-215-1502	RN55D1502F		15K, 1/10W, 1%	R33
	2	2	2	78	A	100-215-4990	RN55D4990F		499Ω, 1/10W, 1%	R34, R57
	2	2	2	79	A	100-215-3161	RN55D3161F		3.16K, 1/10W, 1%	R37, R50
	1	1	1	80	A	100-003-153	RC07GF153J		15K, 1/4W, 5%	R41
	2	2	2	81	A	100-003-332	RC07GF332J		3.3K, 1/4W, 5%	R42, R45
	1	1	1	82	A	100-003-431	RC07GF431J	81349	RES, 430Ω, 1/4W, 5%	R43
				83						

DRAWN F.T.B. DATE 1-17-73	CHECKED R.H. DATE 2-9-73	TITLE CARD ASSEMBLY HLF001-□	CODE IDENT NO. 20747	DWG NO. 460-1065-□ SHEET 5 OF	REV 5

800-0438A

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
	1	1	1	84	A	100-215-1000	RN55D1000F	81349	RES, 100Ω, 1/10W, 1%	R51
	2	2	2	85	A	100-003-182	RC07GF182J		1.8K, 1/4W, 5%	R52, R63
	1	1	1	86	A	100-215-2740	RN55D2740F		274Ω, 1/10W, 1%	R53
	1	1	1	87	A	100-003-151	RC07GF151J		150Ω, 1/4W, 5%	R54
	1	1	1	88	A	100-215-7681	RN55D7681F		7.68K, 1/10W, 1%	R55
	1	1	1	89	A	100-215-4531	RN55D4531F		4.53K, 1/10W, 1%	R56
	1	1	1	90	A	100-003-474	RC07GF474J		470K, 1/4W, 5%	R60
	1	1	1	91	A	100-003-911	RC07GF911J		910Ω, 1/4W, 5%	R66
	1	1	1	92	A	100-003-201	RC07GF201J		200Ω, 1/4W, 5%	R69
	8	8	8	93	A	100-003-105	RC07GF105J		1MEG, 1/4W, 5%	R70-R77
	2	2	2	94	A	100-017-102	RC05GF102J	81349	RES, 1K, 1/8W, 5%	R79, R80
				95						
				96						
				97						
				98						
				99						
				100						
				101						
				102						
				103						
				104						
				105						

DRAWN F.T.B. DATE 1-17-73	CHECKED R.H. DATE 2-9-73	TITLE CARD ASSEMBLY HLF001-□	CODE IDENT NO. 20747	DWG NO. 460-1065-□ SHEET 6 OF	REV 5

800-043P

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
	1	1	1	106	A	139-144-001	LM310H	27014	I.C., VOLTAGE FOLLOWER	U1
	6	6	6	107	A	139-141-001	AD741KH	24355	, OPAMP	U2-U6, U8
	1	1	1	108	A	139-127-003	LM301AH	27014	, OPAMP	U7
	1	—	—	109	A	139-198-400	SN74LS00N	01295	, TTL QUAD NAND GATE	U9
	—	1	1	110	A	139-046-400	SN7400N	01295	, TTL QUAD NAND GATE	U9
	1	1	1	111	A	139-046-416	SN7416N	01295	, TTL HEX INVERTER	U10
	—	1	1	112	A	139-046-483	SN7483N	01295	, TTL 4-BIT ADDER	U11
	1	—	—	113	A	139-198-483	SN74LS83N	01295	, TTL 4-BIT ADDER	U11
	—	1	1	114	A	139-046-442	SN7442N	01295	, TTL BCD DECODER	U12
	1	—	—	115	A	139-198-442	SN74LS42N	01295	, TTL BCD DECODER	U12
	1	1	1	116	A	139-046-417	SN7417N	01295	I.C., TTL HEX BUFFER	U13
				117						
				118						
				119						
				120						
	2	2	2	121	A	139-140-001	CK2119M	49956	RAYSISTOR	Z1, Z2
				122						
				123						
				124						
				125						
				126						
				127						

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
F.T.B.	R.H.	CARD ASSEMBLY HLF001-□	20747	460-1065-□	U
DATE 1-17-73	DATE 2-9-73			SHEET 7 OF	

800-0438A

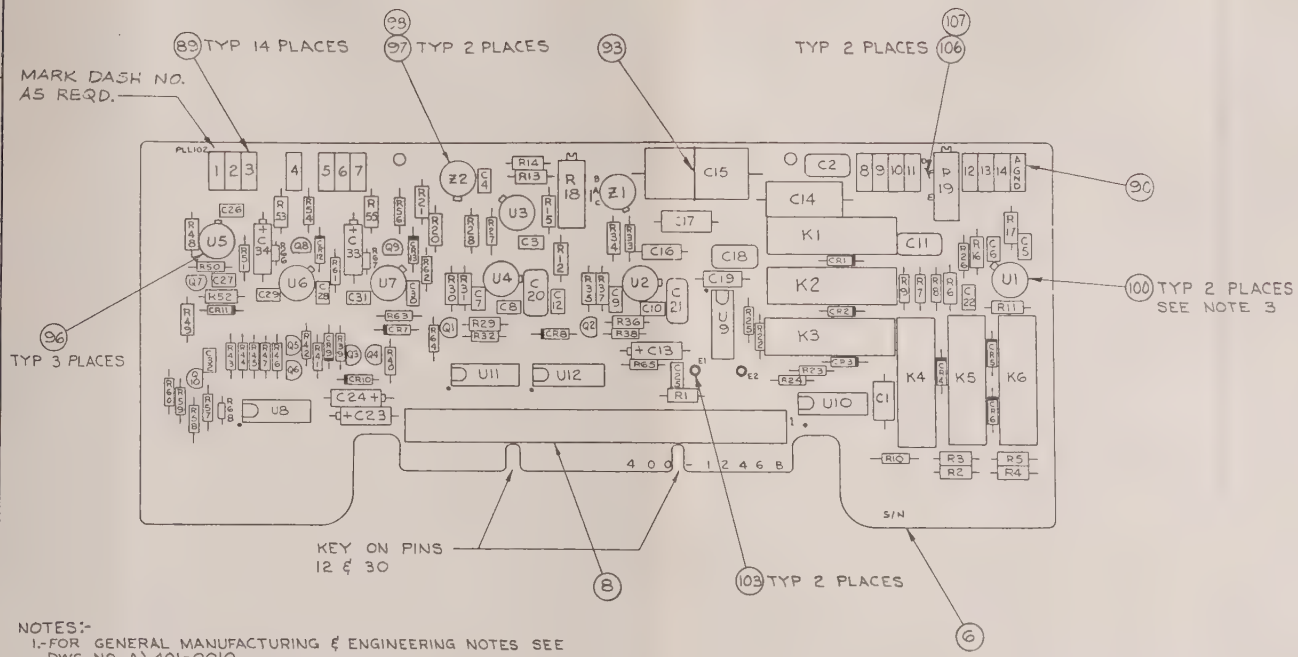
AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
	2	2	2	128	A	118-005-003	1604-2-05	71279	TERMINAL, TURRET	E1, E2
				129						
				130						
	4	4	4	131	A	131-013-001	10047	07047	PAD, TRANSISTOR (TO-18)	FOR Q6, Q7
	10	10	10	132	A	131-017-001	10383	07047	PAD, TRANSISTOR	FOR U1-U8, Q4, Q5
	2	2	2	133	A	131-015-001	10037	07047	PAD, TRANSISTOR (TO-5)	FOR Z1, Z2
	2	2	2	134	A	131-049-001	RC-TO18100-2A	19080	PAD, TRANSISTOR	FOR Q4, Q5
				135						
	2	2	2	136	A	131-020-001	10284	07047	COVER (TO-5)	FOR Z1, Z2
				137						
	1/2"	1/2"	1/2"	138	A	113-001-006	299/1	92194	WIRE, BUS, # 26 AWG	
	18"	18"	18"	139	A	217-0312-001	—	20747	BUS BAR	
				140						
				141						
	AR	AR	AR	142	A	120-101-001	———	81348	SOLDER, SN60 WRAP	QQ-S-571
				143						
				144						
				145						
				146						
				147						
				148						
				149						

DRAWN F.T.B. DATE 1-17-73	CHECKED R.H. DATE 2-9-73	TITLE CARD ASSEMBLY HLF001-□	CODE IDENT NO. 20747	DWG NO. 460-1065-□ SHEET 8 OF	REV W

800-0431

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	SEE PL460-1059-□ FOR PREVIOUS REVISIONS	—	—
	M	REVISED PER ECO 04220 FTB	7-16-73	7/11/73



NOTES:-
1.-FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG NO. A) 401-0010.
2.-THE MAXIMUM COMPONENT PROFILE IS .390.
3.-ITEM 77, LEAD LENGTH (FOR SOCKET MOUNTING) SHALL BE CUT TO 3/16" ± 1/32.

FOR PARTS LIST SEE PL 460-1059-□

QTY	ITEM	FSCM	MONITOR P/N	MFR P/N	DESCRIPTION	NOTES
001					LIST OF MATERIALS	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND APPLY BEFORE FINISH SURFACE ROUGHNESS 125/ TOLERANCE ON

FRACTIONS	DECIMALS	ANGLES
± 1/64	± .XX=.02 ± .XXX=.005	± 1° ± 1/2

MATERIAL

FINISH

	DRAWN	DATE
	K HOUSEAL	1-5-73
	CHECKED J. DILELLO	1-26-73
	DRAFTING J. SAMPEDRO	3-2-73
	ENGINEER T. LOCASALE	2-21-73
	MFG K. HELLER	2-21-73
	APPROVED	

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

CARD ASSEMBLY
TYPE PLL102-1,-2
LOW FREQ PHASE LOOP LOCK FILTER

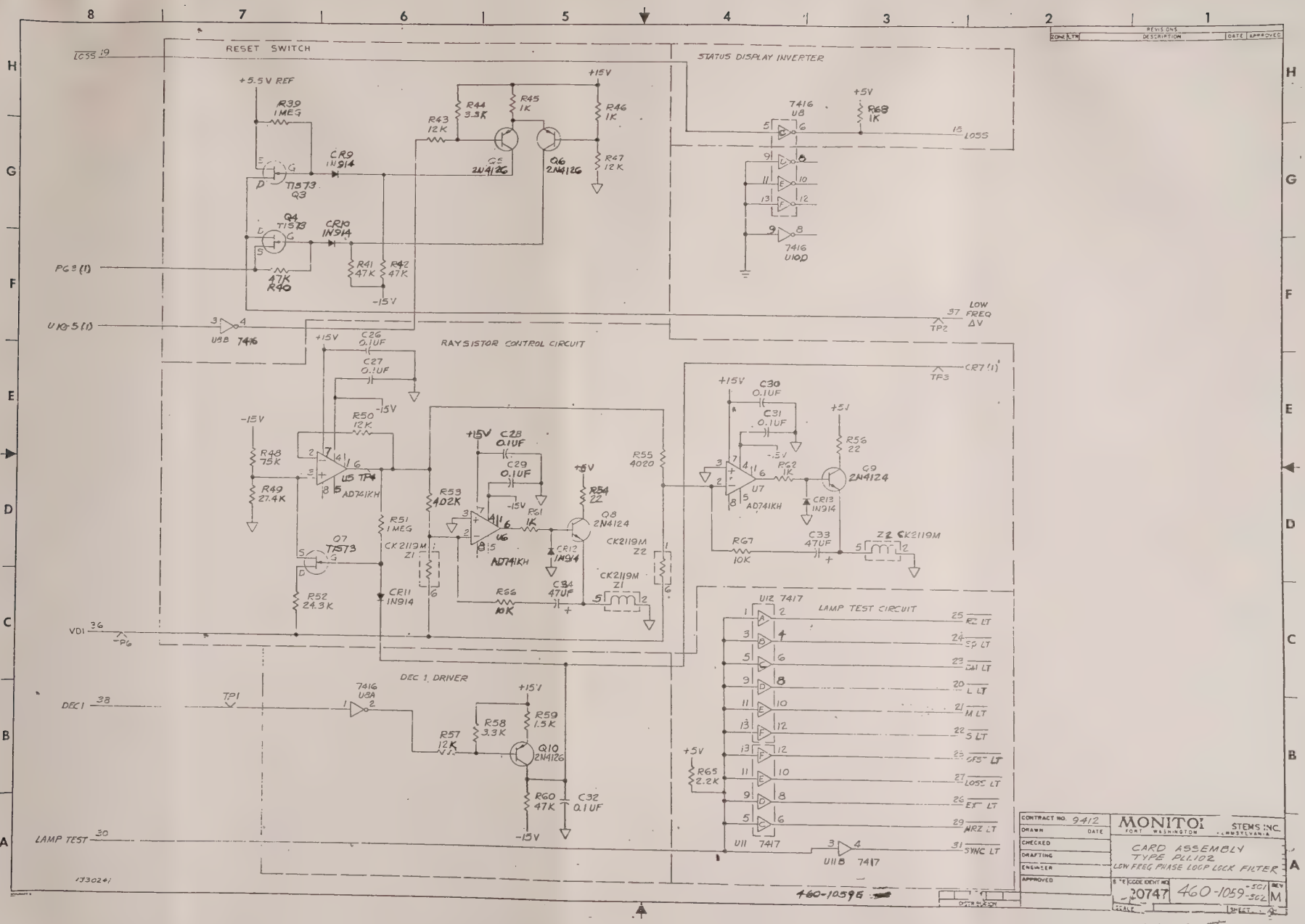
SIZE	CODE IDENT NO.		REV
C	20747	460-1059-501 502	M

SCALE NONE | SHEET 1 OF 4

NEXT ASSY	USED ON
9412	
APPLICATION	

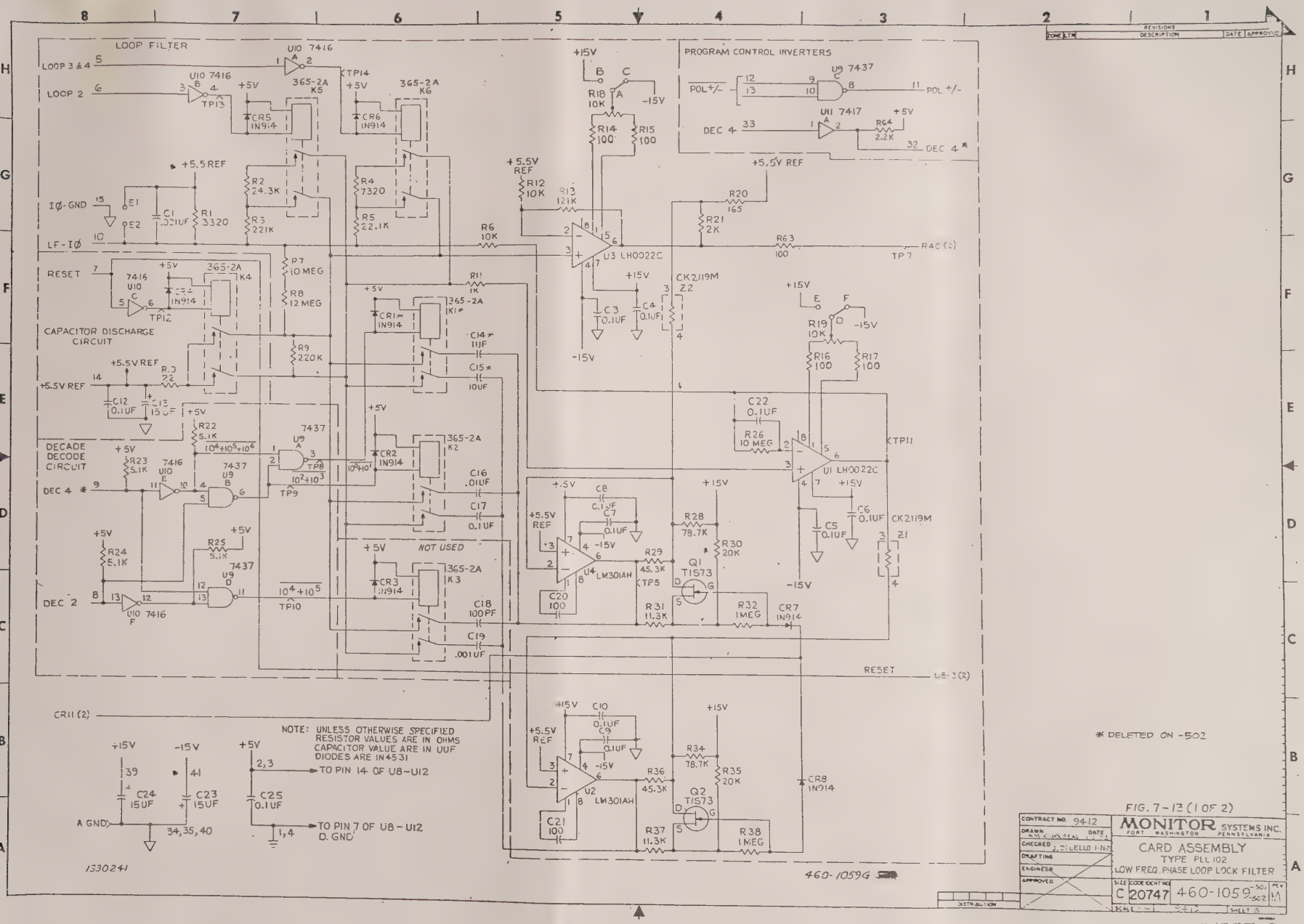
MONITOR SHOP STANDARDS ARE AN INTEGRAL PART OF THIS DRAWING (296-0077)

800-0187C

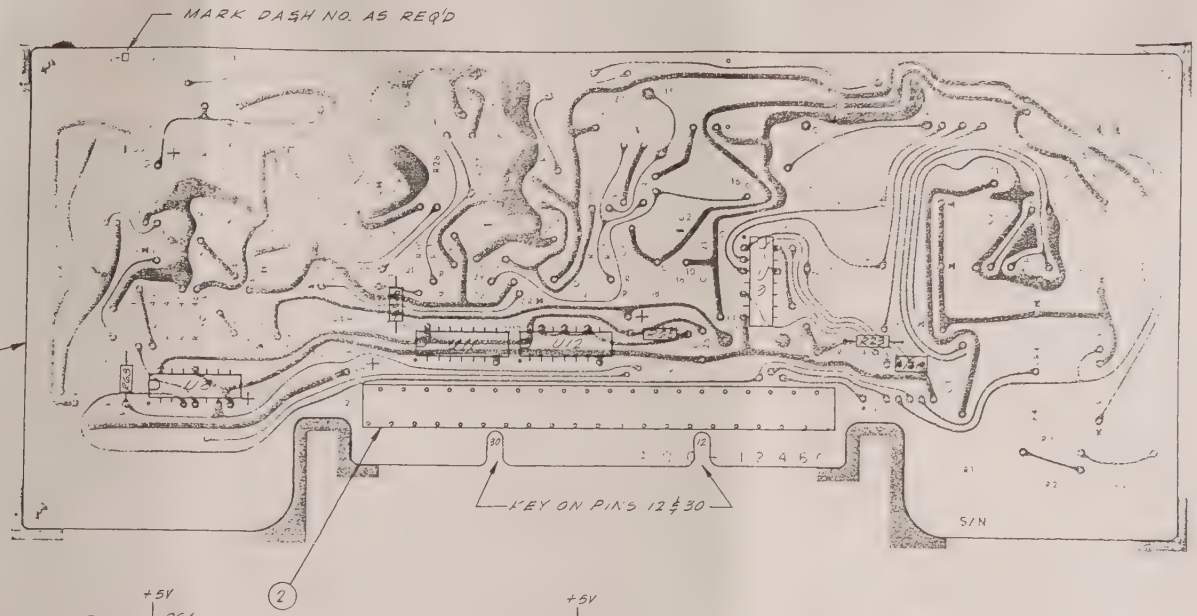


CONTRACT NO. 9412	MONITOR STEMS INC. FORT WASHINGTON, PENNSYLVANIA
DRAWN DATE	CARD ASSEMBLY TYPE PLL102 LOW FREQ PHASE LOOP LOCK FILTER
CHECKED	
DRAFTING	
ENGINEER	
APPROVED	CODE IDENT NO. 20747 — 460-1059-5C1 REV M
	SCALE — SHEET — OF

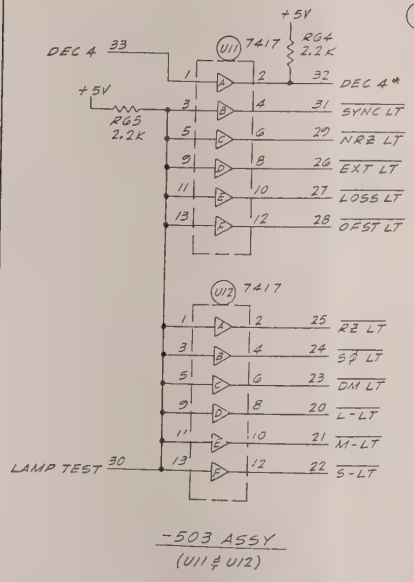
SHEET #2


LOOP FILTER
PROGRAM CONTROL INVERTERS
CAPACITOR DISCHARGE CIRCUIT
DECADE DECODE CIRCUIT
NOT USED
RESET
NOTE: UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS CAPACITOR VALUE ARE IN UUF DIODES ARE IN4531
TO PIN 14 OF U8-U12
TO PIN 7 OF U8 - U12
A GND
D. GND
1330241
460-1059G
* DELETED ON -502
FIG. 7-13 (1 OF 2)
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
TYPE PLL102
LOW FREQ. PHASE LOOP LOCK FILTER
460-1059-502
SHEET 3

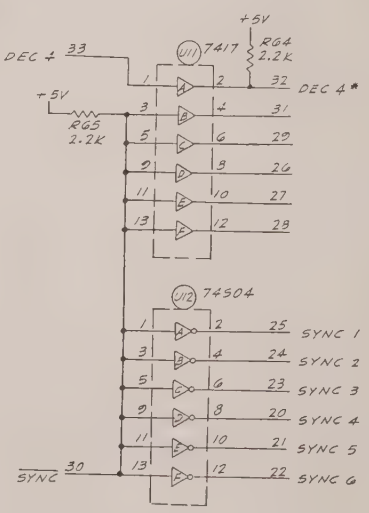
REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED



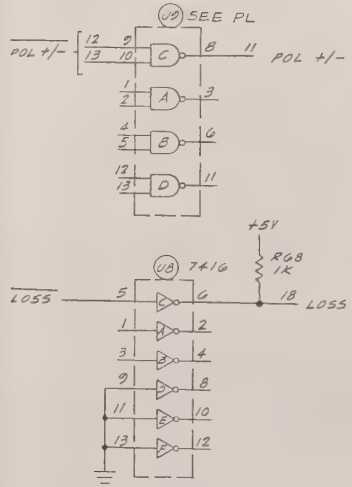
NOTES-
1- FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE A) 401-0010.



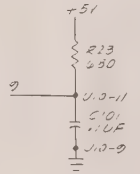
-503 ASSY
(U11 & U12)



-504 ASSY
(U11 & U12)



-503 & -504 ASSY
(U8)



FOR PARTS LIST SEE PL 460-1059-□

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501			LIST OF MATERIALS			

DRAWN	D. MACKLIN	DATE	5-11-76
CHECKED	E. STUCKER		5-10-76
DRAFTING	E. STUCKER		5-10-76
ENGINEER	C. BOYTIM		5-28-76
MFG	E. CODON		5-10-76
APPROVED	D. MOUAT		5-10-76
APPROVED	[illegible]		5/10/76

AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

CARD ASSEMBLY
TYPE PLL102-3&4
LOW FREQ PHASE LOCK LOOP FLT.

2932-4.0	
2700	
NEXT ASSY	USED ON
APPLICATION	

SIZE C | CODE IDENT NO. 20747 | 460-1059-503 504 | REV M

SCALE 2:1 | SHEET 4 OF 4

800-0684-1

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-1059		2-21-73	
C	REVISED PER ECO 460-1059		4-2-73	
D	REVISED PER ECO 460-1059		5-24-73	
E	REVISED PER ECO 460-1059		7-2-73	
F	REVISED PER ECO 460-1059F		2-15-75	
G	REVISED PER ECO 00639		3-5-75	
H	REVISED PER ECO 01494		6-14-76	
J	REVISED PER ECO 02886 BAKER		3-28-78	F. HINKLE
K	REVISED PER ECO 03328		4-26-78	D. MOUAT
L	REVISED PER ECO 03317 BAKER		6-18-78	F. HINKLE
M	REVISED PER ECO 03884		2-13-79	F Hinkle
N	REVISED PER ECO 04220		7-16-79	F. HINKLE
P	REVISED PER ECO 06312 JSG		4-23-81	R MARGRAFF
R	REVISED PER ECO 06068 CMT 4 SEPT 81		8 SEPT 81	R. Volz

NOTES

1.- C1 AND C19 MAY BE REPLACED WITH MONITOR PART 102-427-102, MFG. NO. 3419-100A-102M.

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	R	N	N	N	P	R																	

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
LOW FREQ PHASE LOOP LOCK FILTER
TYPE PLL102-1,-2,-3,-4

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	K HOUSEAL	1-5-73	ENGINEER	T. LOCASALE	2-21-73	DWG NO. PL460-1059-501 THRU 504	REV R
CHECKED	J. DILELLO	1-26-73	APPROVED				
DRAFTING	J. SAMPEDRO	3-2-73	MFG	R. HELLER	2-26-73	SHEET 1 OF 6	

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
–	–	–	REF	1	C	460-1059-501	———	20747	CARD ASS'Y & SCHEM.	
–	–	REF	–	2	C	460-1059-502	———	20747	CARD ASS'Y & SCHEM.	
–	REF	–	–	3	C	460-1059-503	———	20747	CARD ASS'Y & SCHEM.	
REF	–	–	–	4	C	460-1059-504	———	20747	CARD ASS'Y & SCHEM.	
				5						
1	1	1	1	6	C	400-1246	———	20747	BOARD, PRINTED WIRING	
				7						
1	1	1	1	8	A	108-203-041	7022-041-000-001	91662	CONN. FINGER BLOCK	
				9						
				10						
				11						
–	–	2	2	12	A	102-001-102	210B1B102	14752	CAP., .001UF, 100V, 20%	C1, C19 NOTE 1
–	–	1	1	13	A	102-121-SBT	DM15SBTJ0100WV4CR	72136	CAP., SBT, 100V, 5%	C2
–	–	18	18	14	A	102-419-104	8121M100651104M	72982	CAP., .1UF, 100V, 20%	C3-C10, C12, C22, C25-C32
–	–	1	1	15	A	102-121-SBT	DM15SBTJ0100WV4CR	72136	CAP., SBT, 100V, 5%	C11
–	–	3	3	16	A	102-305-156	150D156X0020B2	56289	CAP., 15UF, 20V, 20%	C13, C23, C24
–	–	–	1	17	A	102-015-105	X663F1059.50W2	84411	CAP., 1UF, 50V, 10%	C14
–	–	–	1	18	A	102-053-001	230B1B106K	14752	CAP., 10UF, 100V, 10%	C15
–	–	1	1	19	A	102-017-103	X663FR10391W2	84411	CAP., .01UF, 100V, 10%	C16
–	–	1	1	20	A	102-017-104	X663FR10491W2	84411	CAP., 0.1UF, 100V, 10%	C17
–	–	3	3	21	A	102-121-101	DM15102J0100WV4CR	72136	CAP., 100PF, 100V, 5%	C18, C20, C21
–	–	2	2	22	A	102-313-476	150D476X0006B2	56289	CAP., 47UF, 6V, 20%	C33, C34

DRAWN DATE	CHECKED DATE	TITLE PARTS LIST LOW FREQ PHASE LOOP LOCK FILTER, PLL102-☐	CODE IDENT NO. 20747	DWG NO. PL460-1059-☐ SHEET 2 OF	REV N

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
1	–	–	–	23	A	102-422-104	DG45BU104M	81349	CAP, .1UF, 50V, 20%	C101
				24						
–	–	–	13	25	A	104-014-001	IN914	03877	DIODE, IN914	CR1-CR13
–	–	12	–	26	A	104-014-001	IN914	03877	DIODE, IN914	CR2-CR13
				27						
				28						
–	–	–	6	29	A	106-016-001	365-2A	20891	RELAY, REED, 365-2A	K1-K6
–	–	5	–	30	A	106-016-001	365-2A	20891	RELAY, REED, 365-2A	K2-K6
				31						
				32						
–	–	5	5	33	A	103-604-001	TIS73	01295	TRANS., TIS73	Q1-Q4, Q7
–	–	3	3	34	A	103-304-001	2N4126	04713	TRANS., 2N4126	Q5, Q6, Q10
–	–	2	2	35	A	103-408-001	2N4124	04713	TRANS., 2N4124	Q8, Q9
				36						
				37						
–	–	1	1	38	A	100-215-3321	RN55D3321F	81349	RES., 3.32K, 1/10W, 1%	R1
–	–	2	2	39	A	100-215-2432	RN55D2432F	81349	RES., 24.3K, 1/10W, 1%	R2, R52
–	–	1	1	40	A	100-215-2213	RN55D2213F	81349	RES., 221K, 1/10W, 1%	R3
–	–	1	1	41	A	100-215-7321	RN55D7321F	81349	RES., 7.32K, 1/10W, 1%	R4
–	–	1	1	42	A	100-215-2212	RN55D2212F	81349	RES., 22.1K, 1/10W, 1%	R5
–	–	2	2	43	A	100-215-1002	RN55D1002F	81349	RES., 10K, 1/10W, 1%	R6, R12
–	–	2	2	44	A	100-003-106	RC07GF106J	81349	RES., 10MEG, 1/4W, 5%	R7, R26

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST LOW FREQ PHASE LOOP LOCK FILTER, PLL102-□	20747	PL460-1059-□ SHEET 3 of	N

800-0438A

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
–	–	1	1	45	A	100-003-126	RC07GF126J	81349	RES., 12 MEG, 1/4W, 5%	R8
–	–	1	1	46	A	100-003-224	RC07GF224J	81349	RES., 220K, 1/4W, 5%	R9
–	–	3	3	47	A	100-003-220	RC07GF220J	81349	RES., 22Ω, 1/4W, 5%	R10, R54, R56
–	–	1	1	48	A	100-215-1001	RN55D1001F	81349	RES., 1K, 1/10W, 1%	R11
–	–	1	1	49	A	100-215-1213	RN55D1213F	81349	RES., 121K, 1/10W, 1%	R13
–	–	4	4	50	A	100-003-101	RC07GF101J	81349	RES., 100Ω, 1/4W, 5%	R14-R17
–	–	2	2	51	A	101-115-103	77PR10K	73138	RES., VAR. 10K	R18, R19
–	–	1	1	52	A	100-215-1650	RN55D1650F	81349	RES., 165Ω, 1/10W, 1%	R20
–	–	1	1	53	A	100-215-2001	RN55D2001F	81349	RES., 2K, 1/10W, 1%	R21
–	–	4	4	54	A	100-003-512	RC07GF512J	81349	RES., 5.1K, 1/4W, 5%	R22-R25
–	–	1	1	55	A	100-003-SBT	RC07GFSBTJ	81349	RES., SBT, 1/4W, 5%	R27
–	–	2	2	56	A	100-215-7872	RN55D7872F	81349	RES., 78.7K, 1/10W, 1%	R28, R34
–	–	2	2	57	A	100-215-4532	RN55D4532F	81349	RES., 45.3K, 1/10W, 1%	R29, R36
–	–	2	2	58	A	100-215-2002	RN55D2002F	81349	RES., 20K, 1/10W, 1%	R30, R35
–	–	2	2	59	A	100-215-1132	RN55D1132F	81349	RES., 11.3K, 1/10W, 1%	R31, R37
–	–	4	4	60	A	100-003-105	RC07GF105J	81349	RES., 1MEG, 1/4W, 5%	R32, R38, R39, R51
–	–	1	1	61	A	100-003-SBT	RC07GFSBTJ	81349	RES., SBT, 1/4W, 5%	R33
–	–	4	4	62	A	100-003-473	RC07GF473J	81349	RES., 47K, 1/4W, 5%	R40-R42, R60
–	–	4	4	63	A	100-003-123	RC07GF123J	81349	RES., 12K, 1/4W, 5%	R43, R47, R50, R57
–	–	2	2	64	A	100-003-332	RC07GF332J	81349	RES., 3.3K, 1/4W, 5%	R44, R58
–	–	4	4	65	A	100-003-102	RC07GF102J	81349	RES., 1K, 1/4W, 5%	R45, R46, R61, R62
–	–	1	1	66	A	100-215-7502	RN55D7502J	81349	RES., 75K, 1/10W, 1%	R48

DRAWN DATE	CHECKED DATE	TITLE PARTS LIST LOW FREQ PHASE LOOP LOCK FILTER, PLL102-□	CODE IDENT NO. 20747	DWG NO. PL 460-1059-□ SHEET 4 OF	REV N

800-0438

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
–	–	1	1	67	A	100-215-2742	RN55D2742F	81349	RES., 27.4K, 1/10W, 1%	R49
–	–	2	2	68	A	100-215-4021	RN55D4021F	81349	RES., 4.02K, 1/10W, 1%	R53, R55
–	–	1	1	69	A	100-003-152	RC07GF152J	81349	RES., 1.5K, 1/4W, 5%	R59
–	–	1	1	70	A	100-003-101	RC07GF101J	81349	RES., 100Ω, 1/4W, 5%	R63
2	2	2	2	71	A	100-003-222	RC07GF222J	81349	RES., 2.2K, 1/4W, 5%	R64, R65
–	–	2	2	72	A	100-017-103	RC05GF103J	81349	RES., 10K, 1/8W, 5%	R66, R67
1	1	1	1	73	A	100-017-102	RC05GF102J	81349	RES., 1K, 1/8W, 5%	R68
1	–	–	–	74	A	100-003-681	RC07GF681J	81349	RES., 680Ω, 1/4W, 5%	R23
				75						
				76						
–	–	2	2	77	A	139-197-002	LH0022CH	27014	IC, AMP, LH0022CH	U1, U3 (SEE NOTE 3)
–	–	2	2	78	A	139-127-003	LM301AH	27014	IC, AMP, LM301AH	U2, U4
–	–	3	3	79	A	139-141-001	AD741KH	24355	IC, AMP, AD741KH	U5, U6, U7
–	–	2	2	80	A	139-046-416	SN7416N	01295	IC, TTL, SN7416N	U8, U10
–	1	1	1	81	A	139-046-437	SN7437N	01295	IC, TTL, SN7437N	U9
–	2	2	2	82	A	139-046-417	SN7417N	01295	IC, TTL, SN7417N	U11, U12
1	1	–	–	83	A	139-046-416	SN7416N	01295	IC, TTL	U8
1	–	–	–	84	A	139-046-417	SN7417N	01295	IC, TTL	U11
1	–	–	–	85	A	139-152-404	SN74S04N-10	01295	IC, TTL	U12
1	–	–	–	86	A	139-046-408	SN7408N	01295	IC, TTL	U9
				87						
–	–	2	2	88	A	139-140-001	CK2119M	49956	RAYSISTOR	Z1, Z2

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST LOW FREQ PHASE LOOP LOCK FILTER, PLL102-□	20747	PL460-1059-□ SHEET 5 OF	P

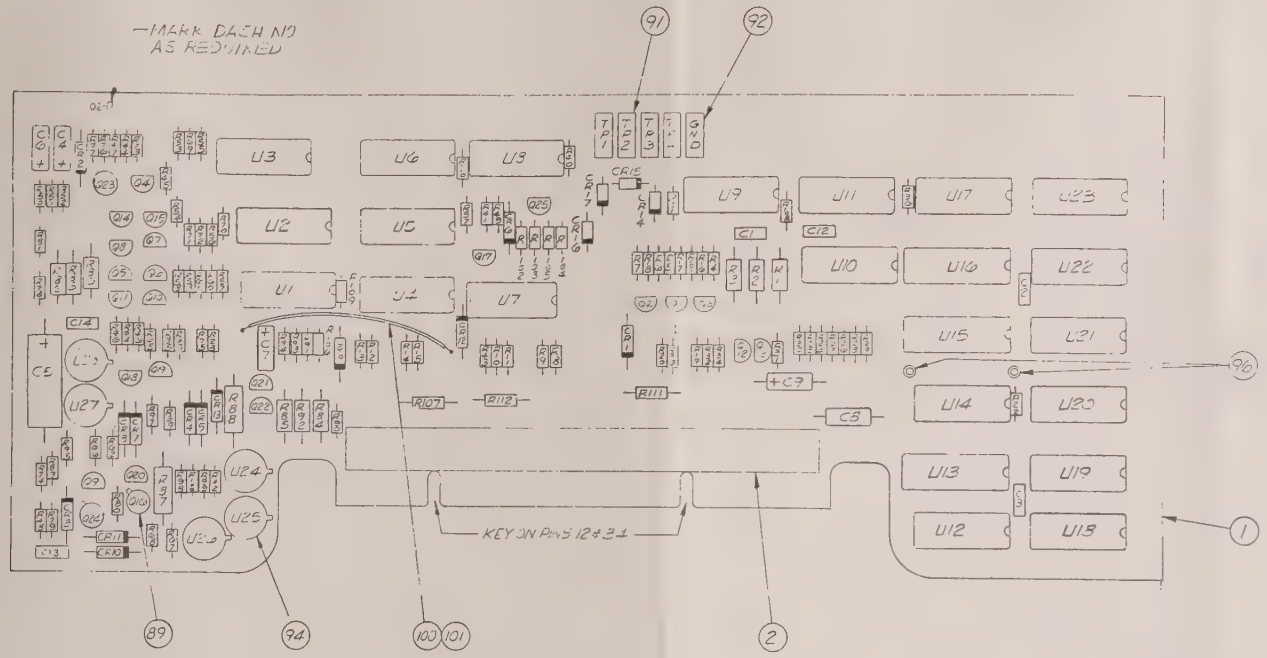
AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
–	–	14	14	89	A	121-202-005	8041-1G7	91506	JACK, TEST, GRN	1-14
–	–	1	1	90	A	121-202-009	8041-1G9	91506	JACK, TEST, WHT	A GND
				91						
				92						
–	–	1	1	93	A	131-200-002	2927-1-2	98159	STRAP, RUBBER, 2"	USE WITH C15
				94						
				95						
–	–	3	3	96	A	131-017-001	10229	07047	PAD, IC, 8 LEAD	USE WITH U5-U7
–	–	2	2	97	A	131-015-001	10037	07047	PAD, IC, 6 LEAD	USE WITH Z1, Z2
–	–	2	2	98	A	131-020-001	10284-N	07047	PLASTIC COVER, TO-5	USE WITH Z1, Z2
				99						
–	–	2	2	100	A	121-315-005	7009-265-5	17117	SOCKET, 8 PIN, TO-5 (NOTE 3)	USE WITH U1, U3
				101						
				102						
–	–	2	2	103	A	118-005-003	1604-2-05	71279	TERMINAL, TURRET	E1, E2
				104						
				105						
–	–	AR	AR	106	A	113-001-004	298	92194	WIRE, BUS, #22 AWG	
–	–	AR	AR	107	A	114-001-004	———	03890	TUBING, TEF, #22 WHT	
				108						
				109						
AR	AR	AR	AR	110	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST LOW FREQ PHASE LOOP LOCK FILTER, PLL102-□	20747	PL 460-1059-□ SHEET 6 OF	R

800-043

ZONE	LTR	REVISIONS DESCRIPTION		DATE	APPROVED
		6 TO 4 SEE PIL FOR ECO NES			
	J	REVISED PER ECO 04453	JSG	9-25-79	[illegible]
	K	ADDED -503 PER ECO 04675	JST	12-7-79	[illegible]
	L	[illegible]		9-28-81	ES
	M	REVISED PER ECO 08133	WKH 12-21-82	5 Jan 83	RS Vulz
	N	REVISED PER ECO 08290	JSG	[illegible]	[illegible]
	P	REVISED PER ECO 08348	WKH 4-4-83	[illegible]	[illegible]



CSD002-1 & -2

NOTES:

1. FOR -502 ASSY., R28 THRU R31 ARE REPLACED WITH JUMPERS, USING ITEMS 100 & 101 .

FOR SCHEMATIC SEE 600-0335-1,-2
FOR PARTS LIST SEE PL460-1095-☐

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501	LIST OF MATERIALS					

DRAWN N. GOODMAN DATE 7-17-73
CHECKED ES
DRAFTING E. STUCKER
ENGINEER L. KOEHLER
MFG G.L. BROWN
APPROVED R. CLEGG 7-23-73
APPROVED

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA 19034

CARD ASSEMBLY
TYPE CSD002-1,-2
COUNTDOWN LOGIC & SYNC DET.

NEXT ASSY	USED ON
	4300
APPLICATION	

SIZE D | CODE IDENT NO 20747 | 460-1095-501 502 | REV P
SCALE 2:1 | SHEET 1 OF 2

800 0F64-1

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 1095B		2-11-74	~~~
C	REVISED PER ECO 01930		1-21-77	~~~
D	REVISED PER ECO 02859			J MATHER
E	REVISED PER ECO 03242		52473	D. MOUAT
F	REVISED PER ECO 03292 BAKER 6-20-78		6-21-78	R. SNEDEKER
G	REVISED PER ECO 03565		9/21/78	R. Valentine
H	REVISED PER ECO 03619 J.K		10/9/78	[illegible]
J	REVISED PER ECO 04459 JSG		9-25-79	[illegible]
K	REVISED PER ECO 04675 JST		12-7-79	[illegible]
L	REVISED PER ECO 04792		9-29-80	ES
M	REVISED PER ECO 08348 WKH 4-4-83		4/7/83	[illegible]

NOTE 2
139-198-490 IS PREFERRED PART.
139-097-490 IS ALTERNATE PART.

NOTE 1
R81 IS A SBT WITH A NOMINAL VALUE OF 3.9K, 1/3W, 5%

SCHEMATIC: D) 600-0335-1

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	M	L	L	L	L																		

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE CARD ASSEMBLY
COUNTDOWN LOGIC & SYNC DET
CSD002-1

CODE IDENT 20747
CONTRACT NO. 4000

DRAWN	H. GOODMAN	7-17 73	ENGINEER	J. KOEHLER		DWG NO. PL 460-1095-501	REV M
CHECKED	ES		APPROVED	R. CLEGG	7-17 73		
DRAFTING	E. STUCKER		MANUF.	G.L. BROWN	7-17 73	SHEET 1 OF 5	

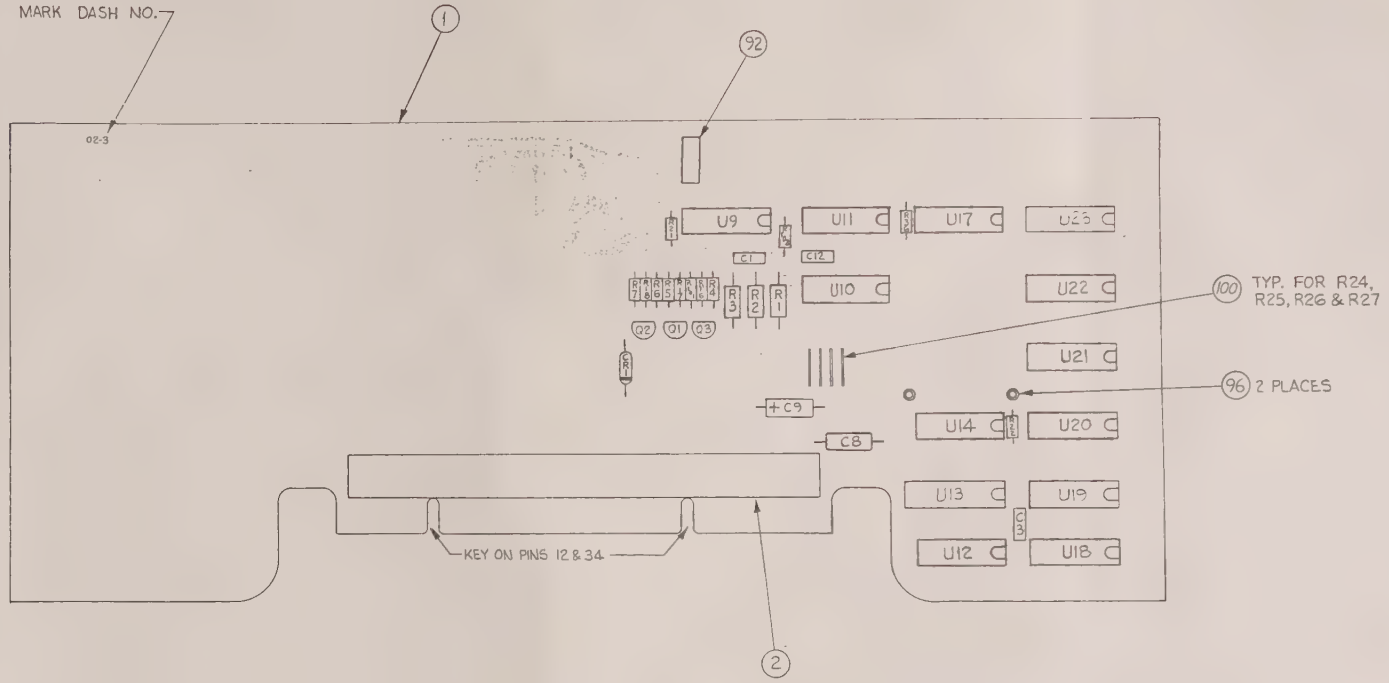
800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		460-1095-501		M	PARENT CSD002-1	
1	001	400-1254			BOARD P.W. DUMBO	
1	002	108-203-041	7022-041-000001	C	CONN FING BLOC 41 POS	
6	005	102-419-104	CY30A104M		CAP .1UF 100V 20%	C1
						C2
						C3
						C12
						C13
1	006	102-369-106	T330C106M035AS		CAP 10UF 35V 20%	C14
1	007	102-306-107	150D107X0010R2		CAP 100UF 10V 2%	C4
2	008	102-369-105	T330B105M035AS		CAP 1UF 35V 20% TANT	C5
						C6
1	009	102-001-473	230B1B473	H	CAP .047UF 100V 20%	C7
1	010	102-313-685	150D685X0006A2		CAP 6.8UF 6V 20%	C8
1	013	104-056-111	1N752A	P	DIODE ZENER CASE 51	C9
11	014	104-014-001	1N914	B	DIODE SILICON DO-7	CR1
						CR2
						CR3
						CR4
						CR5
						CR6
						CR7
						CR8
						CR9
						CR10
						CR11
1	015	104-056-102	IN749A	P	DIODE ZENER CASE 51	CR12
4	016	104-503-014	1N4531	F	DIODE SIG MINIATURE	CR13
						CR14
						CR15
						CR16
						CR17
1	017	139-051-420	SN74H20N-10	L	IC TTL 14 PIN	U1
2	018	139-051-410	SN74H10N-10	L	IC TTL 14 PIN	U2
2	019	139-085-107	SN75107AN-10	A/E	IC LINE RECVR 14 PIN	U3
						U4
1	020	139-051-400	SN74H00N-10	L	IC TTL 14 PIN	U7
1	021	139-046-404	SN7404N-10	A/P	IC TTL 14 PIN	U5
1	022	139-051-453	SN74H53N-10	L	IC TTL 14 PIN	U8
1	023	139-051-404	SN74H04N-10	L	IC TTL 14 PIN	U9
1	024	139-046-197	SN74197N-10	A/P	IC TTL 14 PIN	U10
5	025	139-198-490	74LS90	A/B	IC TTL 14 PIN (NOTE 2)	U11
						U12
						U18
						U19
						U20
1	026	139-046-151	139-217-151	A/P	IC TTL 16 PIN	U21
1	027	139-051-474	SN74H74N-10	L	IC TTL 14 PIN	U13
2	028	139-046-153	SN74153N-10	A/P	IC TTL 16 PIN	U14
						U15
2	029	139-051-103	SN74H103N-10	L	IC TTL 14 PIN	U16
						U17
2	030	139-051-411	SN74H11N-10	L	IC TTL 14 PIN	U22
						U23
						U6

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
5	031	139-141-001	AD741KH	E	IC OP AMP 8 PIN TO-99	U24
						U25
						U26
						U27
						U28
1	034	100-215-1182	RN55D1182F		RES 11.8K 1/8W 1%	R1
1	035	100-215-1961	RN55D1961F		RES 1.96K 1/8W 1%	R2
1	036	100-215-1210	RN55D1210F		RES 121 1/8W 1%	R3
2	037	100-215-4991	RN55D4991F		RES 4.99K 1/8W 1%	R83
						R84
1	038	100-215-2211	RN55D2211F		RES 2.21K 1/8W 1%	R86
1	039	100-003-121	RC07GF121J	D	RES 120 OHMS 1/4W 5%	R87
1	040	100-215-2321	RN55D2321F		RES 2.32K 1/8W 1%	R92
2	041	100-017-271	RC05GF271J		RES 270 1/8W 5%	R4
						R5
10	042	100-017-750	RC05GF750J		RES 75 1/8W 5%	R6
						R7
						R8
						R9
						R10
						R11
						R12
						R13
						R14
						R15
1	044	100-017-153	RC05GF153J		RES 15K 1/8W 5%	R21
1	045	100-017-222	RC05GF222J		RES 2.2K 1/8W 5%	R23
8	046	100-017-471	RC05GF471J		RES 470 1/8W 5%	R24
						R25
						R26
						R27
						R28
						R29
						R30
						R31
2	048	100-017-101	RC05GF101J		RES 100 1/8W 5%	R32
						R33
2	049	100-017-332	RC05GF332J		RES 3.3K 1/8W 5%	R34
						R35
1	050	100-005-221	RC20		RES 220 1/2W 5%	R88
1	051	100-017-221	RC05GF221J		RES 220 1/8W 5%	R102
10	052	100-017-102	RC05GF102J		RES 1K 1/8W 5%	R36
						R37
						R39
						R40
						R41
						R42
						R43
						R96
						R109
						R110
5	054	100-017-472	RC05GF472J		RES 4.7K 1/8W 5%	R44
						R45
						R46
						R75

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
3	056	100-017-473	RC05GF473J		RES 47K 1/8W 5%	R103
						R47
						R48
19	057	100-017-151	RC05GF151J		RES 150 1/8W 5%	R49
						R50
						R51
						R52
						R53
						R54
						R55
						R56
						R57
						R58
						R59
						R60
						R61
						R62
						R63
						R64
						R65
						R66
						R67
4	058	100-017-511	RC05GF511J		RES 510 1/8W 5%	R68
						R69
						R70
						R71
4	060	100-017-272	RC05GF272J		RES 2.7K 1/8W 5%	R72
						R73
						R74
						R104
5	062	100-017-105	RC05GF105J		RES 1MEG 1/8W 5%	R105
						R76
						R77
						R78
						R79
1	064	100-215-1002	RN55D1002F			R80
1	065	100-017-220	RC05GF220J		RES 10K 1/8W 1%	R82
2	066	100-003-152	RC07		RES 22 1/8W 5%	R89
				D	RES 1.5K 1/4W 5%	R111
2	067	100-017-104	RC05GF104J			R112
					RES 100K 1/8W 5%	R91
1	068	100-017-331	RC05GF331J			R93
1	069	100-017-103	RC05GF103J		RES 330 1/8W 5%	R94
1	070	100-017-302	RC05GF302J		RES 10K 1/8W 5%	R95
1	071	100-017-242	RC05GF242J		RES 3K 1/8W 5%	R97
1	072	100-017-112	RC05GF112J		RES 2.4K 1/8W 5%	R98
1	073	100-017-122	RC05GF122J		RES 1.1K 1/8W 5%	R99
1	074	100-003-151	RC07		RES 1.2K 1/8W 5%	R100
1	075	100-017-SBT	RC05	D	RES 150 OHMS 1/4W 5%	R107
2	076	100-017-392	RC05GF392J		RES SBT 1/8W 5%	R106
					RES 3.9K 1/8W 5% (NOTE 1)	R90
1	077	100-017-912	RC05GF912J			R81
1	078	100-215-4531	RN55D4531F		RES 9.1K 1/8W 5%	R23
7	079	100-017-470	RC05GF470J		RES 4.53K 1/8W 1%	R85
					RES 47 1/8W 5%	R108
						R101

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						R16
						R17
						R18
						R19
						R20
2	082	103-438-001	2N5771	E	TRANS UHS PNP TO-92	Q1
						Q2
10	083	103-304-001	2N4126	D	TRANS SIL PNP TO-92	Q3
						Q4
						Q5
						Q6
						Q7
						Q8
						Q9
						Q10
						Q11
						Q25
10	084	103-408-001	2N4124	C	TRANS SIL NPN TO-92	Q12
						Q13
						Q14
						Q15
						Q17
						Q18
						Q19
						Q20
						Q21
						Q22
2	086	103-350-002	2N4857	B	TRANS FET TO-18	Q23
						Q24
1	087	103-019-001	2N2222	B	TRANS SIL NPN TO-18	Q16
3	089	131-013-001	10047	B	PAD TRANS TO 18 4 PIN	
4	091	121-202-005	SPCJ-200-05	K	TEST POINT PC GRN	TP1
						TP2
						TP3
						TP4
1	092	121-202-010	SPCJ-200-03	K	TEST POINT PC BLK	GND
5	094	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	
2	096	118-005-003	1604-2-05	B	TERMINAL TURRET SLDR	A
						B
1	100	113-001-006	299/1	C	WIRE BUS 26 AWG	
1	101	114-001-006	SIZE 26 WHITE	J	TUBING TEF 26 AWG WHT	

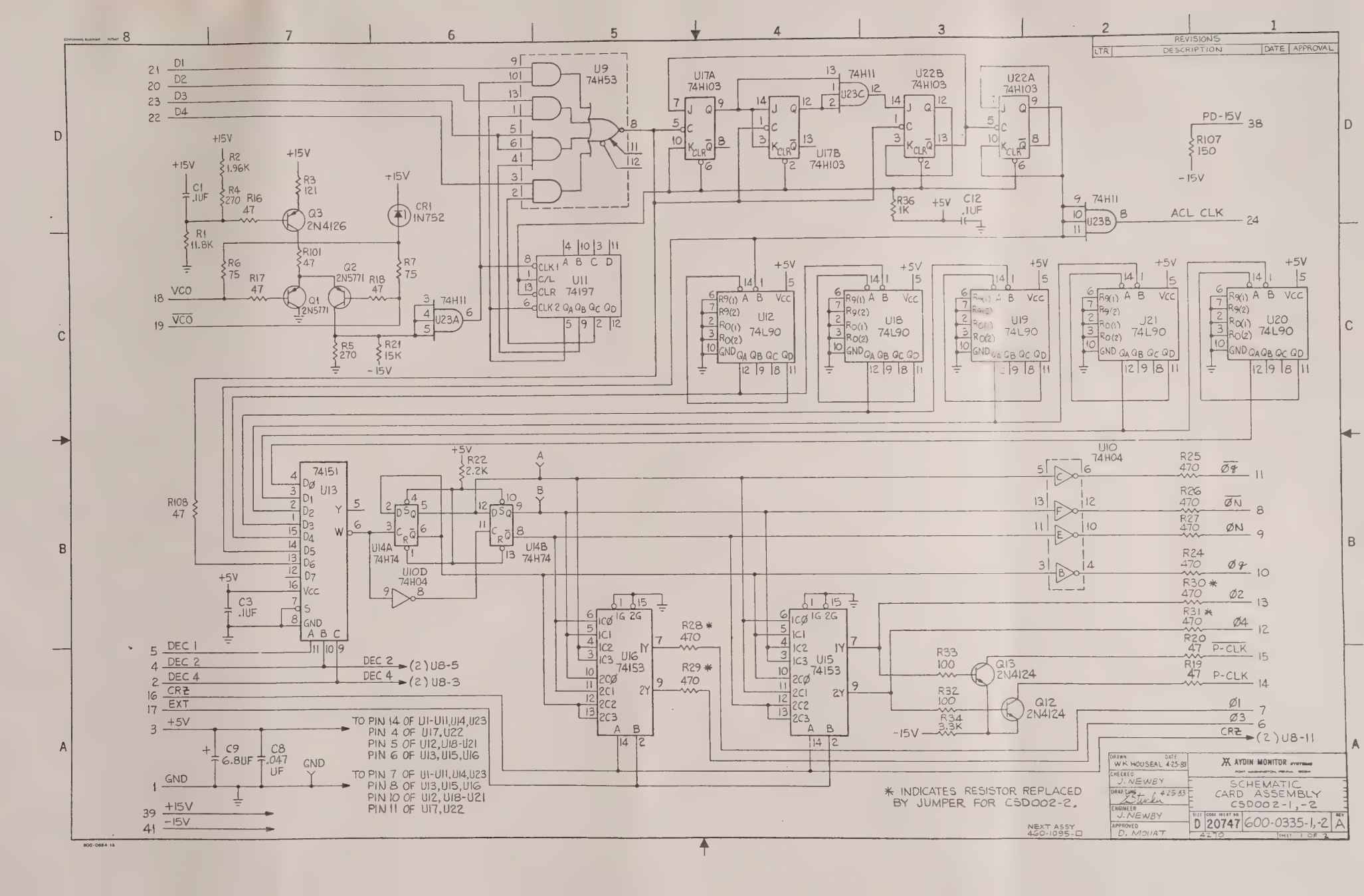


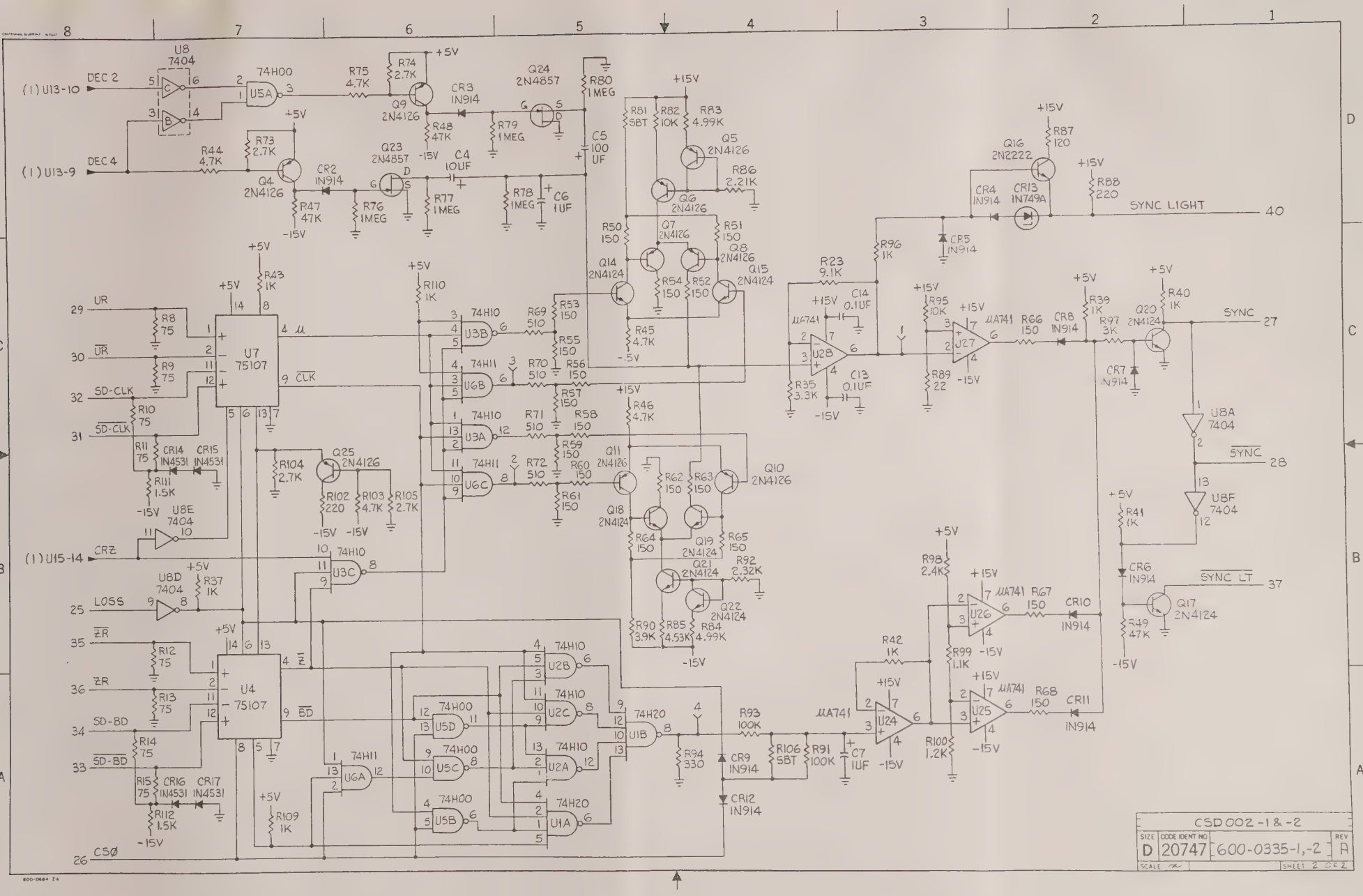
CSD002-3

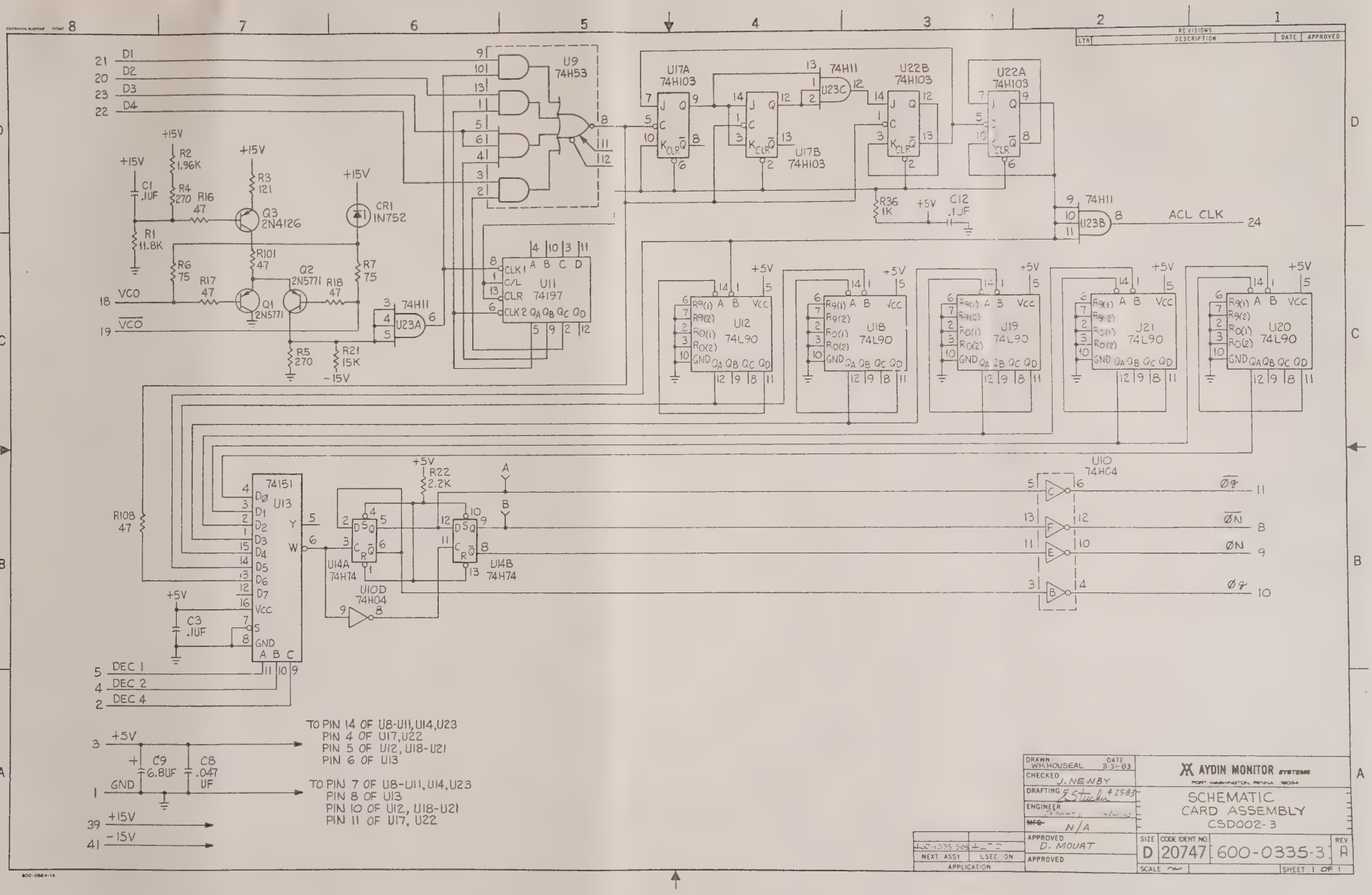
FOR SCHEMATIC SEE 600-0335-3
FOR PARTS LIST SEE PL 460-1095-503

CSD002-3			
SIZE	CODE IDENT NO		REV
D	20747	460-1095-503	P
SCALE 2/1		SHEET 2	

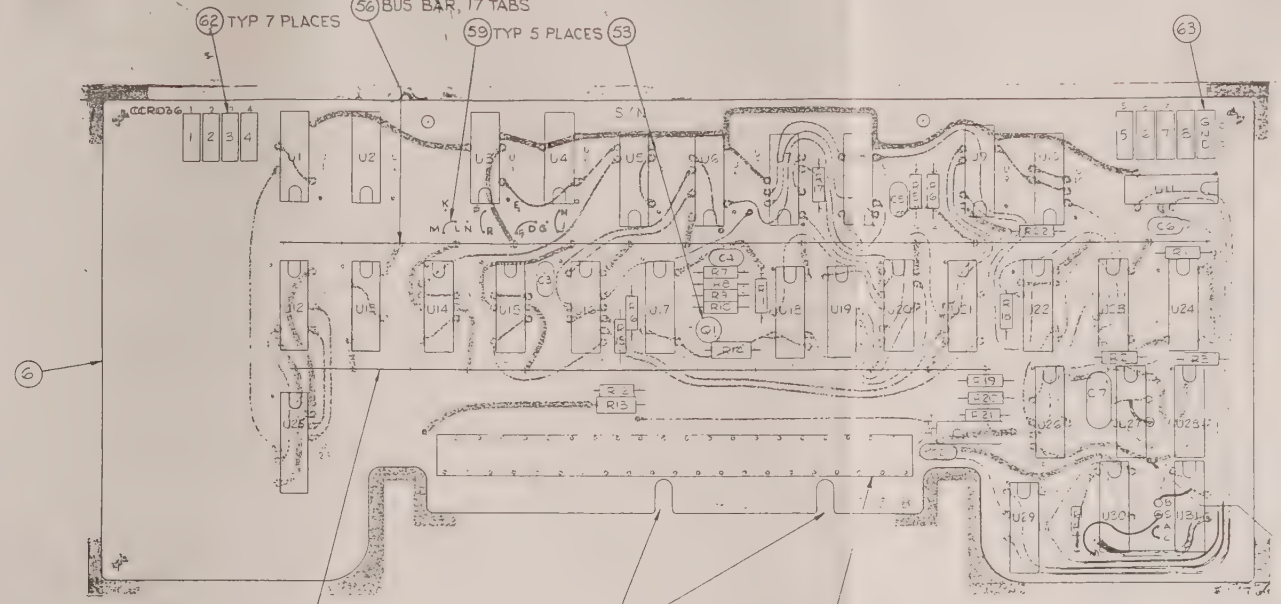
800 0684-24


REVISIONS
LTR DESCRIPTION DATE APPROVAL
D1
D2
D3
D4
U9 74H53
U17A 74H103
U17B 74H103
U22B 74H103
U22A 74H103
74H11 U23C
PD-15V 38
R107 150
-15V
R36 1K
+5V
C12 .1UF
74H11 U23B
ACL CLK 24
+15V
C1 .1UF
R2 1.96K
R4 270
R16 47
R3 121
Q3 2N4126
CR1 1N752
R1 11.8K
R6 75
R17 47
R101 47
Q2 2N5771
Q1 2N5771
R18 47
R7 75
R5 270
R21 15K
VCO
VCO
74H11 U23A
U11 74197
U12 74L90
U18 74L90
U19 74L90
U21 74L90
U20 74L90
R108 47
74151 U13
R22 2.2K
U14A 74H74
U14B 74H74
U10D 74H04
C3 .1UF
U10 74H04
R25 470 Ø8
R26 470 ØN
R27 470 ØN
R24 470 Ø9
R30 * 470 Ø2
R31 * 470 Ø4
R20 47 P-CLK
R19 47 P-CLK
Ø1
Ø3
CR7
(2) U8-11
U16 74153
U15 74153
R28 * 470
R29 * 470
R33 100
R32 100
R34 3.3K
Q13 2N4124
Q12 2N4124
DEC 1
DEC 2
DEC 4
CR7
EXT
DEC 2 (2) U8-5
DEC 4 (2) U8-3
+5V
GND
C9 6.8UF
C8 .047 UF
TO PIN 14 OF U1-U11,U14,U23
PIN 4 OF U17,U22
PIN 5 OF U12,U18-U21
PIN 6 OF U13,U15,U16
TO PIN 7 OF U1-U11,U14,U23
PIN 8 OF U13,U15,U16
PIN 10 OF U12,U18-U21
PIN 11 OF U17,U22
+15V
-15V
* INDICATES RESISTOR REPLACED BY JUMPER FOR CSD002-2.
NEXT ASSY 460-1095-□
DRAWN W.K HOUSEAL 4-25-83
CHECKED J. NEWBY
DRAFTING 4-25-83
ENGINEER J. NEWBY
APPROVED D. MOUAT
AYDIN MONITOR
SCHEMATIC CARD ASSEMBLY CSD002-1,-2
SIZE D CODE IDENT NO 20747 600-0335-1,-2 REV A
SHEET 1 OF 3


(1) U13-10
DEC 2
(1) U13-9
DEC 4
U8 7404
74H00
U5A
R74 2.7K
R75 4.7K
+5V
Q9 2N4126
CR3 IN914
Q24 2N4857
R80 1MEG
R48 47K
R79 1MEG
-15V
C5 100 UF
R73 2.7K
R44 4.7K
Q4 2N4126
CR2 IN914
Q23 2N4857
C4 10UF
R47 47K
R76 1MEG
R77 1MEG
R78 1MEG
C6 1UF
+15V
R81 SBT
R82 10K
R83 4.99K
Q5 2N4126
Q6 2N4126
R86 2.21K
R50 150
Q7 2N4126
R51 150
Q8 2N4126
Q14 2N4124
Q15 2N4124
R54 150
R52 150
R45 4.7K
R87 120
Q16 2N2222
CR4 IN914
CR13 IN749A
R88 220
SYNC LIGHT
40
CR5 IN914
R96 1K
R23 9.1K
C14 0.1UF
C13 0.1UF
μA741
U28
R35 3.3K
R95 10K
U27
R89 22
R66 150
CR8 IN914
R39 1K
R97 3K
Q20 2N4124
R40 1K
SYNC
27
CR7 IN914
U8A 7404
SYNC
28
U8F 7404
R41 1K
CR6 IN914
SYNC LT
37
Q17 2N4124
R49 47K
29 UR
30 UR
32 SD-CLK
31 SD-CLK
R8 75
R9 75
R10 75
R11 75
CR14 IN4531
CR15 IN4531
R111 1.5K
U7 75107
9 CLK
4 μ
R43 1K
R110 1K
74H10
U3B
U6B
U3A
U6C
74H11
R69 510
R70 510
R71 510
R72 510
R53 150
R55 150
R56 150
R57 150
R58 150
R59 150
R60 150
R61 150
R46 4.7K
Q10 2N4126
Q11 2N4126
Q18 2N4124
Q19 2N4124
Q21 2N4124
Q22 2N4124
R62 150
R63 150
R64 150
R65 150
R92 2.32K
R90 3.9K
R85 4.53K
R84 4.99K
Q25 2N4126
R104 2.7K
R102 220
R103 4.7K
R105 2.7K
U8E 7404
(1) U15-14
CRZ
U8D 7404
R37 1K
25 LOSS
35 ZR
36 ZR
34 SD-BD
33 SD-BD
R12 75
R13 75
R14 75
R15 75
CR16 IN4531
CR17 IN4531
R112 1.5K
U4 75107
9 BD
8 Z
R109 1K
26 CSØ
74H00
U5D
U5C
U5B
74H11
U6A
74H10
U2B
U2C
U2A
74H20
U1B
U1A
R94 330
CR9 IN914
CR12 IN914
R93 100K
R106 SBT
R91 100K
C7 1UF
μA741
U24
R42 1K
R98 2.4K
U26
R99 1.1K
R67 150
CR10 IN914
R100 1.2K
U25
R68 150
CR11 IN914
CSD 002-1 & -2
SIZE D
CODE IDENT NO 20747
600-0335-1,-2
REV A
SCALE
SHEET 2 OF 2

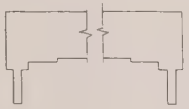


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
D1
D2
D3
D4
U9
74H53
U17A
74H103
U17B
74H103
U22B
74H103
U22A
74H103
74H11
U23C
U23B
ACL CLK
R36
1K
C12
.1UF
+15V
R2
1.96K
R4
270
R16
47
R3
121
Q3
2N4126
CR1
1N752
C1
.1UF
R1
11.8K
R6
75
R17
47
R101
47
Q2
2N5771
R18
47
R7
75
Q1
2N5771
VCO
VCO
R5
270
R21
15K
-15V
74H11
U23A
U11
74197
CLK1
C/L
CLR
CLK2
U12
74L90
U18
74L90
U19
74L90
U21
74L90
U20
74L90
R9(1)
R9(2)
R0(1)
R0(2)
GND
VCC
74151
U13
R108
47
C3
.1UF
DEC 1
DEC 2
DEC 4
R22
2.2K
U14A
74H74
U14B
74H74
U10D
74H04
U10
74H04
Ø9
ØN
ØN
Ø9
C9
6.8UF
C8
.047
UF
GND
TO PIN 14 OF U8-U11, U14, U23
PIN 4 OF U17, U22
PIN 5 OF U12, U18-U21
PIN 6 OF U13
TO PIN 7 OF U8-U11, U14, U23
PIN 8 OF U13
PIN 10 OF U12, U18-U21
PIN 11 OF U17, U22
DRAWN WK HOUSEAL DATE 3-31-83
CHECKED J. NEWBY
DRAFTING E. Stucker 4-25-83
ENGINEER
MFG N/A
APPROVED D. MOUAT
APPROVED
NEXT ASSY
USED ON
APPLICATION
AYDIN MONITOR SYSTEMS
PORT WASHINGTON, PENNA 19034
SCHEMATIC
CARD ASSEMBLY
CSD002-3
SIZE D
CODE IDENT NO. 20747
600-0335-3
REV A
SCALE
SHEET 1 OF 1



JUMPER OPTION	COUNT
A-C	128
A-B	252
A-S	512

TYPICAL END CUTS ON BUS BAR



NOTES:-
1.-FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG NO. 401-0010.

REVISIONS					
ZONE	LTR	DESCRIPTION		DATE	APPROVED
	B	REVISED PER ECO 460-0982B		8-72	[illegible]
	C	REVISED PER ECO 460-0982C	TAP	9-27-72	[illegible]
	D	REVISED PER ECO 460-0982C-D	RMS	9-29-72	[illegible]
	E	REVISED PER ECO 460-0982E	TMB	8-74	[illegible]
	F	REVISED PER ECO 460-0982F	TMB	2-25-74	[illegible]
	G	REVISED PER ECO 00772	DSM	5-[illegible]	[illegible]
	M	REVISED PER ECO 02267	NRW	[illegible]	[illegible]
	J	REVISED PER ECO 04220	FTB	7-2-79	[illegible]

FOR PARTS LIST SEE PL460-0982-☐

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501			LIST OF MATERIALS			

DRAWN	J. DILELLO	DATE 9-8-72
CHECKED	W.K.H 9-27-72 / L.S.G 9-11-72	
DRAFTING	J. SAMPEDRO	10-25-72
ENGINEER	R. WASSERMAN	10-17-72
MFG	L. MILEDOWSKI	11-30-72
APPROVED	R. CLEGG	10-25-72
APPROVED		

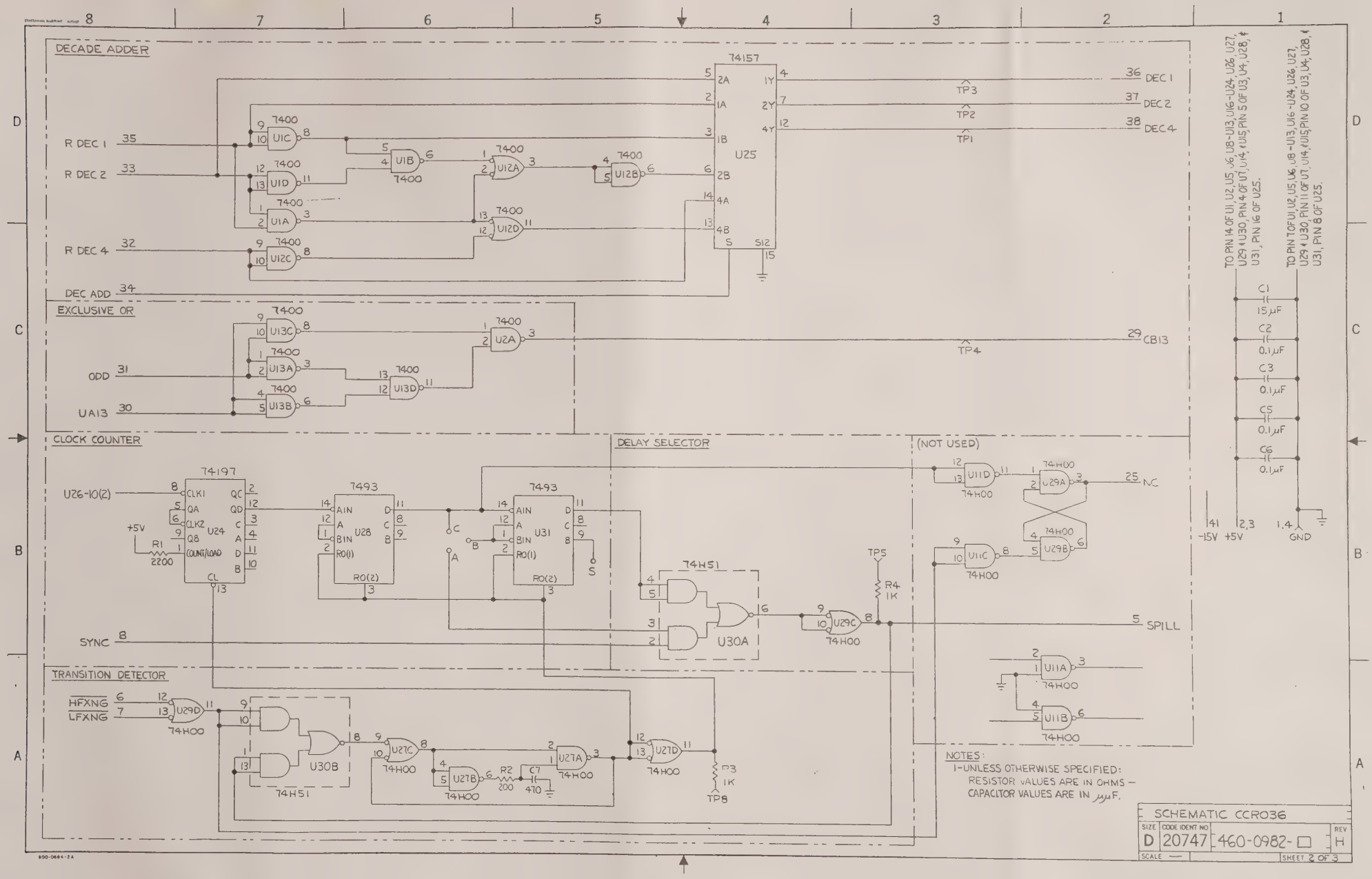
XX AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

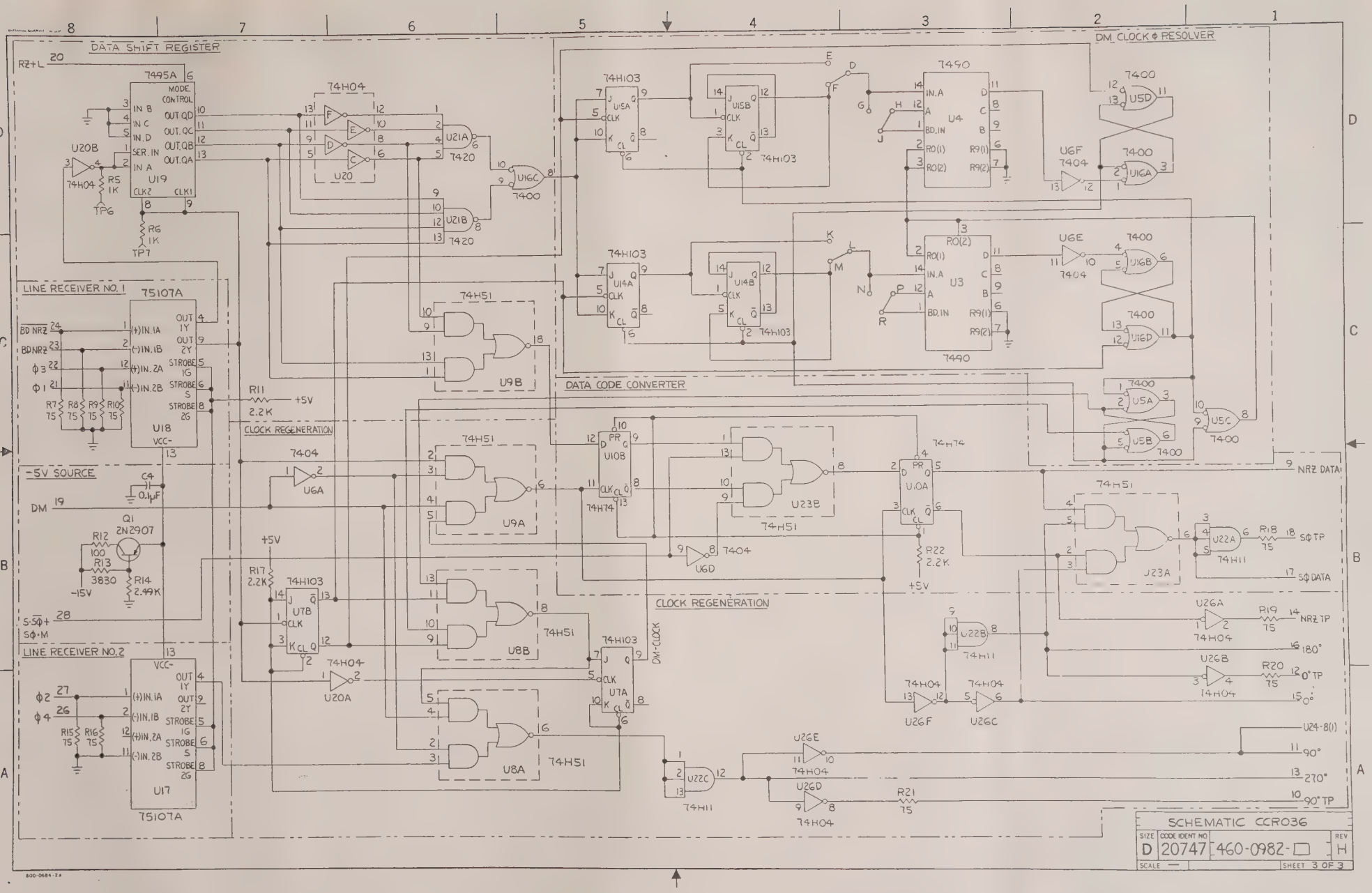
CARD ASSEMBLY
CODE CONVERTER
CCR036-☐

NEXT ASSY	USED ON
	9412
APPLICATION	

SIZE	CODE IDENT NO		REV
D	20747	460-0982-☐	J
SCALE 2/1		SHEET 1 OF 3	

800-0684-1


DECADE ADDER
74157
U25
R DEC 1
R DEC 2
R DEC 4
DEC ADD
DEC 1
DEC 2
DEC 4
TP3
TP2
TP1
EXCLUSIVE OR
ODD
UA13
CB13
TP4
CLOCK COUNTER
74197
U24
U26-10(2)
SYNC
7493
U28
U31
DELAY SELECTOR
74H51
U30A
U30B
TP5
R4 1K
SPILL
(NOT USED)
NC
TRANSITION DETECTOR
HFXNG
LFXNG
R1 220Ω
R2 200
C7 470
R3 1K
TP8
TO PIN 14 OF U1, U2, U5, U6, U8-U13, U16-U24, U26, U27, U29 & U30, PIN 4 OF U7, U14, & U15, PIN 5 OF U3, U4, U28, & U31, PIN 16 OF U25.
TO PIN 7 OF U1, U2, U5, U6, U8-U13, U16-U24, U26, U27, U29 & U30, PIN 11 OF U7, U14, & U15, PIN 10 OF U3, U4, U28, & U31, PIN 8 OF U25.
C1 15µF
C2 0.1µF
C3 0.1µF
C5 0.1µF
C6 0.1µF
-15V
+5V
GND
NOTES:
1-UNLESS OTHERWISE SPECIFIED:
RESISTOR VALUES ARE IN OHMS —
CAPACITOR VALUES ARE IN µµF.
SCHEMATIC CCR036
SIZE D
CODE IDENT NO 20747
460-0982-□
REV H
SCALE —
SHEET 2 OF 3


DATA SHIFT REGISTER
DM CLOCK Φ RESOLVER
DATA CODE CONVERTER
CLOCK REGENERATION
LINE RECEIVER NO. 1
LINE RECEIVER NO. 2
-5V SOURCE
CLOCK REGENERATION
RZ+L
DM
NRZ DATA
SCHEMATIC CCR036
SIZE D
CODE IDENT NO 20747
460-0982-□
REV H
SCALE —
SHEET 3 OF 3

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-0982B		1-8-73	F. HINKLE
C	REVISED PER ECO 460-0982C PAP		3-12-73	F. HINKLE
D	REVISED PER ECO 460-0982C→D RMS		3-29-73	R. VOLZ
E	REVISED PER ECO 460-0982E TMB		1-8-74	J. KOEHLER
F	REVISED PER ECO 460-0982F TMB		2-15-74	F. HINKLE
G	REVISED PER ECO 00772 DSM		5-12-75	J. RONEY
H	REVISED PER ECO 02257 NRW		6-1-77	J. MATHERS
J	REVISED PER ECO 04220 FTB		7-2-79	F Hinkle

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	J	J	J	J																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
CODE CONVERTER
CCR036-1

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	J. DILELLO	9-8-72	ENGINEER	R. WASSERMAN	10-17-72	DWG NO. PL460-0982-501	REV J
CHECKED	WKH J.S.G	9-27-72 9-11-72	APPROVED	R. CLEGG	10-25-72		
DRAFTING	J. SAMPEDRO	10-25-72	MFG	L. MIODONSKI	11-30-72	SHEET 1 OF 4	

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			REF	1	D	460-0982-501	———	20747	CARD ASS'Y & SCHEM.	
				2						
				3						
				4						
				5						
			1	6	C	400-1173	———	20747	BOARD, PRINTED WIRING	
				7						
			1	8	A	108-203-041	7022-041-000-001	91662	CONN., FINGER BLOCK	
				9						
				10						
				11						
			1	12	A	102-305-156	150D156X0020B2	56289	CAP., 15UF, 20V, 20%	C1
			5	13	A	102-419-104	8131M100651104M	72982	CAP., .1UF, 100V, 20%	C2-6
			1	14	A	102-101-471	DM15CD470J04CR	84171	CAP., 470PF, 500V, 5%	C7
				15						
				16						
				17						
			1	18	A	103-314-004	JAN2N2907	81350	TRANSISTOR, PNP	Q1
				19						
				20						
				21						
				22						

DRAWN
DATE

CHECKED
DATE

TITLE PARTS LIST
CODE CONVERTER, CCR036-□

CODE IDENT NO. 20747

DWG NO. PL 460-0982-501

SHEET 2 OF 4

REV J

80C 3A

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			4	23	A	100-003-222	RC07GF222J	81349	RES., 2.2K, 1/4W, 5%	R1,11,17,22
			1	24	A	100-003-201	RC07GF201J	81349	RES., 200Ω, 1/4W, 5%	R2
			4	25	A	100-003-102	RC07GF102J	81349	RES., 1K, 1/4W, 5%	R3-6
			10	26	A	100-003-750	RC07GF750J	81349	RES., 75Ω, 1/4W, 5%	R7-10,15,16,
				27						R18-21
			1	28	A	100-003-101	RC07GF101J	81349	RES., 100Ω, 1/4W, 5%	R12
			1	29	A	100-215-3831	RN55D3831F	81349	RES., 3.83K, 1/10W, 1%	R13
			1	30	A	100-215-2491	RN55D2491F	81349	RES., 2.49K, 1/10W, 1%	R14
				31						
				32						
				33						
				34						
			6	35	A	139-046-400	SN7400N-10	01295	IC, TTL	U1,2,5,12,13,16
			2	36	A	139-046-490	SN7490AN-10	01295	IC, TTL	U3,4
			1	37	A	139-046-404	SN7404N-10	01295	IC, TTL	U6
			3	38	A	139-051-103	SN74H103N-10	01295	IC, TTL	U7,14,15
			4	39	A	139-051-451	SN74H51N-10	01295	IC, TTL	U8,9,23,30
			1	40	A	139-051-474	SN74H74N-10	01295	IC, TTL	U10
			3	41	A	139-051-400	SN74H00N-10	01295	IC, TTL	U11,27,29
			2	42	A	139-085-107	SN75107AN-10	01295	IC	U17,18
			1	43	A	139-046-495	SN7495AN-10	01295	IC, TTL	U19
			2	44	A	139-051-404	SN74H04N-10	01295	IC, TTL	U20,26

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST CODE CONVERTER, CCR036-□	20747	PL 460-0982-501 SHEET 3 OF 4	J

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			1	45	A	139-046-420	SN7420N-10	01295	IC, TTL	U21
			1	46	A	139-051-411	SN74H11N-10	01295	IC, TTL	U22
			1	47	A	139-046-197	SN74197N-10	01295	IC, TTL	U24
			1	48	A	139-046-157	SN74157N-10	01295	IC, TTL	U25
			2	49	A	139-046-493	SN7493AN-10	01295	IC, TTL	U28, 31
				50						
				51						
				52						
			1	53	A	131-013-001	10047	07047	PAD, TRANS., TO18	USE WITH Q1
				54						
				55						
			AR	56	C	217-0312-001	B5207-500-48T	29593	BUS BAR, MODIFICATION	
				57						
				58						
			AR	59	A	113-001-006	299/1	92194	WIRE, BUS #26AWG	
				60						
				61						
			8	62	A	121-202-005	8041-1G7	91506	JACK, TEST, GREEN	1-8
			1	63	A	121-202-010	8041-1G6	91506	JACK, TEST, BLACK	GND
				64						
				65						
			AR	66	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571

DRAWN
DATE

CHECKED
DATE

TITLE PARTS LIST
CODE CONVERTER, CCR036-☐

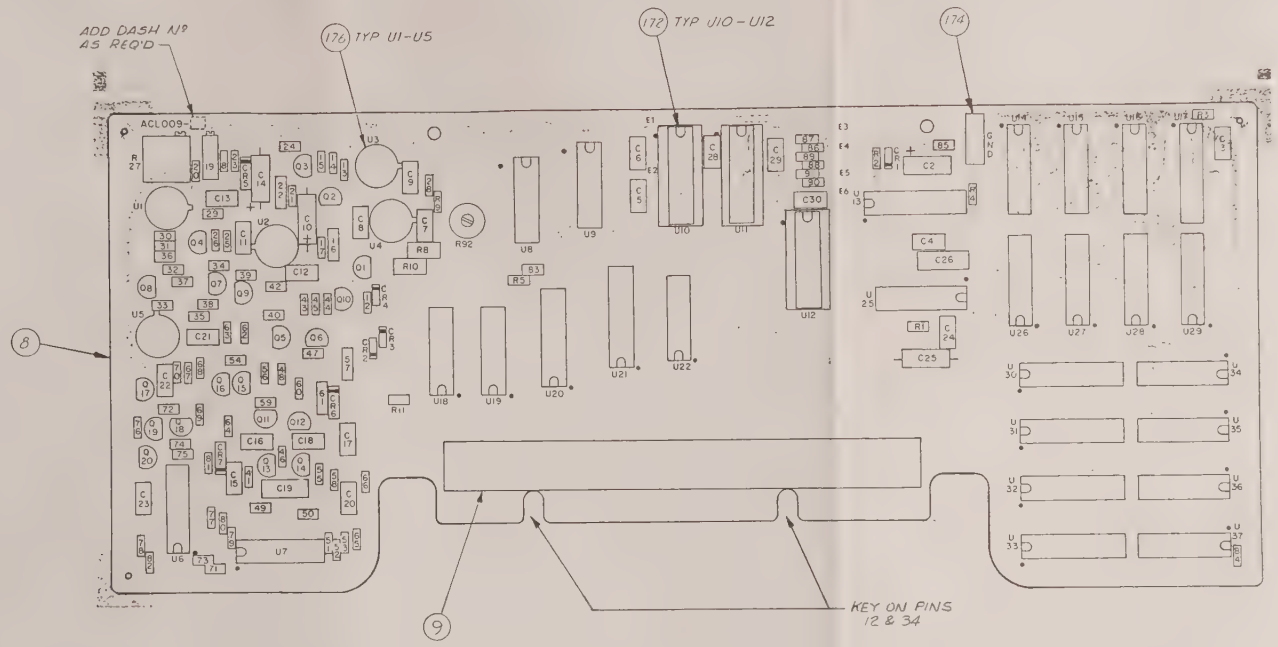
CODE IDENT NO. 20747

DWG NO. PL460-0982-501

SHEET 4 OF 4

REV J

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 08406	5-2-82	



NOTES:

1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. Nº A)401-0010.

FOR PARTS LIST SEE PL 460-1823-□

DRAWN J.S. GOODOLF DATE 4-13-82	AYDIN MONITOR SYSTEMS FORT WASHINGTON PENNA 19034
CHECKED R.K. Kotee 14 APR 82	
DRAFTING	CARD ASSEMBLY AUTO CALIBRATION LOGIC ACL009-□
ENGINEER	
MFG	
APPROVED MOISES LEVY	SIZE D · CODE IDENT NO. 20747 · 460-1823-□ · REV B
APPROVED	SCALE 2:1 · SHEET 1 OF 1

NEXT ASSY	USED ON
	4972-20
APPLICATION	

800-0684-1A

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISE PER ECO 08406 WKH 5-2-83		10MAY83	RSVol2
C	REVISED PER ECO #08565 JSG		19AUG83	RS Vol2

NOTES: 1. MAKE LEAD SPACING OF ITEM 14 .20
2. MAKE LEAD SPACING OF ITEM 16 .25
3. FOR SCHEMATIC SEE D) 600-0311

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION																							

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
AUTO CALIBRATION LOGIC
TYPE ACL009-1

CODE IDENT 20747
CONTRACT NO. 4972-20

DRAWN	J.S. GOODOLF	3-26-82	ENGINEER	M. LEVY	2AUG83	DWG NO.	REV
CHECKED	R.E. Krotee	5 APR 82	APPROVED		2AUG83	PL460-1823-501	C
DRAFTING	E Stricker	3-2-82	MFG		3/31/82	SHEET 1 OF 5	

800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
		460-1823-501		C	PARENT ACL009-1	
1	008	400-1776	400-1776		P.W.BOARD DUMBO	
1	009	108-203-041	7022-041-000001	C	CONN FING BLOC 41 POS	
1	012	102-366-003	T330D227M006AS	E	CAP 220UF 6V 20%	C2
2	014	102-109-200	DM10/D10	B	CAP 20PF 500V 5% (NOTE 1)	C3
						C4
16	016	102-419-104	CK06BX104M	P	CAP .1UF 100V 20% (NOTE 2)	C5
						C6
						C7
						C8
						C9
						C11
						C12
						C13
						C15
						C16
						C17
						C18
						C20
						C21
						C22
						C23
2	019	102-305-225	150D225X0020A2	D	CAP 2.2UF 20V 20%	C1
						C
1	021	102-116-470	DM15CA470G04CR	B	CAP 47PF 100V 2%	C
1	024	100-017-391	RC05GF391J	C	RES 390 OHMS 1/8W 5%	C24
2	026	102-001-473	230B1B473	J	CAP .047UF 100V 20%	C25
						C26
3	028	102-419-103	CY20A103M	P	CAP .01UF 100V 20%	C28
						C29
						C30
4	033	104-503-014	1N4531	G	DIODE SIG MINIATURE	CR1
						CR2
						CR3
						CR4
1	035	104-308-006	IN821A	D	DILDE ZENER SILICON	CR5
1	037	104-056-106	1N751A	P	DIODE ZENER CASE 51	CR6
1	039	104-056-105	1N753A	P	DIODE ZENER CASE 51	CR7
6	043	103-408-001	2N4124	C	TRANS SIL NPN TO-92	Q1
						Q2
						Q5
						Q6
						Q10
						Q19
8	045	103-304-001	2N4126	D	TRANS SIL PNP TO-92	Q3
						Q4
						Q7
						Q8
						Q9
						Q1
						Q.
						Q20
6	048	103-437-001	2N5770	B	TRANS SIL NPN TO-92	Q11
						Q12
						Q13

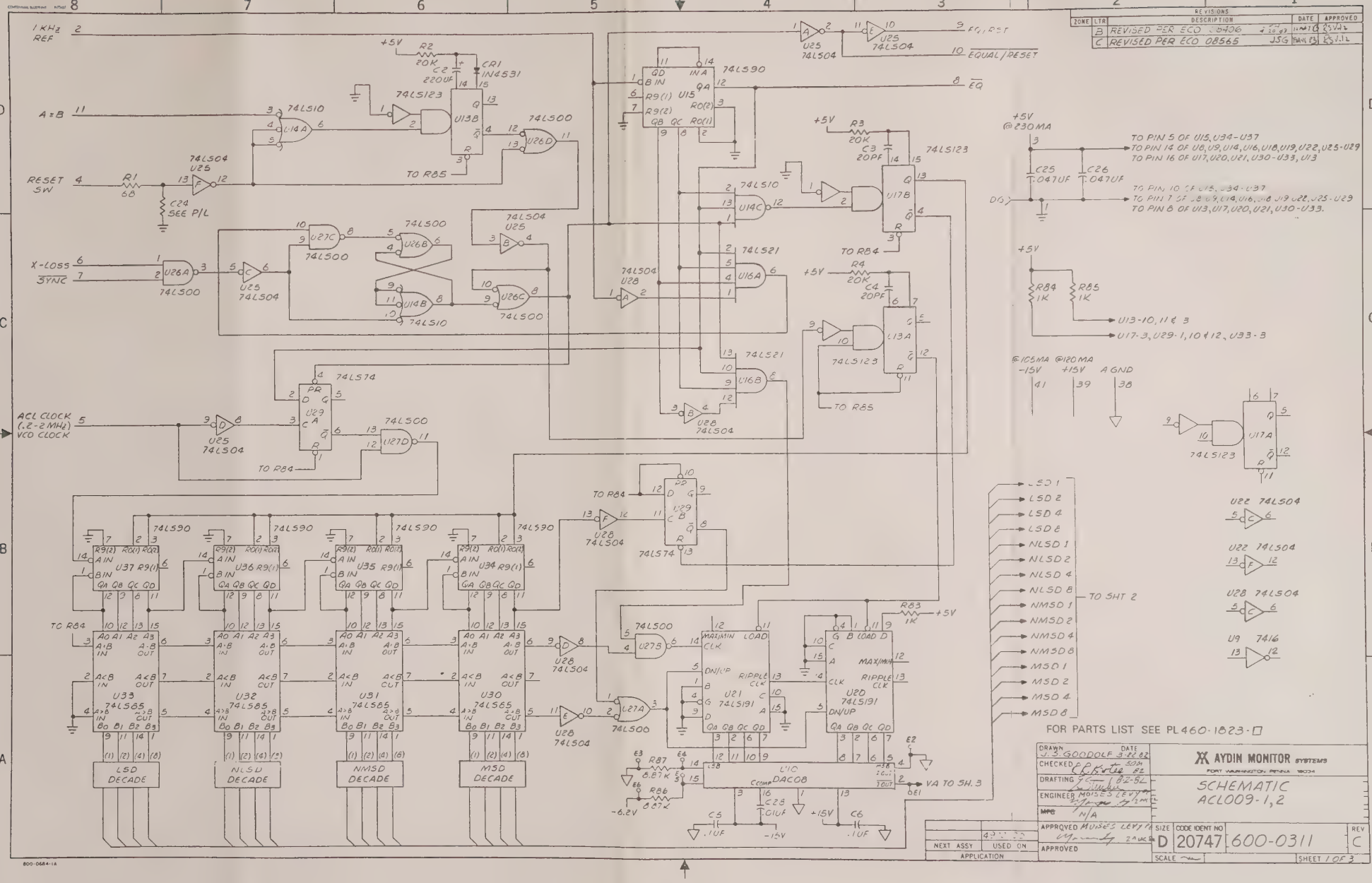
QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						Q14
						Q15
						Q16
1	052	100-017-680	RC05GF680J	C	RES 68 OHMS 1/8W 5%	R1
3	054	100-017-203	RC05GF203J	C	RES 20K 1/8W 5%	R2
						R3
						R4
11	056	100-017-152	RC05GF152J	C	RES 1.5K 1/8W 5%	R5
						R11
						R12
						R24
						R30
						R31
						R32
						R33
						R34
						R35
						R68
1	059	100-017-104	RC05GF104J	C	RES 100K 1/8W 5%	R13
1	061	100-215-1273	RN55D1273F	G	RES 127K 1/8W 1%	R8
1	063	100-222-2371	RN50C2371F		RES 2.37K 1/20W 1%	R9
1	065	100-215-1301	RN55D1301F	G	RES 1.3K 1/8W 1%	R10
3	067	100-017-331	RC05GF331J	C	RES 330 OHMS 1/8W 5%	R14
						R21
						R70
2	069	100-017-512	RC05GF512J	C	RES 5.1K 1/8W 5%	R15
						R17
2	071	100-003-471	RC07	D	RES 470 OHMS 1/4W 5%	R16
						R22
5	073	100-017-102	RC05GF102J	C	RES 1K 1/8W 5%	R18
						R75
						R83
						R84
						R85
1	075	101-130-025	548-72HS-1K	C	POT 1K 1/2W 10%	R19
1	077	100-222-4531	RN50C4531F	F	RES 4.53K 1/20W 1%	R20
1	079	100-222-4991	RN50C4991F	F	RES 4.99K 1/20W 1%	R23
1	081	100-222-1432	RN50C1432F	F	RES 14.3K 1/20W 1%	R25
1	083	100-222-6650	RN50C6650F	F	RES 665 OHMS 1/20W 1%	R26
1	085	101-101-001	3290P-1-101	H	POT 100 1W 5%	R27
2	087	100-017-912	RC05GF912J	C	RES 9.1K 1/8W 5%	R28
						R66
2	089	100-222-1002	RN50C1002F	F	RES 10K 1/20W 1%	R29
						R36
1	091	100-222-2002	RN50C2002F	F	RES 20K 1/20W 1%	R37
1	093	100-222-4022	RN50C4022F	F	RES 40.2K 1/20W 1%	R38
1	095	100-017-SBT	RC05	C	RES SBT 1/8W 5%	R39
13	097	100-017-101	RC05GF101J	C	RES 100 OHMS 1/8W 5%	R40
						R42
						R47
						R48
						R49
						R50
						R53
						R54

PL460-1823-501 C
SHEET 3

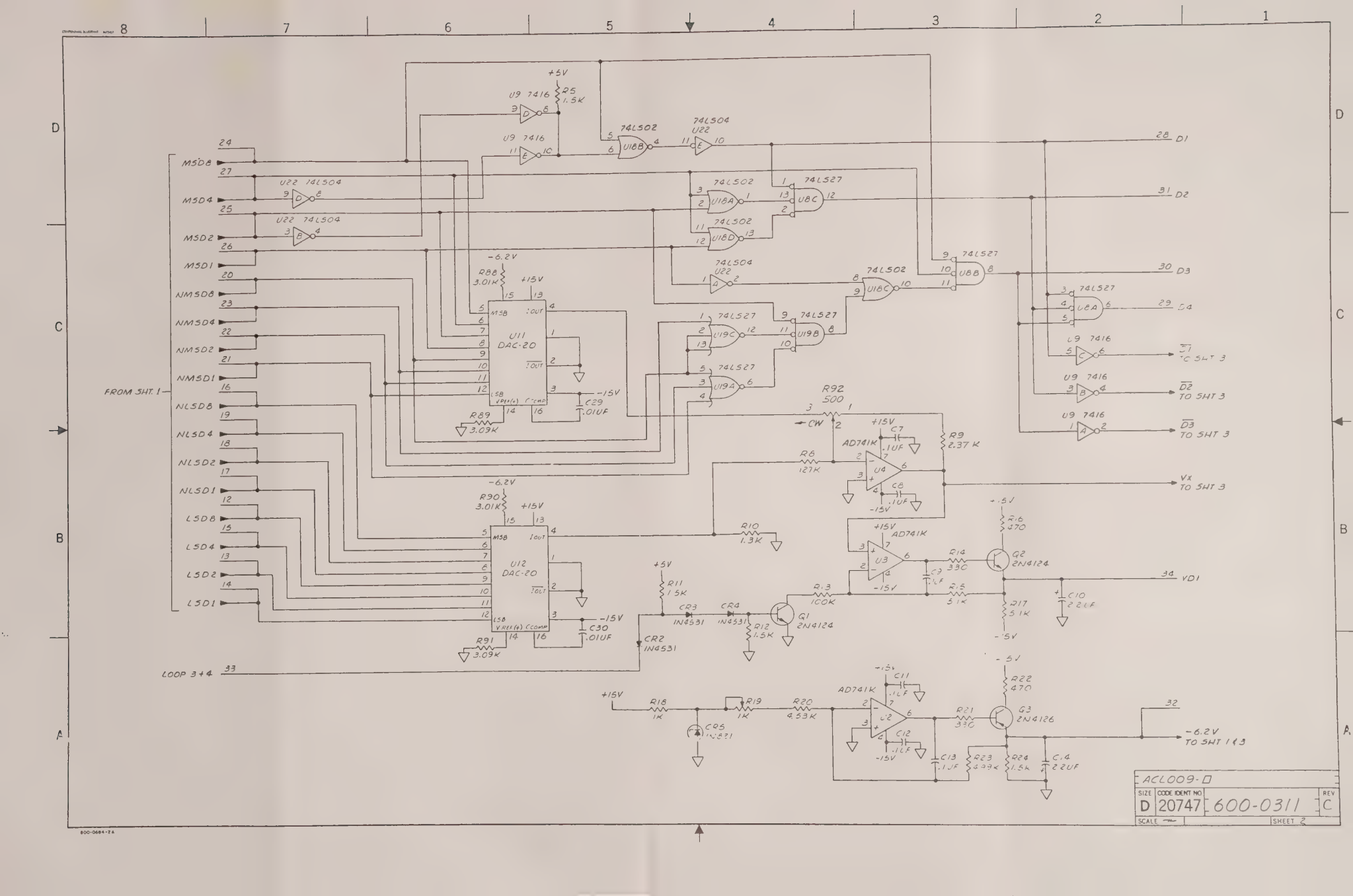
QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						R59
						R72
						R76
						R79
						R80
2	101	100-017-681	RC05GF681J	C	RES 680 OHMS 1/8W 5%	R41
						R58
2	103	100-017-272	RC05GF272J	C	RES 2.7K 1/8W 5%	R43
						R45
1	105	100-017-103	RC05GF103J	C	RES 10K 1/8W 5%	R44
2	107	100-222-1210	RN50C1210F	F	RES 121 OHMS 1/20W 1%	R46
						R55
7	109	100-222-1000	RN50C1000F	F	RES 100 OHMS 1/202 1%	R51
						R52
						R56
						R60
						R71
						R73
						R77
1	112	100-003-182	RC07	D	RES 1.8K 1/4W 5%	R57
1	114	100-003-561	RC07	D	RES 560 OHMS 1/4W 5%	R61
2	116	100-017-470	RC05GF470J	C	RES 47 OHMS 1/8W 5%	R62
						R6
1	118	100-017-471	RC05GF471J	C	RES 470 OHMS 1/8W 5%	R
1	120	100-017-222	RC05GF222J	C	RES 2.2K 1/8W 5%	R65
1	122	100-222-1211	RN50C1211F	F	RES 1.21K 1/20W 1%	R67
3	124	100-222-3011	RN50C3011F	F	RES 3.01K 1/20W 1%	R69
						R88
						R90
2	126	100-017-750	RC05GF750J	C	RES 75 OHMS 1/8W 5%	R78
						R82
2	128	100-222-2001	RN50C2001F	F	RES 2K 1/20W 1%	R74
						R81
2	130	100-222-8871	MF3C		RES 8.87K 1/20W 1%	R86
						R87
2	133	100-222-3091	RN50C3091F	F	RES 3.09K 1/20W 1%	R89
						R91
1	134	101-156-501	3339P-1-501	F	POT 500 .5W 10%	R92
5	139	139-141-001	AD741KH	E	IC OP AMP 8 PIN TO-99	U1
						U2
						U3
						U4
						U5
2	141	139-209-002	CA3046	D	IC	U6
						U7
2	143	139-198-427	SN74LS27	A/B	IC TTL 14 PIN	U8
						U19
1	145	139-046-416	SN7416N-10	A/P	IC TTL 14 PIN	U9
1	147	139-593-002	DAC-08EP		8 BIT D/A CONV	U1
2	149	139-594-002	DAC-20CP		2 DIG BCD D/A CONV	U1
						U12
2	151	139-198-123	74LS123	A/B	IC TTL 16 PIN	U13
						U17
1	153	139-198-410	74LS10N	A/B	IC TTL 14 PIN	U14
5	155	139-198-490	74LS90	A/B	IC TTL 14 PIN	U15
						U34

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						U35
						U36
						U37
1	157	139-198-421	SN74LS21	A/B	IC TTL 14 PIN	U16
1	159	139-198-402	74LS02N	A/B	IC TTL 14 PIN	U18
2	161	139-198-191	SN74LS191	A/B	IC TTL 16 PIN	U20
						U21
3	163	139-198-404	74LS04N	A/B	IC TTL 14 PIN	U22
						U25
						U28
2	165	139-198-400	SN74LS00N	A/B	IC TTL 14 PIN	U26
						U27
1	167	139-198-474	74LS74N	A/B	IC TTL 14 PIN	U29
4	169	139-198-485	74LS85	A/B	IC TTL 16 PIN	U30
						U31
						U32
						U33
3	172	108-935-003	ICO-316-SGT	A	SOCK DIP 16 PIN	
1	174	121-202-010	SPCJ-200-03	K	TEST POINT PC BLK	D. GND
5	176	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	

PL460-1823-501 C
SHEET 5



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B REVISED PER ECO 08406
C REVISED PER ECO 08565 JSG
1 KHz REF
A=B
RESET SW
X-LOSS
SYNC
ACL CLOCK (.2-2 MHz) VCO CLOCK
EQ/RST
EQUAL/RESET
EQ
TO R85
TO R84
TO PIN 5 OF U15, U34-U37
TO PIN 14 OF U8, U9, U14, U16, U18, U19, U22, U25-U29
TO PIN 16 OF U17, U20, U21, U30-U33, U13
TO PIN 10 OF U15, U34-U37
TO PIN 7 OF U8, U9, U14, U16, U18, U19, U22, U25-U29
TO PIN 8 OF U13, U17, U20, U21, U30-U33.
U13-10, 11 & 3
U17-3, U29-1, 10 & 12, U33-3
@105MA -15V
@120MA +15V
A GND
TO SHT 2
VA TO SH. 3
LSD DECADE
NLSD DECADE
NMSD DECADE
MSD DECADE
FOR PARTS LIST SEE PL460-1823-□
DRAWN J.S. GOODOLF
CHECKED
DRAFTING
ENGINEER MOISES LEVY
MFG N/A
APPROVED MOISES LEVY
APPROVED
NEXT ASSY
USED ON
APPLICATION
AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 18034
SCHEMATIC ACL009-1,2
SIZE D
CODE IDENT NO 20747
600-0311
REV C
SCALE
SHEET 1 OF 3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MSD8
MSD4
MSD2
MSD1
NMSD8
NMSD4
NMSD2
NMSD1
NLSD8
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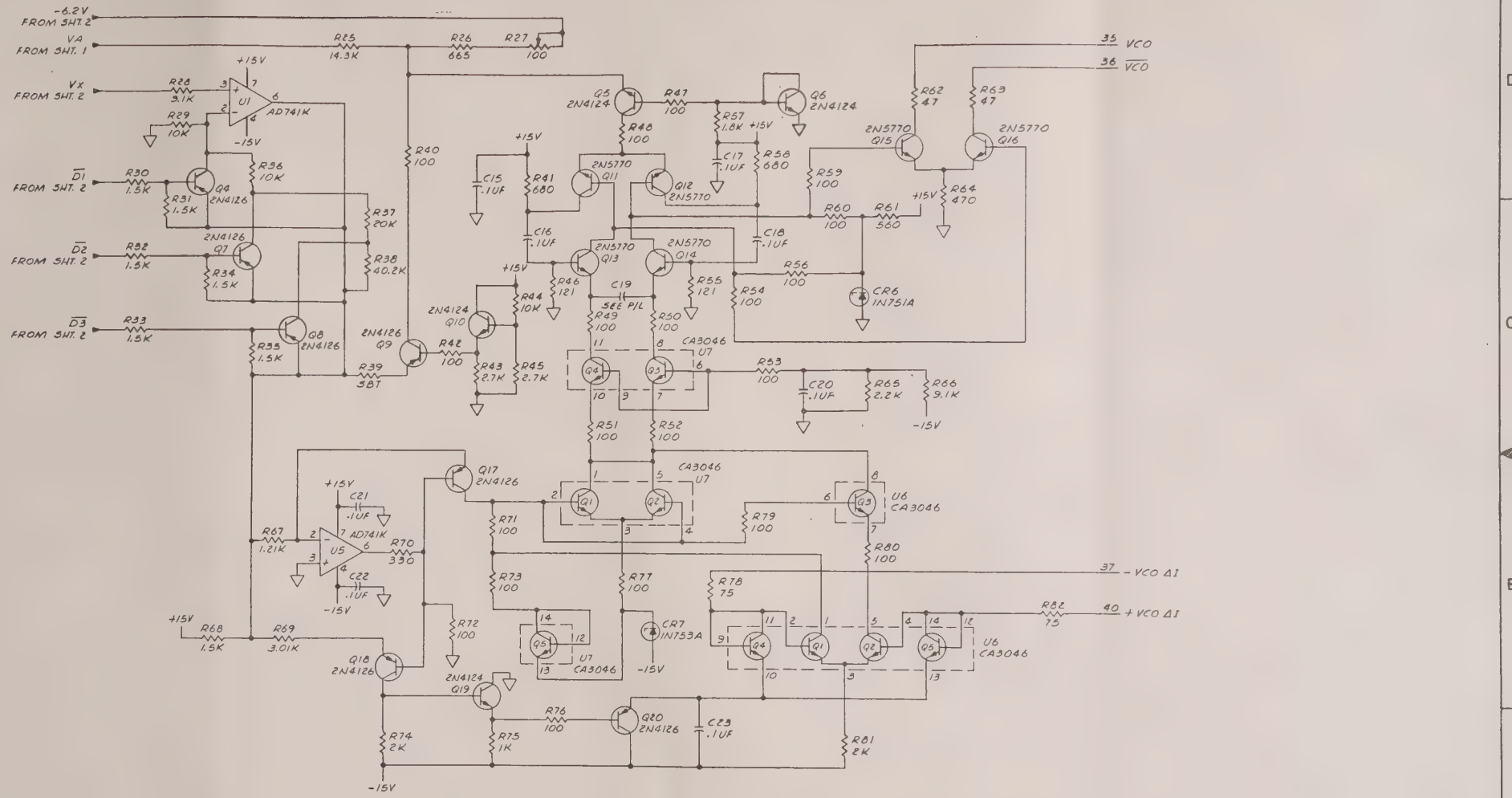
NLSD2
NLSD1
LSD8
LSD4
LSD2
LSD1
LOOP 3+4
+5V
-6.2V
+15V
-15V
U9 7416
U22 74LS04
74LS02
74LS27
U11 DAC-20
U12 DAC-20
AD741K
R88 3.01K
R89 3.09K
R90 3.01K
R91 3.09K
R92 500
R9 2.37 K
R8 127K
R10 1.3K
R11 1.5K
R12 1.5K
R13 100K
R14 330
R15 5.1K
R16 470
R17 5.1K
R18 1K
R19 1K
R20 4.53K
R21 330
R22 470
R23 4.99K
R24 1.5K
C7 .1UF
C8 .1UF
C29 .01UF
C30 .01UF
C1 .1UF
C2 .1UF
C10 2.2UF
C11 .1UF
C12 .1UF
C13 .1UF
C14 2.2UF
CR2 IN4531
CR3 IN4531
CR4 IN4531
CR5 IN821
Q1 2N4124
Q2 2N4124
Q3 2N4126
D1
D2
D3
D4
VD1
Vx
TO SHT 3
-6.2V TO SHT 1 & 3
ACL009-□
SIZE D
CODE IDENT NO 20747
600-0311
REV C
SCALE
SHEET 2

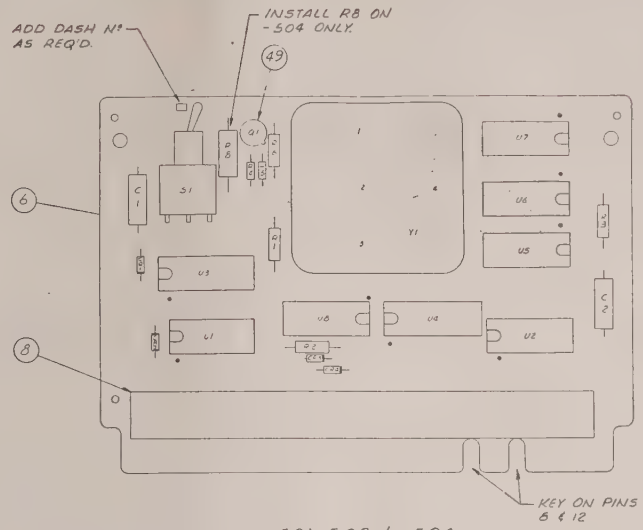


ACL009-D

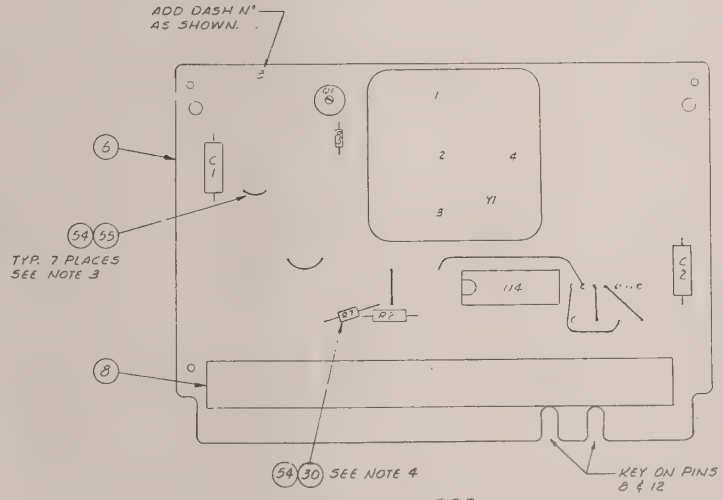
SIZE	CODE IDENT NO.		REV
D	20747	600-0311	C

SCALE — SHEET 3

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
		SEE P/L FOR REV'S B THRU G		
	H	REVISED PER ECO # 07280 JSG	12-5-72	RSV



-501, -502 & -504



-503

NOTES:

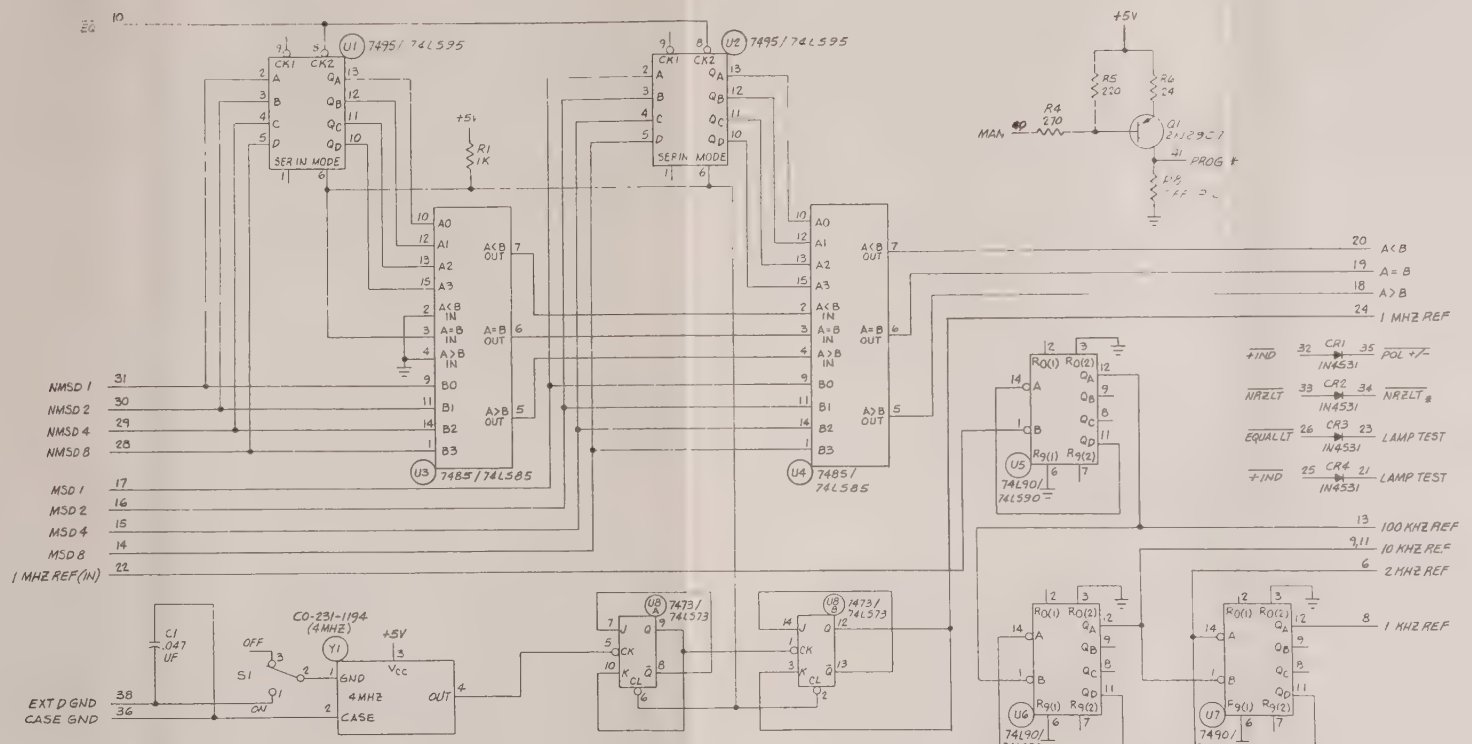
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. Nº A) 401-0010.
2. THIS CARD IS DESIGNED TO FIT INTO TWO .500 OR .600 CARD SLOTS.
3. JUMPER LIST (-503 ONLY)
   1. U2-7 TO U2-11
   2. U2-3 TO U2-12
   3. U2-5 TO U2-14
   4. U2-13 TO U8-1
   5. U8-5 TO U8-10
   6. U3-5 TO U3-8
   7. S1-1 TO S1-2
4. INSTALL R7 BETWEEN U1-7 & U8-9

FOR PARTS LIST SEE PL 460-1105-□

DRAWN N DAVIS DATE	AYDIN MONITOR SYSTEMS FORT WASHINGTON, PENNA.
CHECKED G LEONARD	
DRAFTING E. STUCKER	CARD ASSEMBLY TYPE XTL028 (CRYSTAL OSCILLATOR)
ENGINEER R CLEGG	
MFG G. BROWN	
APPROVED R CLEGG 12-31-73	SIZE D · CODE IDENT NO 20747 · 460-1105-501 THRU 504 · REV H
APPROVED	SCALE 2:1 · SHEET 1 OF 3

NEXT ASSY	USED ON
	2509
APPLICATION	

800-0684-1A



SIZE	CODE IDENT NO		REV
D	20747	XTL028-1,-2,-4 460-1105-501 -502	H
SCALE		SHEET 2 OF 3	

800 0684 2

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-1105		8-10-74	P. TYLER
C	REVISED PER ECO 03043		4-24-76	F. HINKLE
D	REVISED PER ECO 03242		5-28-78	D. MOUAT
E	REVISED PER ECO 03308 R.R.K		7-18-78	WASSERMAN
F	REVISED PER ECO 04220 J.S.G.		7-2-79	F. Hinkle
G	REVISED PER ECO 06248 Gur		4/30/81	R Malcolmson
H	REVISED PER ECO 07280 JSG		18Feb82	R.S. Volz

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	H	H																					

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

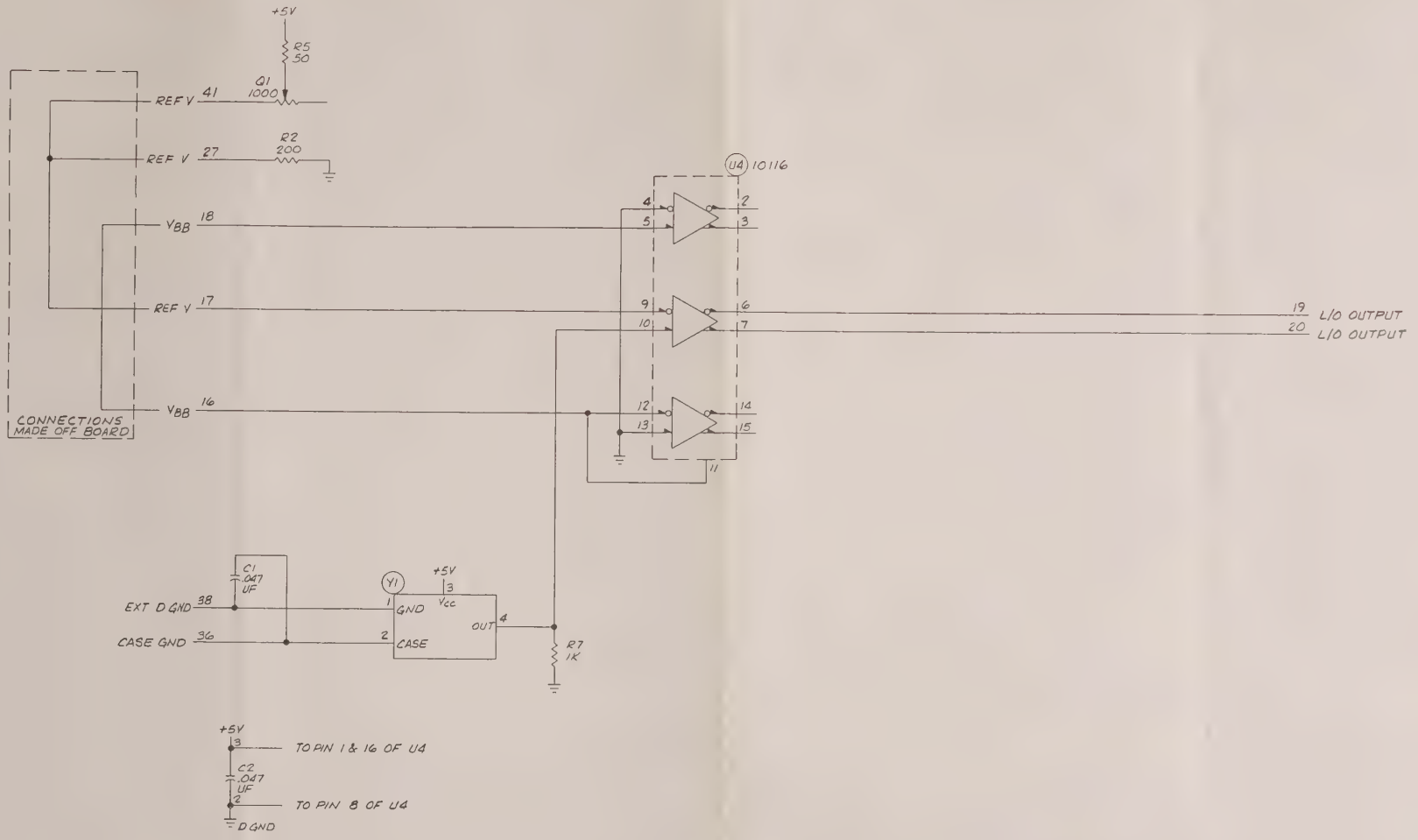
TITLE PARTS LIST
CRYSTAL OSCILLATOR
XTL028-1

CODE IDENT 20747
CONTRACT NO. 2509

DRAWN	N. DAVIS		ENGINEER	R. CLEGG		DWG NO. PL460-1105-501	REV H
CHECKED	G. LEONARD		APPROVED	R. CLEGG	12-31-73		
DRAFTING	E. STUCKER		MFG	G. BROWN		SHEET 1 OF 2	

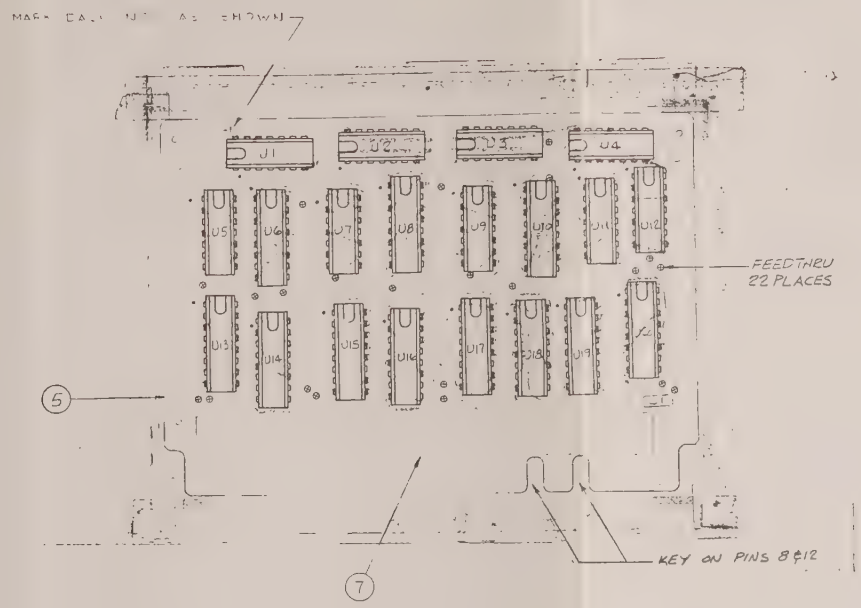
800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		460-1105-501		H	PARENT XTL028-1	
1	006	400-1534			BOARD P.W. MONI 1	
1	008	108-203-040	7022-040-000001	C	CONN FING BLOC 40 POS	
2	012	102-001-473	230B1B473	H	CAP .047UF 100V 20%	C1
						C2
4	015	104-503-014	1N4531	F	DIODE SIG MINIATURE	CR1
						CR2
						CR3
						CR4
1	018	103-314-004	JAN2N2907	E	TRANS SIL PNP TO-18	Q1
1	023	100-003-102	RC07	D	RES 1K 1/4W 5%	R1
2	024	100-003-390	RC07	D	RES 39 OHMS 1/4W 5%	R2
						R3
1	025	100-017-271	RC05GF271J		RES 270 1/8W 5%	R4
1	026	100-017-221	RC05GF221J		RES 220 1/8W 5%	R5
1	027	100-003-240	RC07	D	RES 24 OHMS 1/4 W 5%	R6
1	031	107-205-001	7101AB	G	SW TGL SPDT	S1
2	034	139-046-495	139-217-495	A/P	IC TTL 14 PIN	U1
						U2
2	036	139-046-485	SN7485N-10	A/P	IC TTL 16 PIN	U3
						U4
2	038	139-198-490	74LS90	A/B	IC TTL 14 PIN	U5
						U6
1	040	139-046-490	139-217-490	A/P	IC TTL 14 PIN	U7
1	041	139-046-473	SN7473N-10	A/P	IC TTL 14 PIN	U8
1	046	133-019-001	NO.231-49-006	B	CRYSTAL OSC 4 MHZ	Y1
1	049	131-013-001	10047	B	PAD TRANS TO 18 4 PIN	



XTL028-3			
SIZE D	CODE IDENT NO. 20747	460-1105-503	REV H
SCALE		SHEET 3 of 3	

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 460-0981B	[illegible]	[illegible]
	C	REVISED PER ECO 460-0981C	[illegible]	[illegible]
	D	REVISED PER ECO 03472	[illegible]	[illegible]
	E	REVISED PER ECO 04220	[illegible]	[illegible]



NOTES:
FOR GENERAL MANUFACTURING
& ENGINEERING NOTES SEE DWG
NO. 401-0010

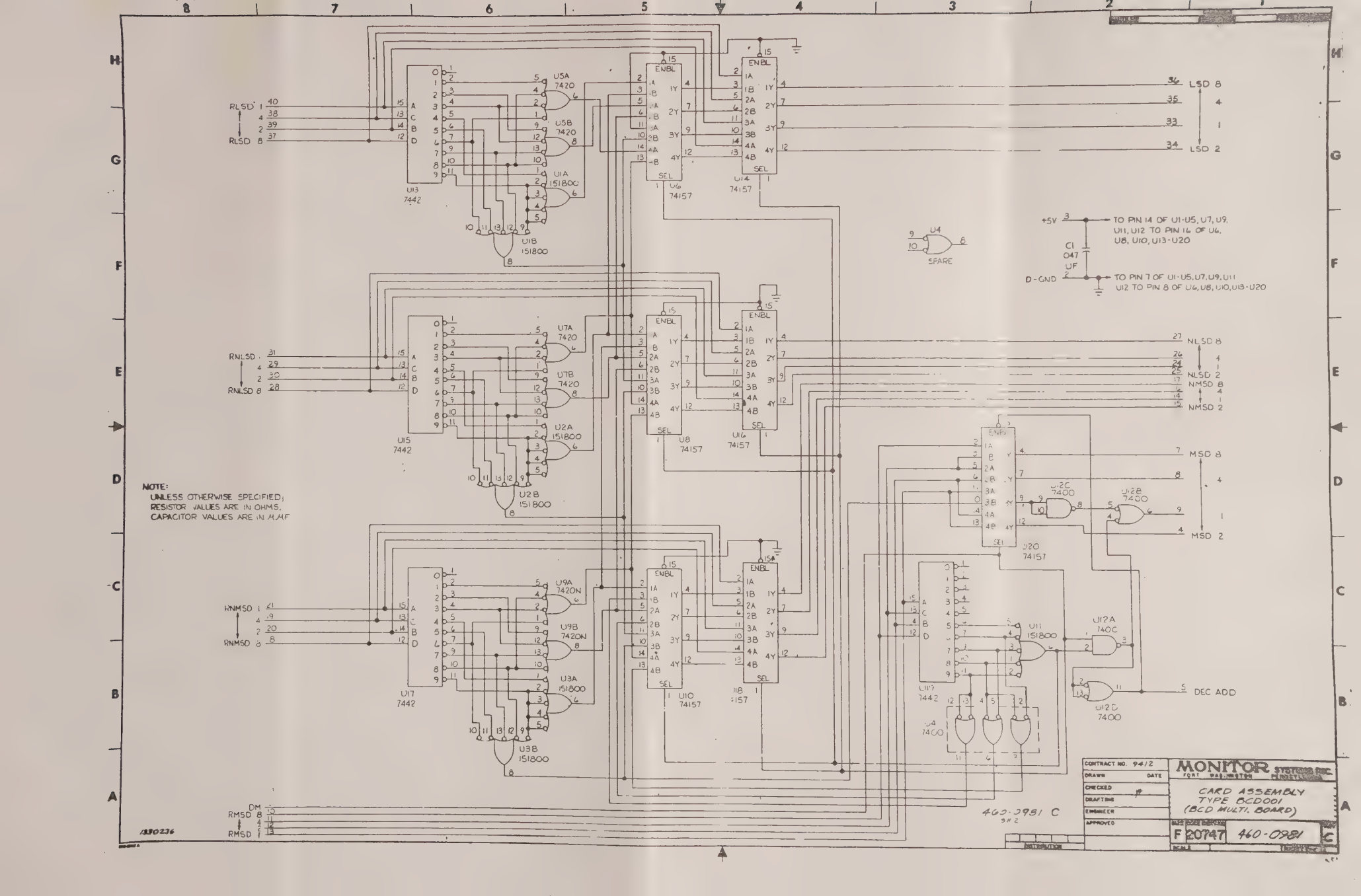
FOR SCHEMATIC SEE MICROFILM.
FOR PARTS LIST SEE PL460-0981-501

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501	LIST OF MATERIALS					

DRAWN J WALLACE	DATE 8-8-72	AYDIN MONITOR SYSTEMS, FORT WASHINGTON PENNA 19034
CHECKED K HOUSEAL	10-2-72	
DRAFTING SAMPEDRO	10-2-72	CARD ASSEMBLY BCD MULTI. BD BCD001-1
ENGINEER R WASSERMAN	10-9-72	
MFG P.R HELLER	10/10/72	
APPROVED R CLEGG	10/25/72	SIZE D · CODE IDENT NO 20747 · 460-0981-501 · REV E
APPROVED		SCALE 2:1 · SHEET 1 OF 2

NEXT ASSY	USED ON
	9412
APPLICATION	

600-0684-1


RLSD 1
RLSD 8
U13
7442
U5A
7420
U5B
7420
U1A
151800
U1B
151800
U6
74157
U14
74157
LSD 8
LSD 4
LSD 2
RNLSD 1
RNLSD 8
U15
7442
U7A
7420
U7B
7420
U2A
151800
U2B
151800
U8
74157
U16
74157
NLSD 8
NLSD 4
NLSD 2
NMSD 8
NMSD 4
NMSD 2
RNMSD 1
RNMSD 8
U17
7442
U9A
7420N
U9B
7420N
U3A
151800
U3B
151800
U10
74157
U18
74157
U20
74157
U2C
7400
U2B
7400
MSD 8
MSD 4
MSD 2
U11
151800
U12A
7400
U12D
7400
U4
7400
U19
7442
DEC ADD
U4
SPARE
+5V
C1
047
UF
D-GND
TO PIN 14 OF U1-U5, U7, U9, U11, U12 TO PIN 14 OF U6, U8, U10, U13-U20
TO PIN 7 OF U1-U5, U7, U9, U11 U12 TO PIN 8 OF U6, U8, U10, U13-U20
DM
RMSD 8
RMSD 1
NOTE:
UNLESS OTHERWISE SPECIFIED;
RESISTOR VALUES ARE IN OHMS,
CAPACITOR VALUES ARE IN MMF
460-0981 C
CONTRACT NO. 9412
DRAWN
DATE
CHECKED
DRAFTING
ENGINEER
APPROVED
MONITOR SYSTEMS INC.
CARD ASSEMBLY
TYPE BCD001
(BCD MULTI. BOARD)
F 20747
460-0981
C

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	SEE ECO 460-0981B		3/29/73	R. VOLZ
C	SEE ECO 460-0981C		10/15/73	J. G.
D	REVISED PER ECO 03472		9/18/78	D. MOUAT
E	REVISED PER ECO 04220 AP		7-2-79	J Hinkle

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	E	E																					

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
BCD MULTI BD.
BCD 001-1

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	J. WALLACE	8-8-72	ENGINEER	R. WASSERMAN	10-9-72	DWG NO. PL 460-0981-501	REV E
CHECKED	K. HOUSEAL	10-2-72	APPROVED	R. CLEGG	10-25-72		
DRAFTING	J. SAMPEDRO	10-27				SHEET 1 OF 2	

800-0066

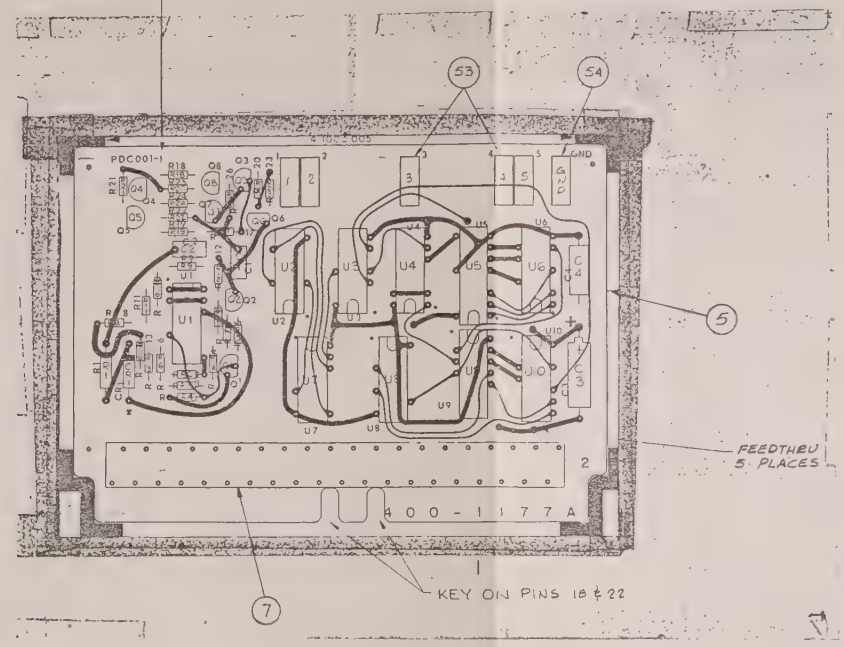
AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			REF	1	D	460-0981-501	———	20747	CARD ASSY & SCHEMATIC	
				2						
				3						
				4						
			1	5	C	400-1172	———	20747	BD. PRINTED WIRING	
				6						
			1	7	A	108-203-040	7022-040-000-001	91662	CONNECTOR, FINGER BLOCK	
				8						
				9						
			1	10	A	102-419-104	8131M10065 1104M	72982	CAP, .1UF, 100V ± 20%	C1
				11						
				12						
				13						
			3	14	A	139-046-420	SN7420N-10	01295	I.C. TTL	U5, U7, U9
			2	15	A	139-046-400	SN7400N-10	01295	I.C. TTL	U4, U12
			4	16	A	139-045-800	SN151800N-10	01295	I.C. DTL	U1-U3, U11
			7	17	A	139-046-157	SN74157N-10	01295	I.C. TTL	U6, U8, U10, U14, U16, U18, U20
				18						
			4	19	A	139-046-442	SN7442N	01295	I.C. TTL	U13, U15, U17, U19
				20						
				21						
			AR	22	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571

DRAWN J. WALLACE DATE 8·8·72	CHECKED K. HOUSEAL DATE 10·2·72	TITLE PARTS LIST BCD001-1	CODE IDENT NO. 20747	DWG NO. PL 460-0981-501 SHEET 2 OF 2	REV E

800[illegible]438A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 460-0985B	12-4-72	F. HELLER
	C	REVISED PER ECO 460-0985C	2/1/73	R.S. VOLZ
	D	REVISED PER ECO 460-0985D	5/3/73	F. HELLER
	E	REVISED PER ECO 460-0985E	7-20-73	F. HELLER
	F	REVISED PER ECO 04220	2-2-79	J. Hunter



NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO. 401-0010

FOR SCHEMATIC SEE MICROFILM
FOR PARTS LIST SEE PL460-0985-501

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501					LIST OF MATERIALS	

	DRAWN	DATE
	M. GRIES	AUG 17, 1972
	CHECKED K. HOUSEAL	9-10-72
	DRAFTING J. SAMPEDRO	10-12-72
	ENGINEER R. WASSERMAN	10-9-72
	MFG R. HELLER	10-16-72
	APPROVED R. CLEGG	10/25/72
	APPROVED	

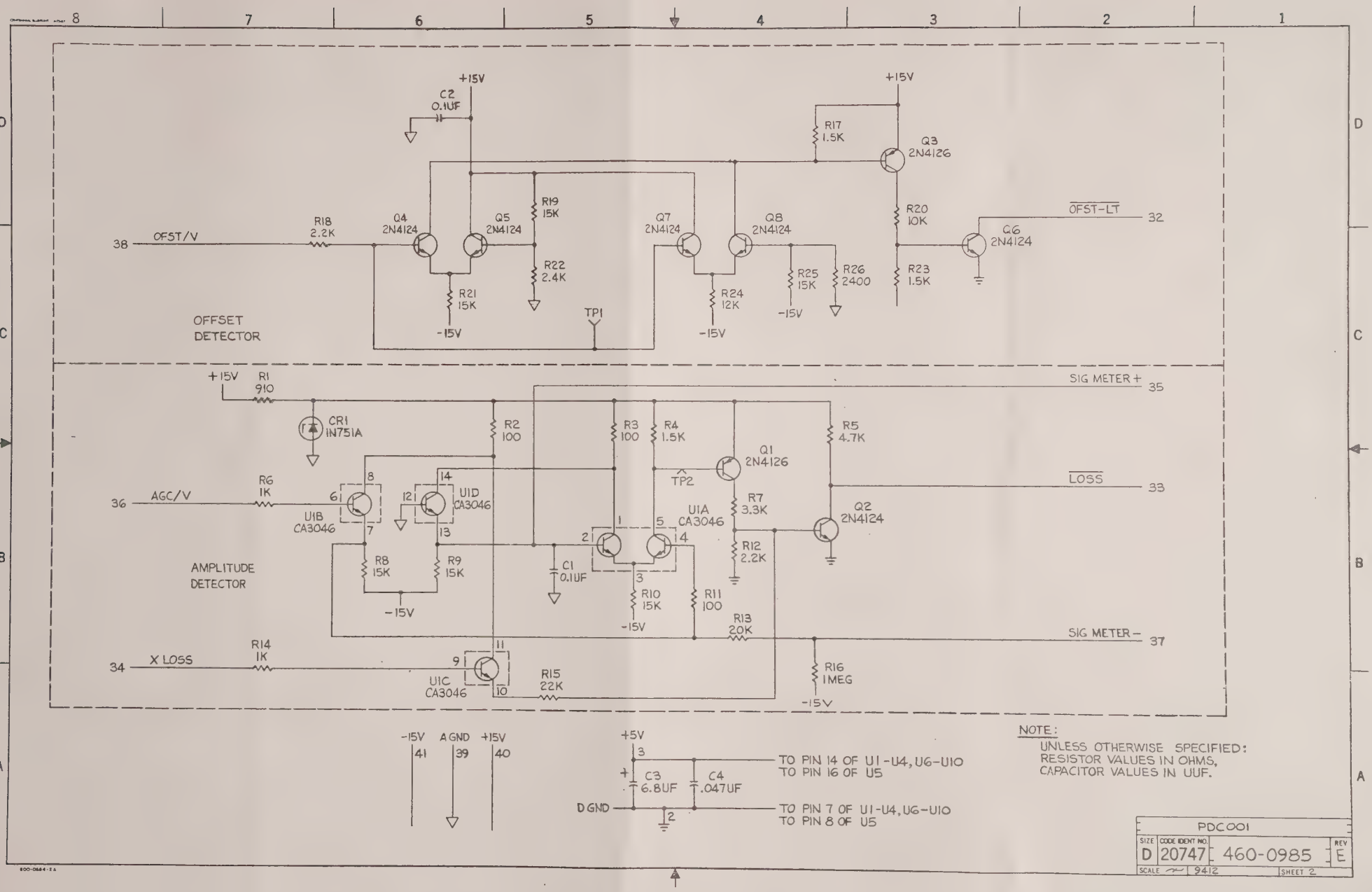
AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

CARD ASSEMBLY
PROGRAM DECODING
PDC001-1

NEXT ASSY	USED ON
	9412
APPLICATION	

SIZE	CODE IDENT NO.		REV
D	20747	460-0985-501	F
SCALE 2:1		SHEET 1 OF 3	

800-0684-1

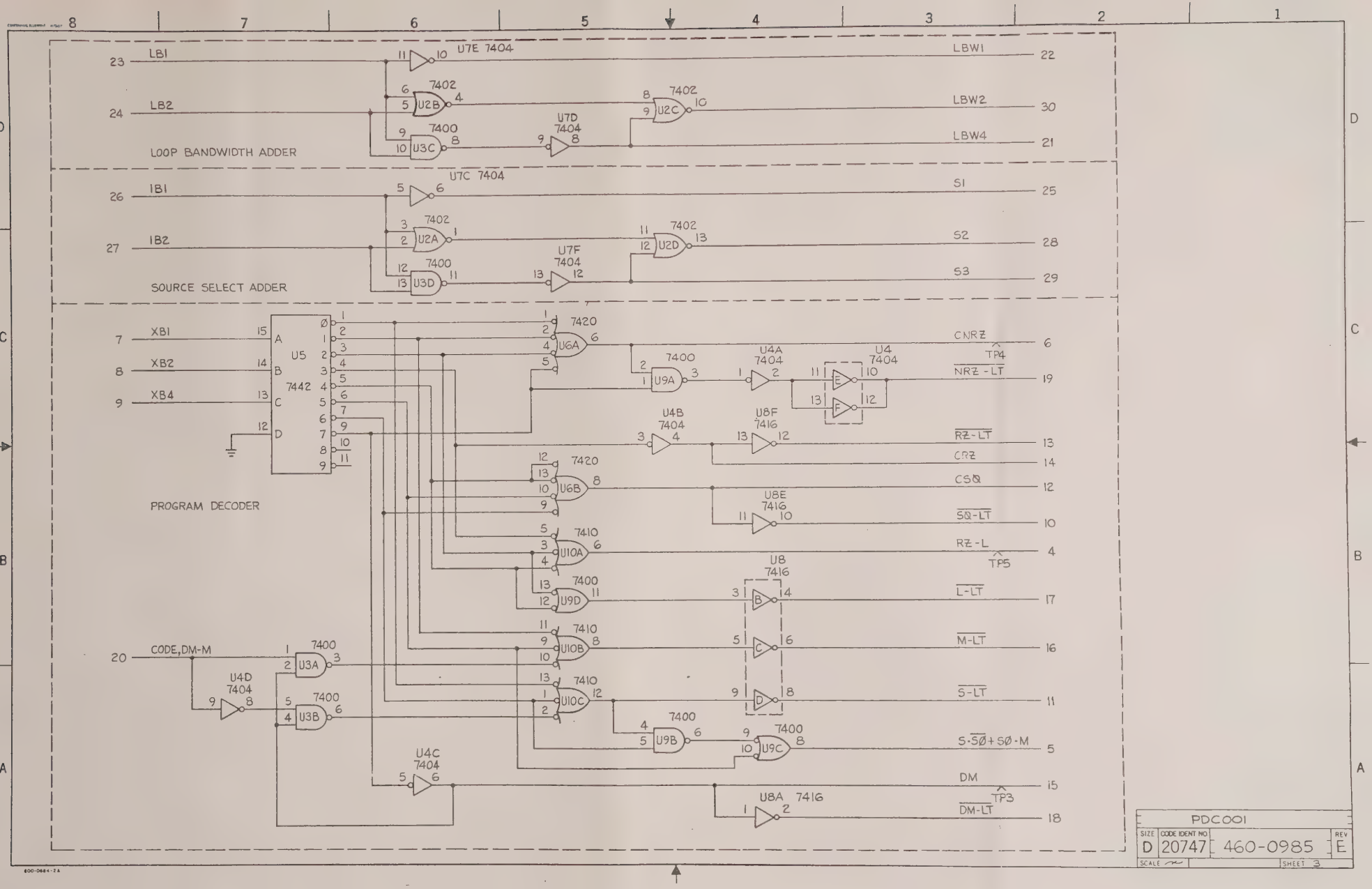


NOTE:
UNLESS OTHERWISE SPECIFIED:
RESISTOR VALUES IN OHMS,
CAPACITOR VALUES IN UUF.

PDC001

SIZE	CODE IDENT NO.		REV
D	20747	460-0985	E

SCALE ~ | 9412 | SHEET 2



PDC001

SIZE	CODE IDENT NO		REV
D	20747	460-0985	E

SCALE ~ SHEET 3

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-0985B		12·4·72	F. HINKLE
C	REVISED PER ECO 460-0985C		3·21·73	R. VOLZ
D	REVISED PER ECO 460-0985D		5·25·73	F. HINKLE
E	REVISED PER ECO 460-0985E		7·20·73	F. HINKLE
F	REVISED PER ECO 04220 O.P.		2-2-79	F Heibel

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	F	F	F	F																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
PROGRAM DECODING
PDC001-1

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	M. GRIES	8-17-72	ENGINEER	R. WASSERMAN	10-9-72	DWG NO.	REV
CHECKED	K. HOUSEAL	9-10-72	APPROVED	R. CLEGG	10-25-72	PL460-0985-501	F
DRAFTING	J. SAMPEDRO	10-12-72				SHEET 1 OF 4	

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			REF	1	D	460-0985-501	———	20747	CARD ASSY & SCHEM	
				2						
				3						
				4						
			1	5	C	400-1177	———	20747	BD. PRINTED WIRING	
				6						
			1	7	A	108-203-040	7022-040-000-001	91662	CONNECTOR, FINGER BLOCK	
				8						
				9						
			2	10	A	102-419-104	CS30A104M	71590	CAP., 0.1UF, 100V, 20%	C1, C2
			1	11	A	102-305-156	150D156X0020B2	56289	CAP., 15UF, 20V, 20%	C3
			1	12	A	102-001-473	230B1B473	14752	CAP., .047UF, 100V, 20%	C4
				13						
				14						
				15						
			1	16	A	104-056-106	IN751A	04713	DIODE	CR1
				17						
				18						
				19						
			1	20	A	100-003-911	RC07GF911J	81349	RES, 910Ω, 1/4W, 5%	R1
			3	21	A	100-017-101	RC05GF101J	81349	RES, 100Ω, 1/8W, 5%	R2, R3, R11
			3	22	A	100-017-152	RC05GF152J	81349	RES, 1.5K, 1/8 W, 5%	R4, R17, R23

DRAWN M. GRIES	CHECKED K. HOUSEAL	TITLE PARTS LIST PDC001-1	CODE IDENT NO. 20747	DWG NO. PL460-0985-501	REV F
DATE 8.17.72	DATE 9-10-72			SHEET 2 OF	

8C 38,

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			1	23	A	100-017-472	RC05GF472J	81349	RES., 4.7K, 1/8W, 5%	R5
			2	24	A	100-017-102	RC05GF102J	81349	RES., 1K, 1/8W, 5%	R6, R14
			1	25	A	100-017-332	RC05GF332J	81349	RES., 3.3K, 1/8W, 5%	R7
			6	26	A	100-017-153	RC05GF153J	81349	RES., 15K, 1/8W, 5%	R8-R10 R19, R21, R25
				27						
			2	28	A	100-017-242	RC05GF242J	81349	RES., 2.4K, 1/8W, 5%	R22, R26
			1	29	A	100-017-203	RC05GF203J	81349	RES., 20K, 1/8W, 5%	R13
			3	30	A	100-017-222	RC05GF222J	81349	RES., 2.2K, 1/8W, 5%	R12, R15, R18
			1	31	A	100-017-105	RC05GF105J	81349	RES., 1 MEG, 1/8W, 5%	R16
			1	32	A	100-017-103	RC05GF103J	81349	RES., 10K, 1/8W, 5%	R20
			1	33	A	100-017-123	RC05GF123J	81349	RES., 12K, 1/8W, 5%	R24
				34						
				35						
				36						
			2	37	A	103-304-001	2N4126	04713	TRANS.	Q1, Q3
			6	38	A	103-408-001	2N4124	04713	TRANS.	Q2, Q4-Q8
				39						
				40						
				41						
			1	42	A	139-209-002	CA3046	86684	I. C. TRANSISTOR ARRAY	U1
			1	43	A	139-046-442	DM7442N	01295	I. C. TTL	U5
			1	44	A	139-046-420	SN7420N-10	01295	I. C. TTL	U6

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
M. GRIES	K. HOUSEAL	PARTS LIST PDC001-1	20747	PL460-0985-501	F
DATE 8-17-72	DATE 9-10-72			SHEET 3 OF	

800-0438A

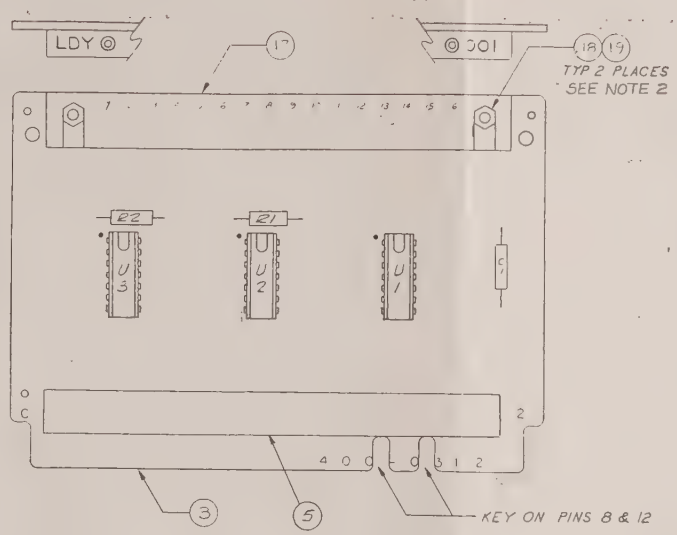
AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			2	45	A	139-046-404	SN7404N-10	01295	I.C., TTL	U4, U7
			1	46	A	139-046-402	SN7402N-10	01295	I.C., TTL	U2
			2	47	A	139-046-400	SN7400N-10	01295	I.C., TTL	U3, U9
			1	48	A	139-046-416	SN7416N-10	01295	I.C., TTL	U8
			1	49	A	139-046-410	SN7410N-10	01295	I.C., TTL	U10
				50						
				51						
				52						
			5	53	A	121-202-005	8041-1G7	91506	TEST JACK, GREEN	1-5
			1	54	A	121-202-010	8041-1G6	91506	TEST JACK, BLACK	GND
				55						
				56						
				57						
			AR	58	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571
				59						
				60						
				61						
				62						
				63						
				64						
				65						
				66						

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
M. GRIES	K. HOUSEAL	PARTS LIST	20747	PL460-0985-501	F
DATE 8-17-72	DATE 9-10-72	PDC001-1		SHEET 4 OF	

BC [illegible]SE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 460-1085B	9/27/72	F. HINKLE
	C	REVISED PER ECO 04220	12/7/72	F. HINKLE
	D	REVISED PER ECO 05185	6/11/73	6/14/73 JTD



PIN CONNECTIONS

I.C. PIN	CONN. PIN	TEST PT.	I.C. PIN	CONN. PIN	TEST PT.	I.C. PIN	CONN. PIN	TEST PT.
A1-1	15		A2-1	27		A3-1	40	
A1-2	14		A2-2	26		A3-2	39	
A1-3	13	11	A2-3	25	6	A3-3	38	1
A1-4	12		A2-4	24		A3-4	37	
A1-5	11		A2-5	23		A3-5	36	
A1-6	10	12	A2-6	22	7	A3-6	35	2
A1-7	2	16	A2-7	2	16	A3-7	2	16
A1-8	9	13	A2-8	21	8	A3-8	34	3
A1-9	8		A2-9	20		A3-9	33	
A1-10	7		A2-10	19		A3-10	32	
A1-11	6	14	A2-11	18	9	A3-11	31	4
A1-12	5		A2-12	17		A3-12	30	
A1-13	4		A2-13	16		A3-13	29	
A1-14	3		A2-14	3		A3-14	3	

NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO. 401-0010
2. TEST POINT BLOCK MOUNTING SCREW AND NUT (ITEM 18 & 19) ARE OPTIONAL, MANDATORY ONLY WHEN SPECIFIED ON MA OR ERN.

FOR SCHEMATIC SEE "C" SIZE 460-1085
FOR PARTS LIST SEE PL 460-1085-501

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501					LIST OF MATERIALS	

		DATE
DRAWN	F TOUT	3-28-73
CHECKED	R SCHOEN	3-27-73
DRAFTING	J SAMPEDRO	4-2-73
ENGINEER	J KOEHLER	3/30/73
MFG	P HELLER	4/2/73
APPROVED	R. CLEGG	3/3/73
APPROVED		

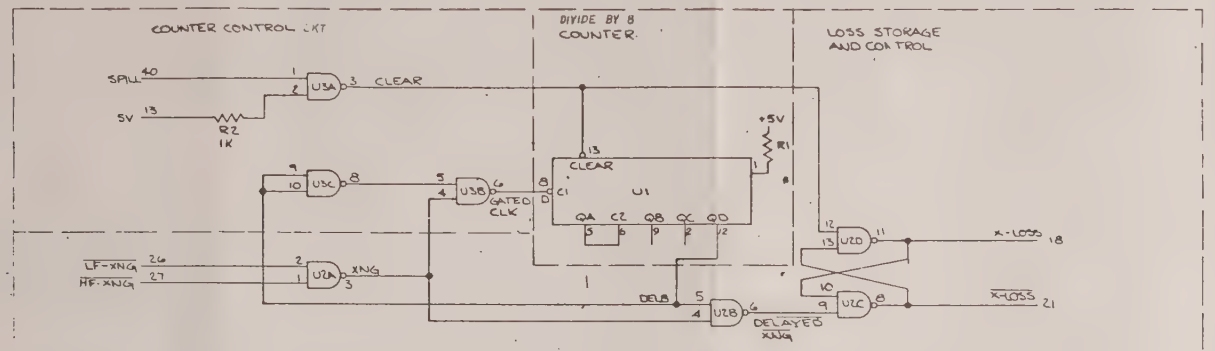
AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

CARD ASSEMBLY
LOSS DELAY
LDY-001-1

NEXT ASSY	USED ON
	9412
APPLICATION	

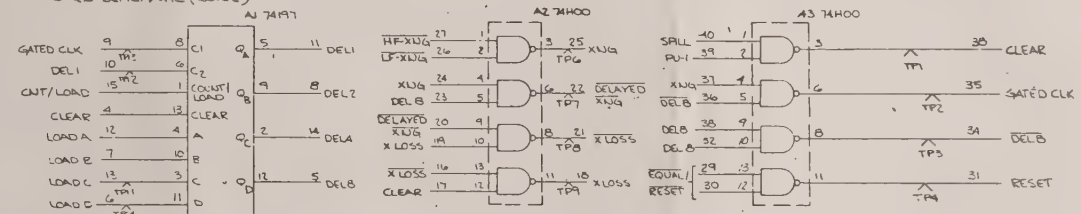
SIZE	CODE IDENT NO		REV
D	20747	460-1085-501	D

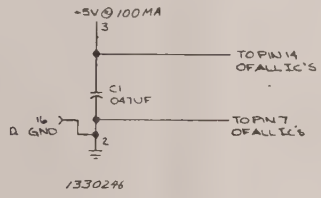
SCALE 2:1 SHEET 1 OF 2



LOGIC DIAGRAM (NOTE 1)

CARD SCHEMATIC (NOTE 2)





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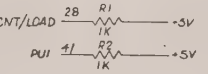


NOTES:

1. LOGIC DIAGRAM INCLUDES LIBRARY WIRING INTERCONNECTIONS
2. CARD SCHEMATIC SHOWS INTERCONNECTIONS OF CARD ONLY.
3. RESISTORS ARE IN OHMS

460-1085 B
SH 2

CONTRACT NO 9412	MONITOR SYSTEMS INC. FORT WASHINGTON PENNSYLVANIA		
DRAWN DATE	CARD ASSEMBLY LOSS DELAY TYPE LDY-001		
CHECKED			
DRAFTING			
ENGINEER			
APPROVED	SIZE A	CODE IDENT NO 20747	460-1085 REV B
DISTRIBUTION	SCALE	SHEET OF	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-1085B		7-9-73	F. HINKLE
C	REVISED PER ECO 04220 O.P.		7-2-79	F Hinkle

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	C	C																					

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
LOSS DELAY
LDY-001

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	F. TOUT.	3-28-73	ENGINEER	J. KOEHLER	3-30-73	DWG NO.		REV
CHECKED	N. SCHOEN	3-29-73	APPROVED	R. CLEGG	3-30-73	PL460-1085-501		C
DRAFTING	J. SAMPEDRO	4-2-73				SHEET 1 OF 2		

800-0066

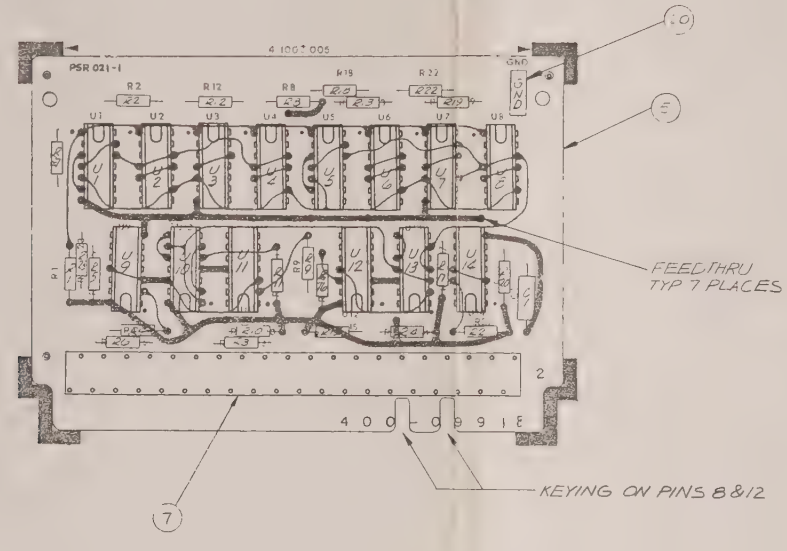
AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			REF	1	D	460-1085-501	———	20747	CARD ASSY & SCHEM	
				2						
			1	3	C	400-0312	———	20747	BD. PRINTED WIRING	
				4						
			1	5	A	108-203-040	7022-040-000-001	91662	CONNECTOR, FINGER BLOCK	
				6						
			1	7	A	102-001-473	230B1 B473	14752	CAP., .047UF, 100V, 20%	C1
				8						
				9						
			2	10	A	100-003-102	RC07GF102J	81349	RES., 1K, 1/4W, 5%	R1, R2
				11						
				12						
			1	13	A	139-046-197	SN74197N-10	01295	I.C. TTL	U1
			2	14	A	139-051-400	SN74H00N-10	01295	I.C. TTL	U2, U3
				15						
				16						
			1	17	A	108-900-001	SEE SPEC	03877	CONNECTOR, TEST POINT	
			2	18	A	127-109-014	MS51957-14	96906	SCREW, MACH, P.H., X-REC, CRES	4-40 X 5/16
			2	19	A	129-001-003	92-1660-40	72962	NUT, HEX, MINIATURE, 4-40	
				20						
				21						
			AR	22	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
F. TOUT.	N. SCHOEN	PARTS LIST	20747	PL460-1085-501	C
DATE 3-28-73	DATE 3-29-73	LDY-001		SHEET 2 OF 2	

800-[illegible]38A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 04220		



NOTES.
FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO 401-0010

FOR PARTS LIST SEE PL460-1096-501

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501			LIST OF MATERIALS			

DRAWN	N GOODMAN 7/23/73
CHECKED	
DRAFTING	E STUCKER 7.23.73
ENGINEER	J. ROEHLER 7-11-73
MFG	G L BROWN
APPROVED	R CLARK 7.24.73
APPROVED	

	4900
NEXT ASSY	USED ON
APPLICATION	

AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

CARD ASSEMBLY (PROGRAM STOR. RGTR) PSR 021-1

SIZE	CODE IDENT NO.		REV
D	20747	460-1096-501	B
SCALE 2:1		SHEET 1 OF 2	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 04220 D.P		7-16-79	[illegible]
C	REVISED PER ECO 04541 D.P.		1-7-79	J Heiker

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	C	C																					

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
(PROGRAM STOR. RGTR)
PSR 021-1

CODE IDENT 20747
CONTRACT NO. 4900

DRAWN	N. GOODMAN	7-17-73	ENGINEER	J. KOEHLER	7-19-73	DWG NO.		REV
CHECKED			APPROVED	R. CLEGG	7-23-73	PL460-1096-501		C
DRAFTING	E. STUCKER	7-23-73				SHEET 1 OF 2		

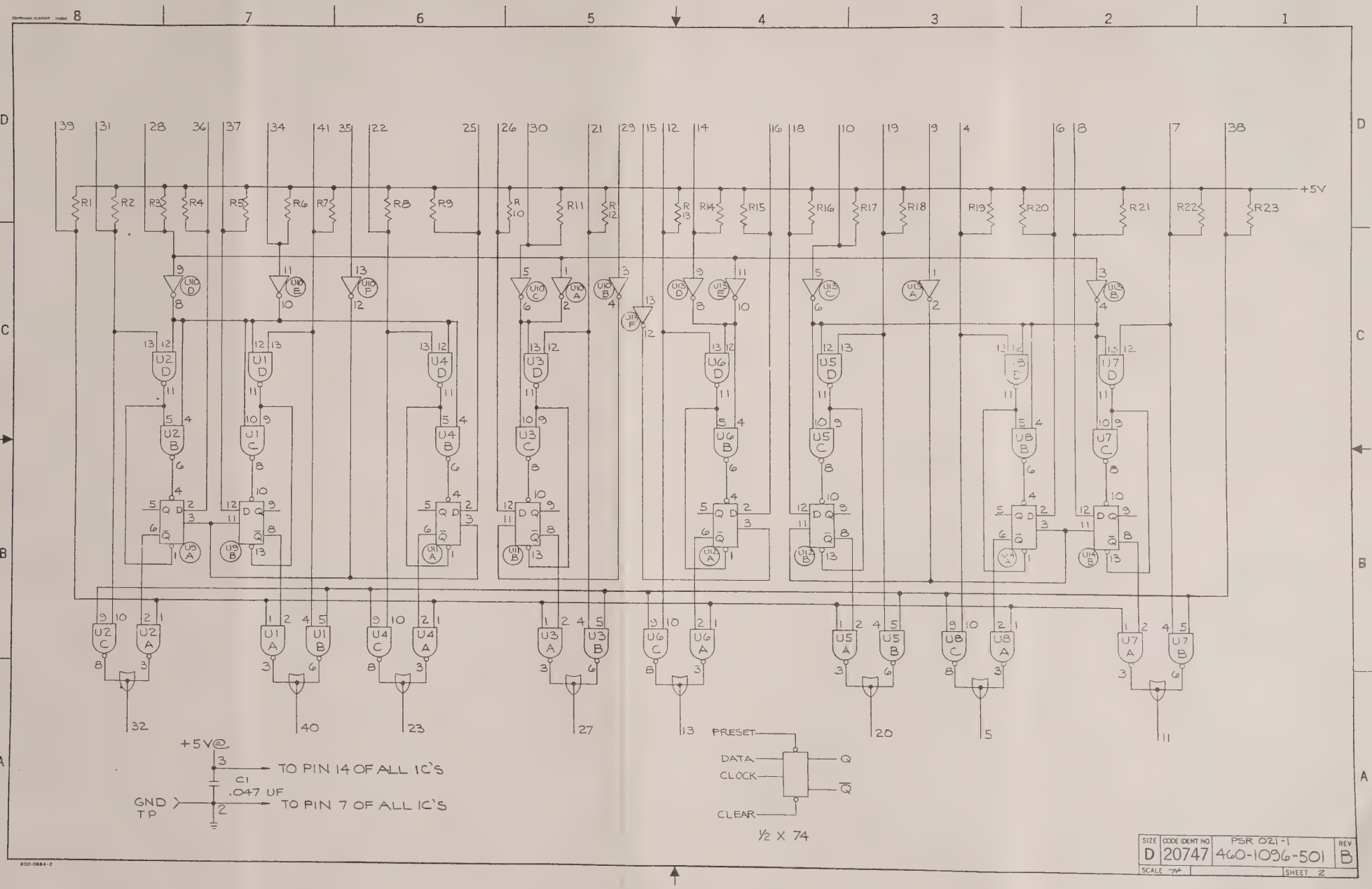
800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			REF	1	D	460-1096-501	———	20747	CARD ASS'Y & SCHEM	
				2						
				3						
				4						
			1	5	C	400-0991	———	20747	BD, PRINTED WIRING	
				6						
			1	7	A	108-203-040	7022-040-000-001	91662	CONNECTOR, FINGER BLOCK	
				8						
				9						
			1	10	A	102-001-473	230B1B473	14752	CAP, .047UF, 100V, 20%	C1
				11						
				12						
			23	13	A	100-003-682	RC07GF682J	81349	RES., 6.8K, 1/4W, 5%	R1 - R23
				14						
				15						
			8	16	A	139-045-846	SN15846N-10	01295	I.C., DTL	U1 - U8
			4	17	A	139-198-474	SN74LS74N-10	01295	I.C., TTL	U9, U11, U12, U14
			2	18	A	139-045-836	SN15836N-10	01295	I.C., DTL	U10, U13
				19						
			1	20	A	121-202-010	8041-1G6	91506	JACK, TEST, BLACK	
				21						
			AR	22	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
N. GOODMAN DATE 7.1 73	E. STUCKER DATE 7.23.73	PARTS LIST PSR 021	20747	PL460-1096-501 SHEET 2 OF	C

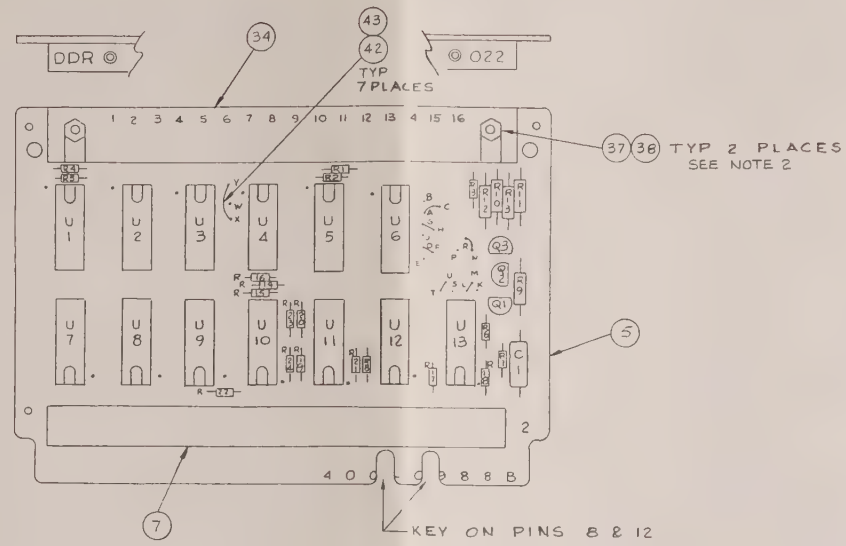
143DA



SIZE	CODE IDENT NO.	PSR 021-1	REV
D	20747	460-1096-501	B
SCALE -74		SHEET 2	

800-0684-2

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 460-0836B	[illegible]	D MOUAT
	C	REVISED PER ECO 460-0836C	[illegible]	J BOYTIM
	D	REVISED PER ECO 460-0836D	6-20-73	D MOUAT
	E	REVISED PER ECO 460-0836E	8-8-73	E STUCKER
	F	REVISED PER ECO 460-0836F	1-8-74	J. KOEHLER
	G	REVISED PER ECO 04220 D.P.	7-18-77	F Hinke
	H	REVISED PER ECO 04380 D.P.	8-24-79	D OM
	J	REVISED PER ECO 05185	[illegible]	JTZ



NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO. 401-0010.
2. TEST POINT BLOCK MOUNTING SCREW AND NUT (ITEM 37 & 38) ARE OPTIONAL, MANDATORY ONLY WHEN SPECIFIED ON MA OR ERN.

FOR SCHEMATIC SEE MICROFILM
FOR PARTS LIST SEE PL460-0836-501

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501	LIST OF MATERIALS					

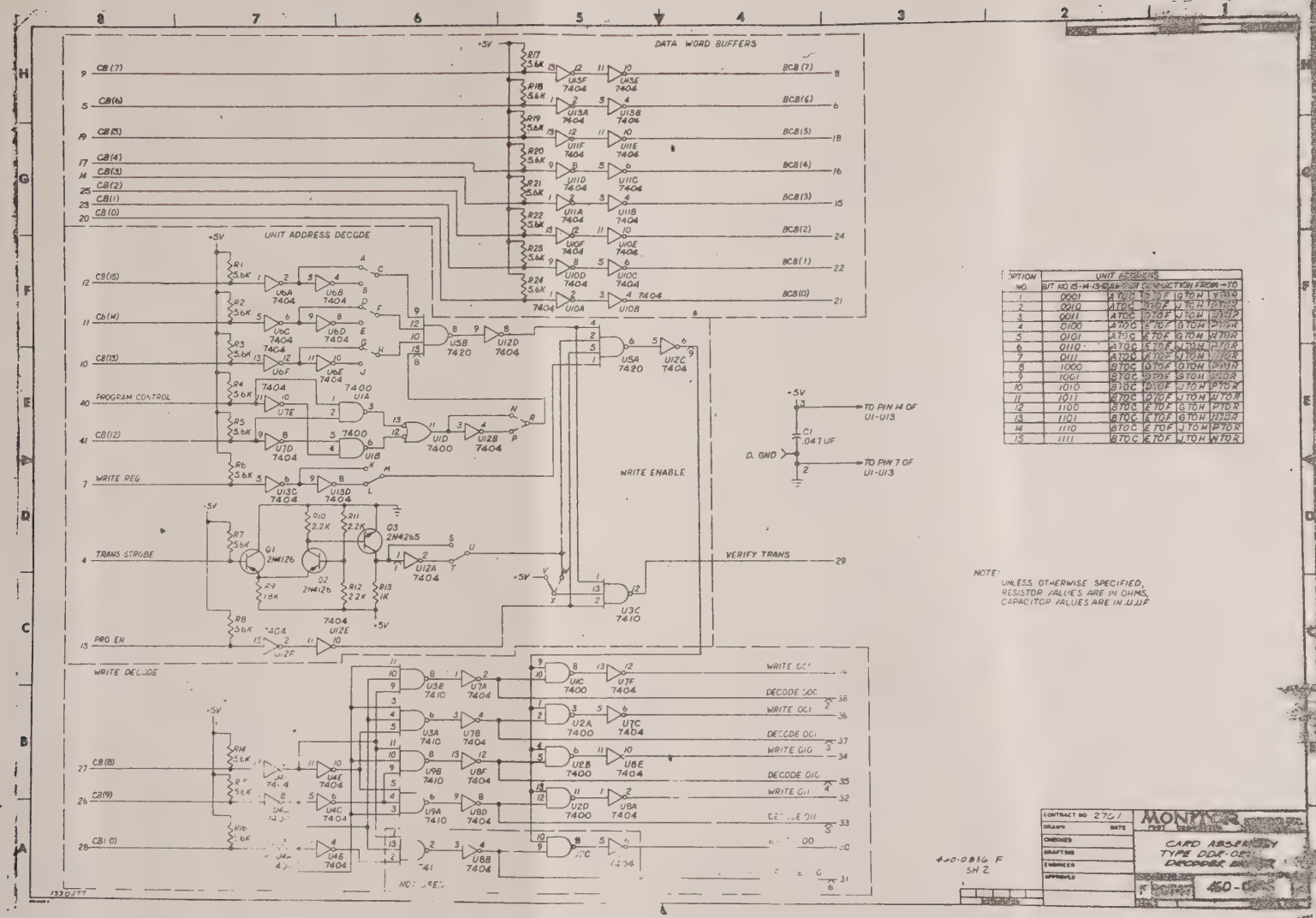
DRAWN M. GRIES	DATE 6-15-71
CHECKED J. DILELLO	
DRAFTING J. SAMPEDRO	
ENGINEER D. MOUAT	
MFG R. HELLER	
APPROVED R. CLEGG	8-9-71
APPROVED	

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

CARD ASSEMBLY
DECODER DRIVER
DDR 022-1

NEXT ASSY	USED ON
	2761
APPLICATION	

SIZE	CODE IDENT NO.		REV
D	20747	460-0836-501	J
SCALE 2:1		SHEET 1 OF 2	



OPTION NO.	UNIT ADDRESS BIT NO 15-14-13-12	POSITION CONNECTION FROM -Y0
1	0001	ATOC DTOF GTOH WTOR
2	0010	ATOC DTOF JTOH PTOR
3	0011	ATOC DTOF JTOH WTOR
4	0100	ATOC ETOF GTOH PTOR
5	0101	ATOC ETOF GTOH WTOR
6	0110	ATOC ETOF JTOH PTOR
7	0111	ATOC ETOF JTOH WTOR
8	1000	BTOC DTOF GTOH PTOR
9	1001	BTOC DTOF GTOH WTOR
10	1010	BTOC DTOF JTOH PTOR
11	1011	BTOC DTOF JTOH WTOR
12	1100	BTOC ETOF GTOH PTOR
13	1101	BTOC ETOF GTOH WTOR
14	1110	BTOC ETOF JTOH PTOR
15	1111	BTOC ETOF JTOH WTOR

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECC 460-0836B		9-15-71	D. MOUAT
C	REVISED PER ECC 460-0836C		10-3-72	J. BOYTIM
D	REVISED PER ECO 460-0836D		6-20-73	D. MOUAT
E	REVISED PER ECO 460-0836E		8-8-73	E. STUCKER
F	REVISED PER ECO 460-0836F		1-8-74	J. KOEHLER
G	REVISED PER ECO 04220 D.P.		7-18-79	J Hinkle

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	G	G	G																				

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE: PARTS LIST
DECODER DRIVER
DDR 022-1

CODE IDENT: 20747
CONTRACT NO.: 2761

DRAWN	M. GRIES	6-15-71	ENGINEER	D. MOUAT		DWG NO.	REV
CHECKED	J. DILELLO		APPROVED	R. CLEGG	8-9-71	PL460-0836-501	G
DRAFTING	J. SAMPEDRO					SHEET 1 OF 3	

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			REF	1	D	460-0836-501	———	20747	CARD ASSY & SCHEM	
				2						
				3						
				4						
			1	5	C	400-0988	———	20747	BOARD, PRINTED WIRING	
				6						
			1	7	A	108-203-040	7022-040-000-001	91662	CONNECTOR, FINGERBLOCK	
				8						
				9						
				10						
			1	11	A	102-001-473	230B1B473	14752	CAP., .047UF, 100V, 20%	C1
				12						
				13						
				14						
			1	15	A	103-403-001	2N4265	04713	TRANSISTOR	Q3
			2	16	A	103-304-001	2N4126	04713	TRANSISTOR	Q1, Q2
				17						
				18						
				19						
			19	20	A	100-017-562	RC05GF562J	81349	RES., 5.6K, 1/8W, 5%	R1-R8, R14-R24
			1	21	A	100-003-182	RC07GF182J	81349	RES., 1.8K, 1/4W, 5%	R9
			3	22	A	100-003-222	RC07GF222J	81349	RES., 2.2K, 1/4W, 5%	R10, R11, R12

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
M. GRIFS DATE 6-15-71	J. DILELLO DATE	PARTS LIST DDR-022	20747	PL460-0836-501 SHEET 2 OF	9

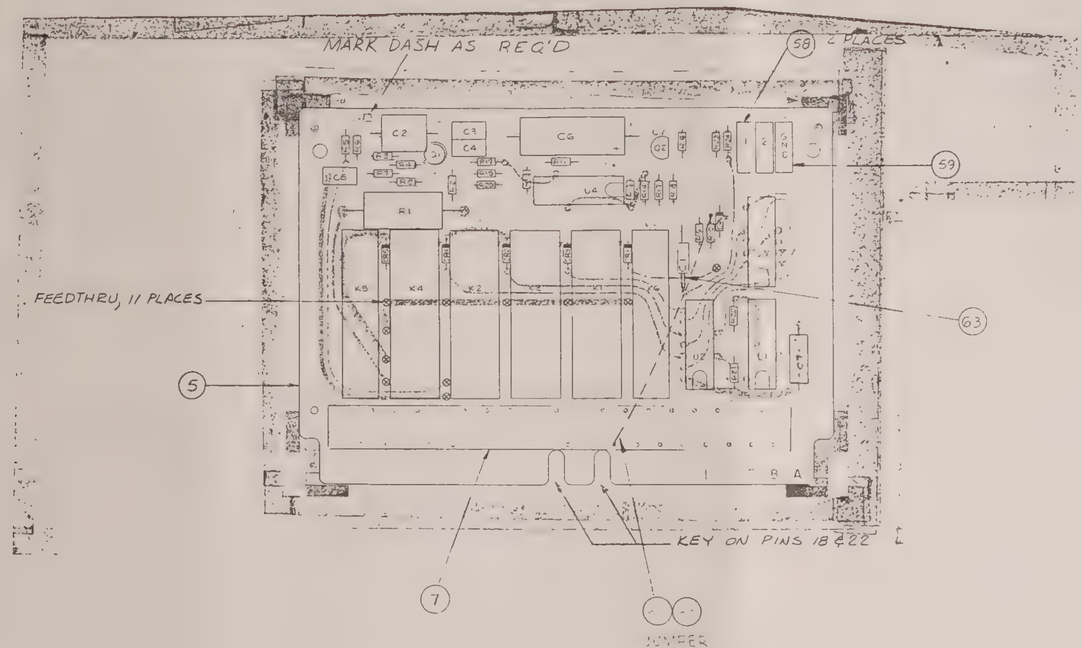
AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			1	23	A	100-003-102	RC07GF102J	81349	RES., 1K, 1/4W, 5%	R13
				24						
				25						
				26						
			1	27	A	139-046-420	SN7420N-10	01295	I.C. TTL	U5
			8	28	A	139-046-404	SN7404N-10	01295	I.C. TTL	U4, U6-U8 U10-U13
			2	29	A	139-046-410	SN7410N-10	01295	I.C. TTL	U3, U9
			2	30	A	139-046-400	SN7400N-10	01295	I.C. TTL	U1, U2
				31						
				32						
				33						
			1	34	A	108-900-001	SEE SPEC	03877	CONNECTOR, TEST POINT	
				35						
				36						
			2	37	A	127-109-014	MS51957-14	96906	SCREW, MACH, PH XRE: #4-40X5/16	
			2	38	A	129-001-003	92-1660-40	72962	NUT. HEX, MINIATURE #4-40	
				39						
				40						
				41						
			AR	42	A	113-001-006	299/1	92194	WIRE, BUS #26 AWG	
			AR	43	A	114-001-006	26.C18.C12W	03890	TUBING, TEFLON, WHT, #26AWG	
			AR	44	A	120-101-001	SN63B5	81348	SOLDER	QQ-S-571

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
M. GRIES	J. DILELLO	PARTS LIST DDR-022	20747	PL 460-[illegible]-401	G
DATE 6-15-71	DATE			SHEET 3 OF	

800-0438A

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 460-09868	[illegible]	F HINKLE
	C	REVISED PER ECO 460-09860	[illegible]	J KOEHLER
	D	REVISED PER ECO 460-0986D	[illegible]	KOEHLER
	E	REVISED PER ECO 02454	[illegible]	F HINKLE
	F	REVISED PER ECO 03236	[illegible]	F HINKLE
	G	REVISED PER ECO 04220	[illegible]	F.HINKLE
	H	REVISED PER ECO [illegible]	[illegible]	ES



NOTES:

1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG NO. 401-0010
2. R1 TO BE MOUNTED 1/16 OFF BOARD SURFACE

FOR SCHEMATIC SEE MICROFILM

FOR PARTS LIST SEE PL 460-0986-501/502/503

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501	LIST OF MATERIALS					

DRAWN	M GRIES 8-5-72
CHECKED	J WALLACE 9-6-7[illegible]
DRAFTING	J SAMPEDRO 10/25/72
ENGINEER	R. WASSERMAN 10-1[illegible]
MFG	R KELLER 10-26-72
APPROVED	R CLEGG 10-25-72
APPROVED	

NEXT ASSY	USED ON
	9412

APPLICATION

AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

CARD ASSEMBLY
INPUT SELECT BD
INP050-1, -2, -3

SIZE	CODE IDENT NO		REV
D	20747	460-0986-501/502/503	H

SCALE 2:1 SHEET 1 OF 2

800-0684-1

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-0986B		10·10·72	F. HINKLE
C	REVISED PER ECO 460-0986C		10·26·72	J. KOEHLER
D	SEE CO460-0986D		12·5·73	J. KOEHLER
E	ADDED-2 PER ECO 02454		8·30·77	F. HINKLE
F	REVISED PER ECO 03236		5·8·78	F. HINKLE
G	REVISED PER ECO 04220 D.P.		7-2-79	F. Hinkle
H	REVISED PER ECO 06791		10-5-81	ES

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	H	G	H	H																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
INPUT SELECT
INP050-1,-2,-3

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	M. GRIES	8-15-72	ENGINEER	R. WASSERMAN	10-17-72	DWG NO.	501 502	REV
CHECKED	J. WALLACE	9-6-72	APPROVED	R. CLEGG	10-25-72	PL 460-0986-503		H
DRAFTING	J. SAMPEDRO	10-25-72				SHEET 1 OF 4		

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
	—	—	REF	1	D	460-0986-501	———	20747	CARD ASSY & SCHEM	
	—	REF	—	2	D	460-0986-502	———	20747	CARD ASSY & SCHEM	
	REF	—	—	3	D	460-0986-503	———	20747	CARD ASSY & SCHEM	
				4						
	1	1	1	5	C	400-1178	———	20747	BD, PRINTED WIRING	
				6						
	1	1	1	7	A	108-203-040	7022-040-000-001	91662	CONNECTOR, FINGER BLOCK	
				8						
				9						
				10						
	1	1	1	11	A	102-001-473	230B1B473	14752	CAP., .047UF, 100V, 20%	C7
	1	1	1	12	A	102-305-107	150D107X002052	56289	CAP., 100UF, 20V, 20%	C6
	5	5	5	13	A	102-419-104	8131M100651104M	72982	CAP., 0.1UF, 100V, 20%	C1-C5
				14						
				15						
				16						
	6	6	6	17	A	104-503-014	IN4531	01295	DIODE	CR1-CR6
				18						
				19						
				20						
	4	4	4	21	A	106-016-001	365-4-2A	20891	RELAY, REED	K1-K4
	2	2	2	22	A	106-016-002	365-4-1A	20891	RELAY, REED	K5, K6

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
M. GRIES	J. WALLACE	PARTS LIST INPO50-1,-2,-3	20747	PL460-0986-501 -502-503	G
DATE 8-15-72	DATE 9-6-72			SHEET 2 OF	

800-0

A. JIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
				23						
				24						
				25						
				26						
	1	1	1	27	A	103-350-002	2N4857	01295	TRANSISTOR	Q1
	1	1	1	28	A	103-408-001	2N4124	04713	TRANSISTOR	Q2
				29						
				30						
				31						
	1	-	1	32	A	100-009-510	RC42GF510J	81349	RES., 51Ω, 2W, 5%	R1
	-	1	-	33	A	100-009-750	RC42GF750J	↑	↑ ,75Ω, 2W, 5%	R1
	2	2	2	34	A	100-017-221	RC05GF221J	↑	↑ ,220Ω, 1/8W, 5%	R2, R8
	4	4	4	35	A	100-017-101	RC05GF101J	↑	↑ ,100Ω, 1/8W, 5%	R3, R11, R12, R15
	4	4	4	36	A	100-017-102	RC05GF102J	↑	↑ ,1K, 1/8W, 5%	R4, R7, R23, R24
	1	1	1	37	A	100-017-103	RC05GF103J	↑	↑ ,10K, 1/8W, 5%	R5
	1	1	1	38	A	100-017-106	RC05GF106J	↑	↑ ,10MEG, 1/8W, 5%	R6
	1	1	1	39	A	100-017-470	RC05GF470J	↑	↑ ,47Ω, 1/8W, 5%	R9
	-	1	1	40	A	100-017-470	RC05GF470J	↑	↑ ,47Ω, 1/8W, 5%	R10
	1	-	-	41	A	100-017-151	RC05GF151J	↑	↑ ,150Ω, 1/8W, 5%	R10
	2	2	2	42	A	100-017-682	RC05GF682J	↑	↑ ,6.8K, 1/8W, 5%	R13, R14
	1	1	1	43	A	100-017-123	RC05GF123J	↑	↑ ,12K, 1/8W, 5%	R16
	1	1	1	44	A	100-017-272	RC05GF272J	81349	RES., 2.7K, 1/8W, 5%	R17

DRAWN M.GRIES DATE 8·15·72	CHECKED J.WALLACE DATE 9·6·72	TITLE PARTS LIST INP050-1,-2,-3	CODE IDENT NO. 20747	DWG NO. PL460-0986-501 -502,-503 SHEET 3 OF	REV H

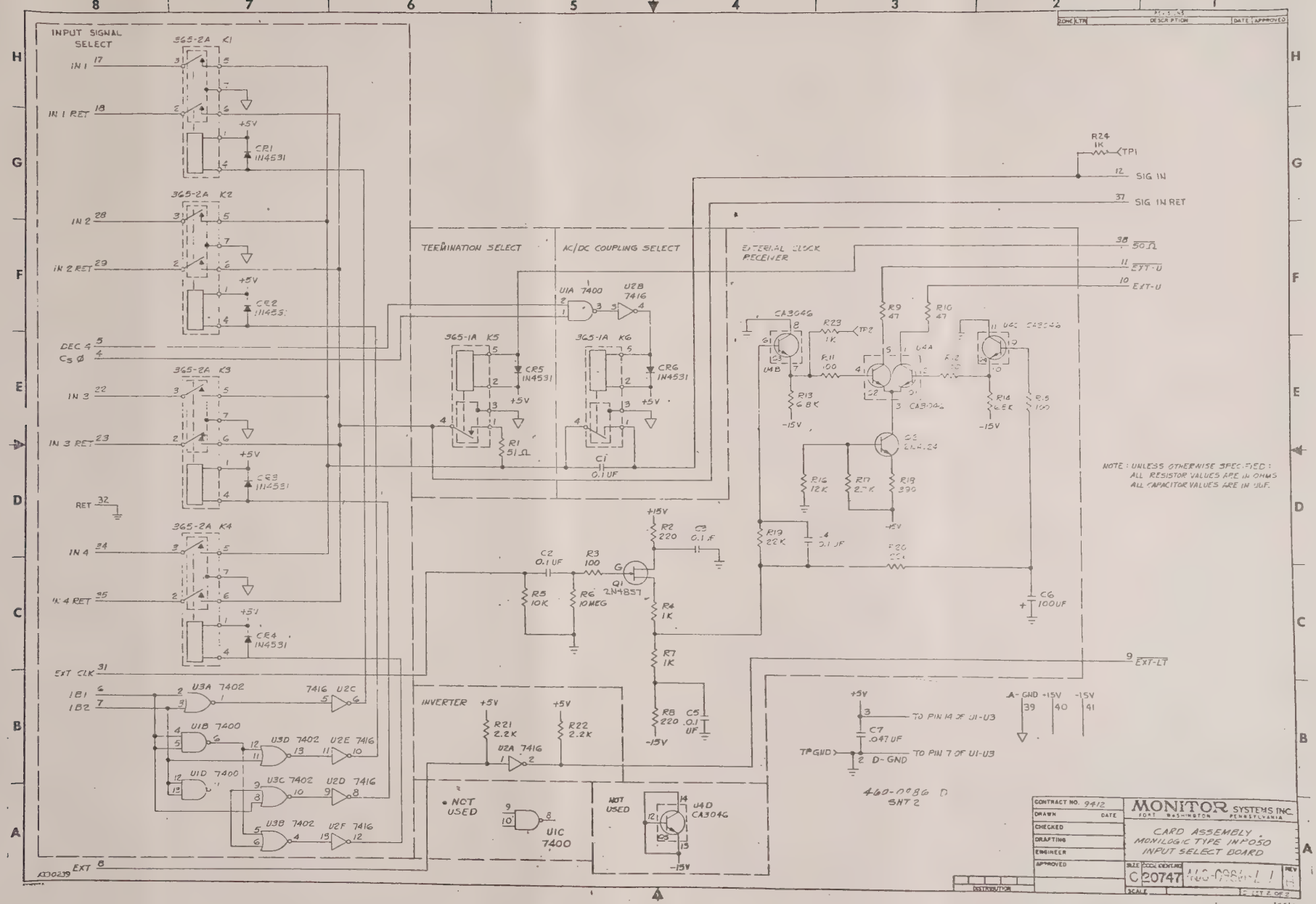
800-0438A

AYDIN MONITOR SYSTEMS

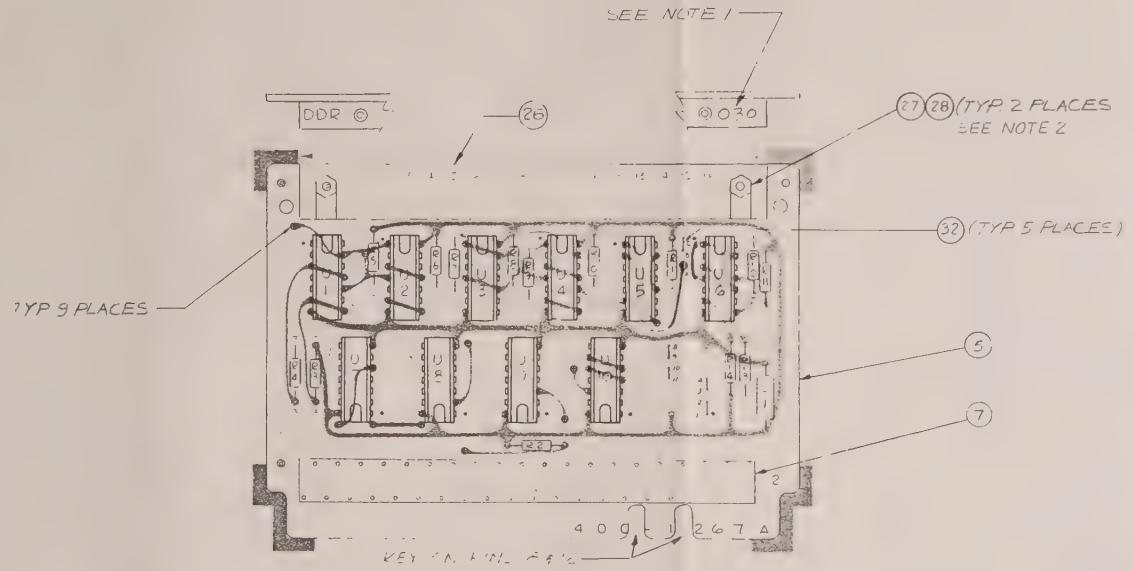
QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
	1	1	1	45	A	100-017-391	RC05GF391J	81349	RES., 390Ω, 1/8W, 5%	R18
	2	2	2	46	A	100-017-223	RC05GF223J	81349	RES., 22K, 1/8W, 5%	R19, R20
	2	2	2	47	A	100-017-222	RC05GF222J	81349	RES., 2.2K, 1/8W, 5%	R21, R22
				48						
				49						
				50						
	1	1	1	51	A	139-046-402	SN7402N-10	01295	I.C. TTL	U3
	1	1	1	52	A	139-046-400	SN7400N-10	01295	I.C. TTL	U1
	1	1	1	53	A	139-046-416	SN7416N-10	01295	I.C. TTL	U2
	1	1	1	54	A	139-209-002	CA3046	86684	I.C. TRANSISTOR ARRAY	U4
	1	1	1	55	A	131-013-001	2N4857	07047	PAD, TRANSISTOR	Q1
				56						
				57						
	2	2	2	58	A	121-202-005	8041-1G7	91506	TEST JACK, GREEN	1, 2
	1	1	1	59	A	121-202-010	8041-1G6	91506	TEST JACK, BLACK	GND
				60						
				61						
	AR	-	-	62	A	113-001-006	299/1	92194	WIRE, BUS #26 AWG	
	AR	-	-	63	A	114-001-006	26.018.012WHT	03890	TUBING, TEFLON, #26 AWG, WHT	
				64						
				65						
	AR	AR	AR	66	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571

DRAWN M. GRIES DATE 8-15-72	CHECKED J. WALLACE DATE 9-6-72	TITLE PARTS LIST INP050-1,-2,-3	CODE IDENT NO. 20747	DWG NO. -502,-503 PL460-0986-501 SHEET 4 OF	REV H

800-0438A


INPUT SIGNAL SELECT
IN 1
IN 1 RET
IN 2
IN 2 RET
DEC 4
Cs Ø
IN 3
IN 3 RET
RET
IN 4
IN 4 RET
EXT CLK
IB1
IB2
EXT
365-2A K1
365-2A K2
365-2A K3
365-2A K4
CR1 1N4531
CR2 1N4531
CR3 1N4531
CR4 1N4531
U3A 7402
U1B 7400
U1D 7400
U3D 7402
U3C 7402
U3B 7402
U2C 7416
U2E 7416
U2D 7416
U2F 7416
TERMINATION SELECT
AC/DC COUPLING SELECT
EXTERNAL CLOCK RECEIVER
U1A 7400
U2B 7416
365-1A K5
365-1A K6
CR5 1N4531
CR6 1N4531
R1 51Ω
C1 0.1 UF
R24 1K
TP1
SIG IN
SIG IN RET
50Ω
EXT-U
EXT-U
CA3046
R23 1K
TP2
R9 47
R10 47
R11 100
R13 6.8K
R14 6.8K
R15 100
R16 12K
R17 2.7K
R18 390
R19 22K
C6 100UF
Q2 2N4124
NOTE: UNLESS OTHERWISE SPECIFIED:
ALL RESISTOR VALUES ARE IN OHMS
ALL CAPACITOR VALUES ARE IN UUF.
+15V
R2 220
C3 0.1 UF
C2 0.1 UF
R3 100
Q1 2N4857
R5 10K
R6 10MEG
R4 1K
R7 1K
R8 220
C5 0.1 UF
-15V
INVERTER
R21 2.2K
R22 2.2K
U2A 7416
NOT USED
U1C 7400
NOT USED
U4D CA3046
TO PIN 14 OF U1-U3
C7 .047 UF
TP GND
D-GND
TO PIN 7 OF U1-U3
A-GND
+15V
-15V
460-0986 D
SHT 2
CONTRACT NO. 9412
DRAWN
DATE
CHECKED
DRAFTING
ENGINEER
APPROVED
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
MONILOGIC TYPE IMP050
INPUT SELECT BOARD
SIZE C
CODE IDENT NO 20747
REV
SCALE
SHEET 2 OF 2
DISTRIBUTION
A30239

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
		REVISED PER ECO 460-1097B	7-6-73	J KOEHLER
		REVISED PER ECO 460-1097C	1-2-74	F HINKLE
		REVISED PER ECO 04200		
		REVISED PER ECO 05081		
		REVISED PER ECO 05152		
		[illegible]		



NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO. 401-0010
2. TEST POINT BLOCK MOUNTING SCREW AND NUT (ITEM 7 & 28) ARE OPTIONAL, MANDATORY ONLY WHEN SPECIFIED ON MA OR ERN.

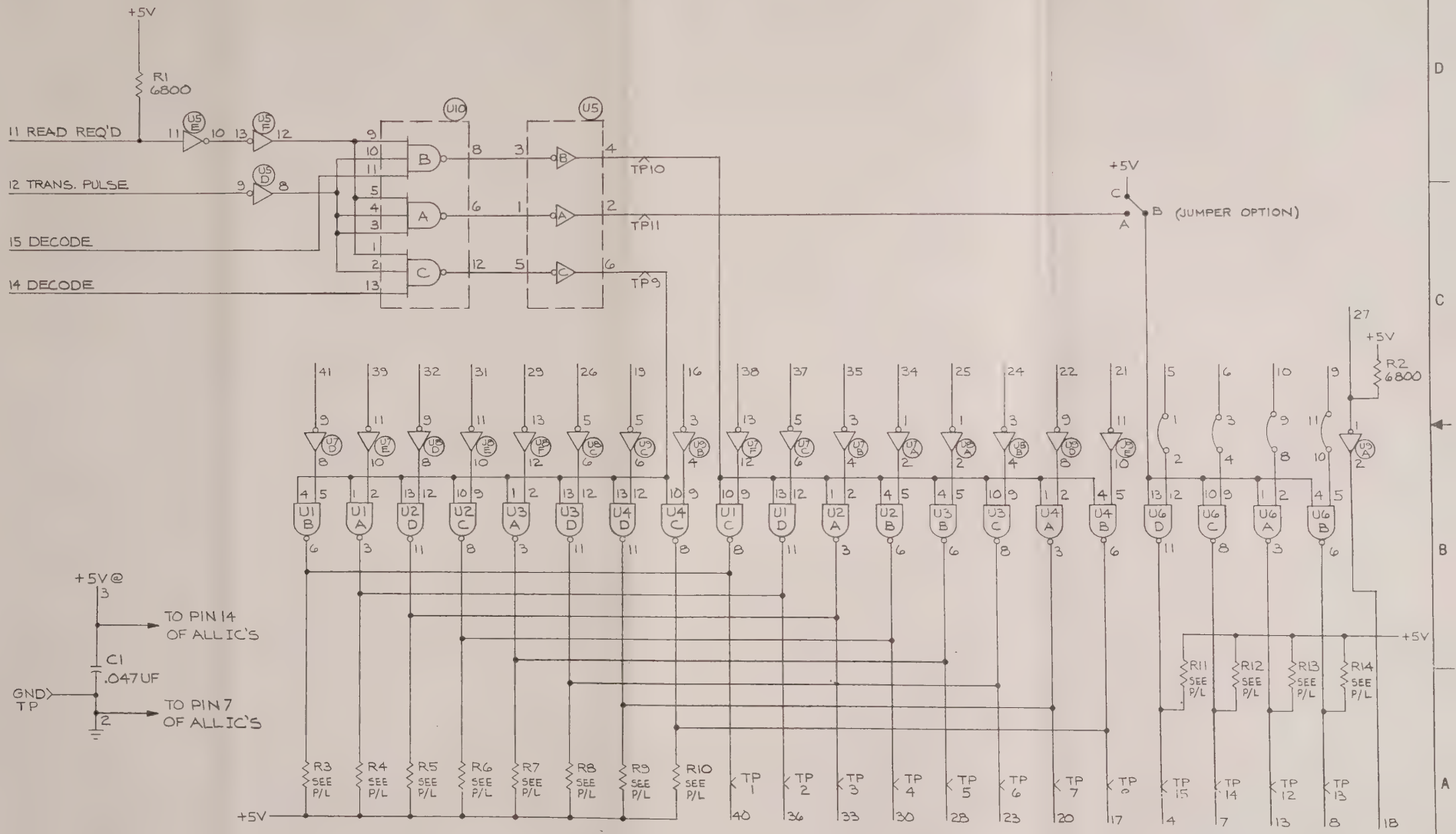
FOR PARTS LIST SEE PL 460-1097-☐

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501	LIST OF MATERIALS					

DRAWN N GOODMAN DATE 7-17-73	AYDIN MONITOR SYSTEMS FORT WASHINGTON PENNA 19034
CHECKED	
DRAFTING E STUCKER 7-23-73	CARD ASSEMBLY 16 BIT VERIFY DDR030-[illegible]
ENGINEER J KOEHLER [illegible]	
MFG	
APPROVED R CLEGG 7-23-73	SIZE D · CODE IDENT NO 20747 · 460-1097-[illegible] · REV [illegible]
APPROVED	SCALE 2 1 · SHEET 1 OF 2

NEXT ASSY	USED ON
	4900
APPLICATION	

800 0684-1



SIZE	CODE IDENT NO.	DDR030-1	REV
D	20747	460-1097-501	F
SCALE		SHEET 2 OF 2	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	SEE CO 460-1097 B		7·26·73	J. KOEHLER
C	REVISED PER ECO 460-1097C		1·2·74	F. HINKLE
D	REVISED PER ECO 04220 D.R		7-16-79	F. Hinkle
E	ADDED -502 PER ECO 05081 JST		5-8-80	F Hinkle
G	REVISED PER ECO°07280 JSG		18FEB82	RS Volz

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	G	G																					

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
16 BIT VERIFY
DDR 030-1

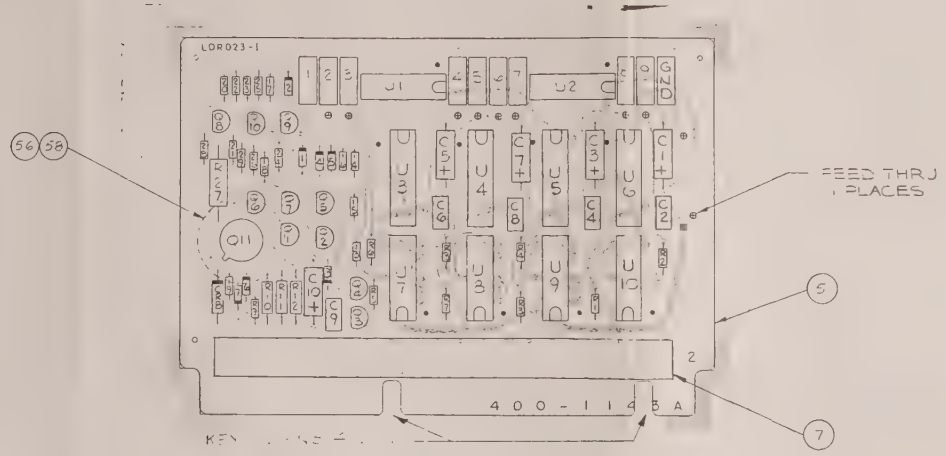
CODE IDENT 20747
CONTRACT NO. 4900

DRAWN	N.GOODMAN	7·17·73	ENGINEER	J. KOEHLER	7·19·73	DWG NO.	REV
CHECKED	————		APPROVED	R. CLEGG	7·23·73	PL460-1097-501	G
DRAFTING	E. STUCKER	7·23·73				SHEET 1 OF 2	

800-0068

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DE
		460-1097-501		G	PARENT DDR030-1	
1	005	400-1267			BOARD P.W. MONI 1	
1	007	108-203-040	7022-040-000001	C	CONN FING BLOC 40 POS	
1	010	102-001-473	230B1B473	H	CAP .047UF 100V 20%	C1
2	014	100-003-682	RC07	D	RES 6.8K 1/4W 5%	R1
						R2
12	015	100-003-SBT	RC07	D	RES SBT 1/4W 5%	R3
						R4
						R5
						R6
						R7
						R8
						R9
						R10
						R11
						R12
						R13
						R14
5	019	139-046-403	139-046-403	A/P	IC TTL 14 PIN	U1
						U2
						U3
						U4
						U6
1	020	139-046-404	SN7404N-10	A/P	IC TTL 14 PIN	U5
3	021	139-045-836	SN15836N-10	E	IC DTL 14 PIN	U
						U9
1	022	139-046-410	SN7410N-10	A/P	IC TTL 14 PIN	U10
1	026	108-900-001	UTP-16-30T	E	CONN PC TEST PT	
2	027	127-109-014	MS51957-14	A	SCR PAN HD 4-40X5\16	
2	028	129-001-003	92-1660-40	C	NUT HEX LK MINTR 4-40	
0	032	113-001-006	299/1	C	WIRE BUS 26 AWG	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 460-0949B	12-5-72	FG HINKLE
	C	REVISED PER ECO 460-0949C	5-15-73	FG HINKLE
	D	REVISED PER ECO 02082	3-16-79	J MATHER
	E	REVISED PER ECO 04220	7-16-79	J Mather



NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO 401-0010
2. MAX COMPONENT PROFILE .437

FOR SCHEMATIC SEE MICRO FILM
FOR PARTS LIST SEE PL460-0949-501

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
SOI			LST OF MATERIALS			

DRAWN	M. LEIBSON	DATE 8-10-72
CHECKED	J HARTZELL	8/24/72
DRAFTING	J SAMPEDRO	8-19-72
ENGINEER	R Wasserman	6-23-72
MFG	R HELLER	8/10/72
APPROVED	R CLEGG	8/10/72
APPROVED		

AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA. 19034

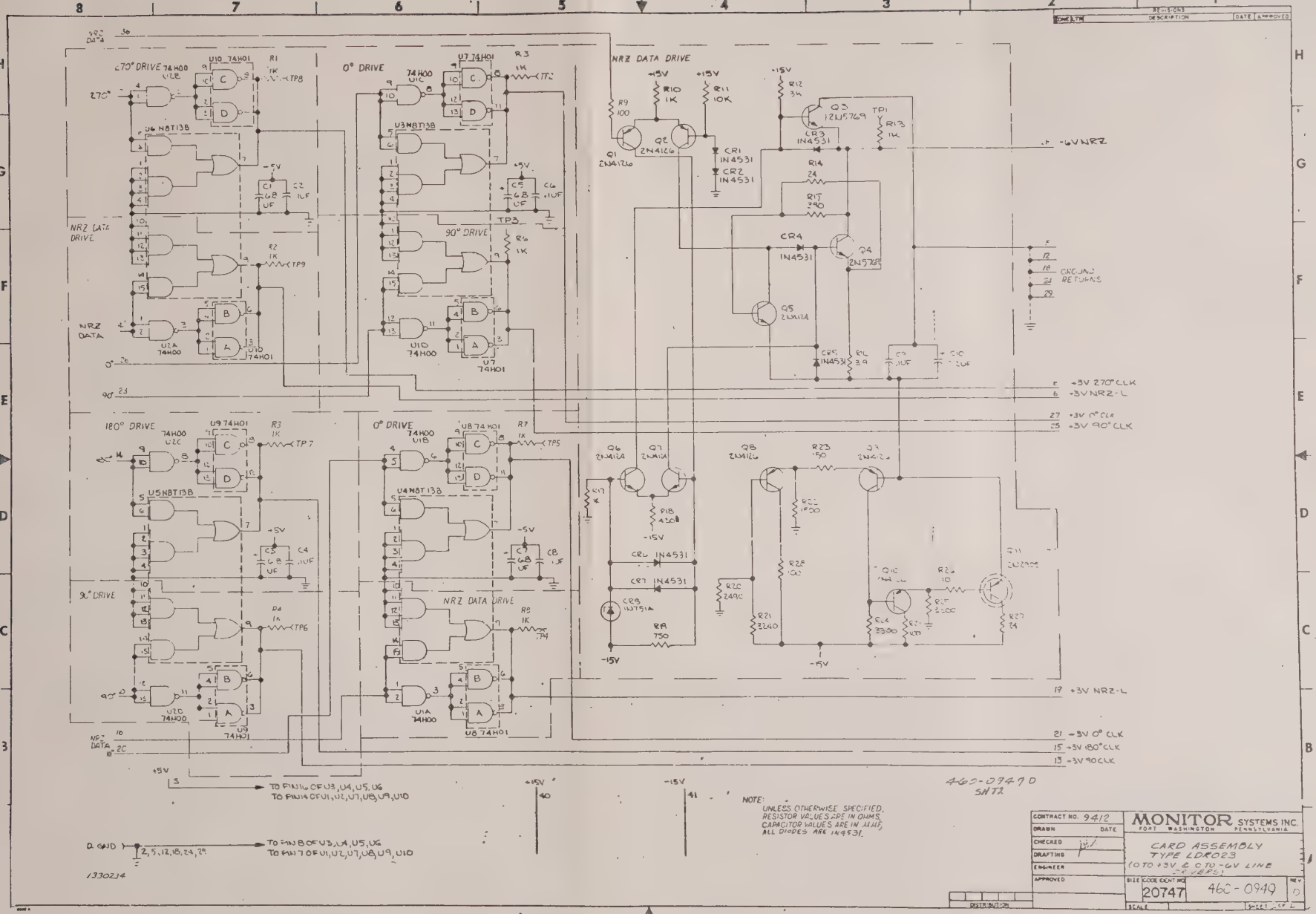
CARD ASSEMBLY
LINE DRIVERS
LDR023-1

NEXT ASSY	USED ON
	9412
APPLICATION	

SIZE	CODE IDENT NO		REV
D	20747	460-0949-501	E

SCALE 2" | SHEET 1 OF 2

800-0684-1



270° DRIVE
0° DRIVE
NRZ DATA DRIVE
90° DRIVE
180° DRIVE
NRZ DATA
-6V NRZ
GROUND RETURNS
+3V 270° CLK
+3V NRZ-L
+3V 0° CLK
+3V 90° CLK
+3V NRZ-L
+3V 0° CLK
+3V 180° CLK
+3V 90 CLK
TO PIN 16 OF U3, U4, U5, U6
TO PIN 14 OF U1, U2, U7, U8, U9, U10
TO PIN 8 OF U3, U4, U5, U6
TO PIN 7 OF U1, U2, U7, U8, U9, U10
D. GND
1330234
465-0949 D
SHT 2
NOTE:
UNLESS OTHERWISE SPECIFIED,
RESISTOR VALUES ARE IN OHMS,
CAPACITOR VALUES ARE IN μμF,
ALL DIODES ARE 1N4531.
CONTRACT NO. 9412
DRAWN
DATE
CHECKED
DRAFTING
ENGINEER
APPROVED
MONITOR SYSTEMS INC.
FORT WASHINGTON PENNSYLVANIA
CARD ASSEMBLY
TYPE LDR023
(0 TO +3V & 0 TO -6V LINE DRIVERS)
SIZE
CODE IDENT NO.
20747
46C-0949
REV
D
SCALE
SHEET
DISTRIBUTION

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-0949B		12-5-72	F. HINKLE
C	REVISED PER ECO 460-0949C		5-15-73	F. HINKLE
D	REVISED PER ECO 02082		3-16-77	J. MATHER
E	REVISED PER ECO 04220		7-16-79	F Hinkle

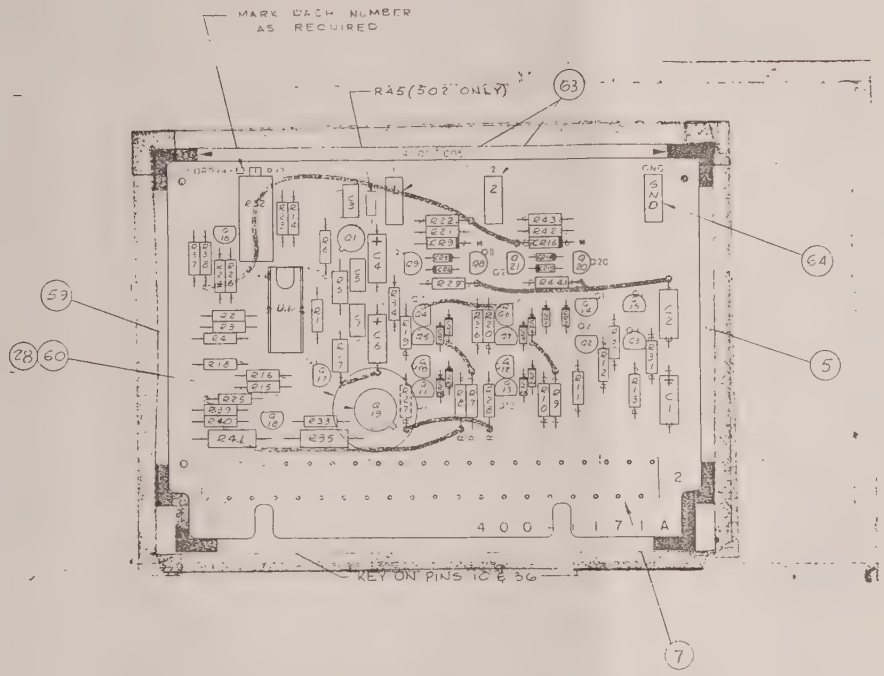
AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			REF	1	D	460-0949-501	———	20747	BD. ASSY. & SCHEM.	
				2						
				3						
				4						
			1	5	C	400-1143	———	20747	BD. PRINTED WIRING	
				6						
			1	7	A	108-203-040	7022-040-000-001	91662	CONNECTOR, FINGER BLOCK	
				8						
				9						
				10						
			4	11	A	102-313-685	150D685X0006A2	56289	CAP, 6.8UF, 6V, 20%	C1, C3, C5, C7
			5	12	A	102-419-104	8131M 100651104M	72982	CAP, .1UF, 100V, 20%	C2, C4, C6, C8, C9
			1	13	A	102-305-225	150D225X0020A2	56289	CAP, 2.2UF, 20V, 20%	C10
				14						
				15						
				16						
				17						
			7	18	A	104-503-014	IN4531	01295	DIODE	CR1-CR7
			1	19	A	104-056-106	IN751A	04713	DIODE, ZENER	CR8
				20						
				21						
				22						

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST LDR 023	20747	PL460-0949-501 SHEET 2 OF	F

800-043(

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 460-0380B	7/9/72	F. Hinkue
	C	REVISED PER ECO 02082	7/14/72	J Mather
	D	REVISED PER ECO 02654	1/3/73	F HINKLE
	E	REVISED PER ECO C4220	10-2-79	R Hinkle



NOTES.
FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO. 401-0010

FOR PARTS LIST SEE PL460-0380-501,-502

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501				LIST OF MATERIALS		

DRAWN	M GRIES 5-8-72
CHECKED	J SAMPEDRO 10-2-72
DRAFTING	J SAMPEDRO 10-2-72
ENGINEER	R WASSERMAN 10-9-72
MFG	R HELLER 10/16/72
APPROVED	R CLEGG 10/15/72
APPROVED	

AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

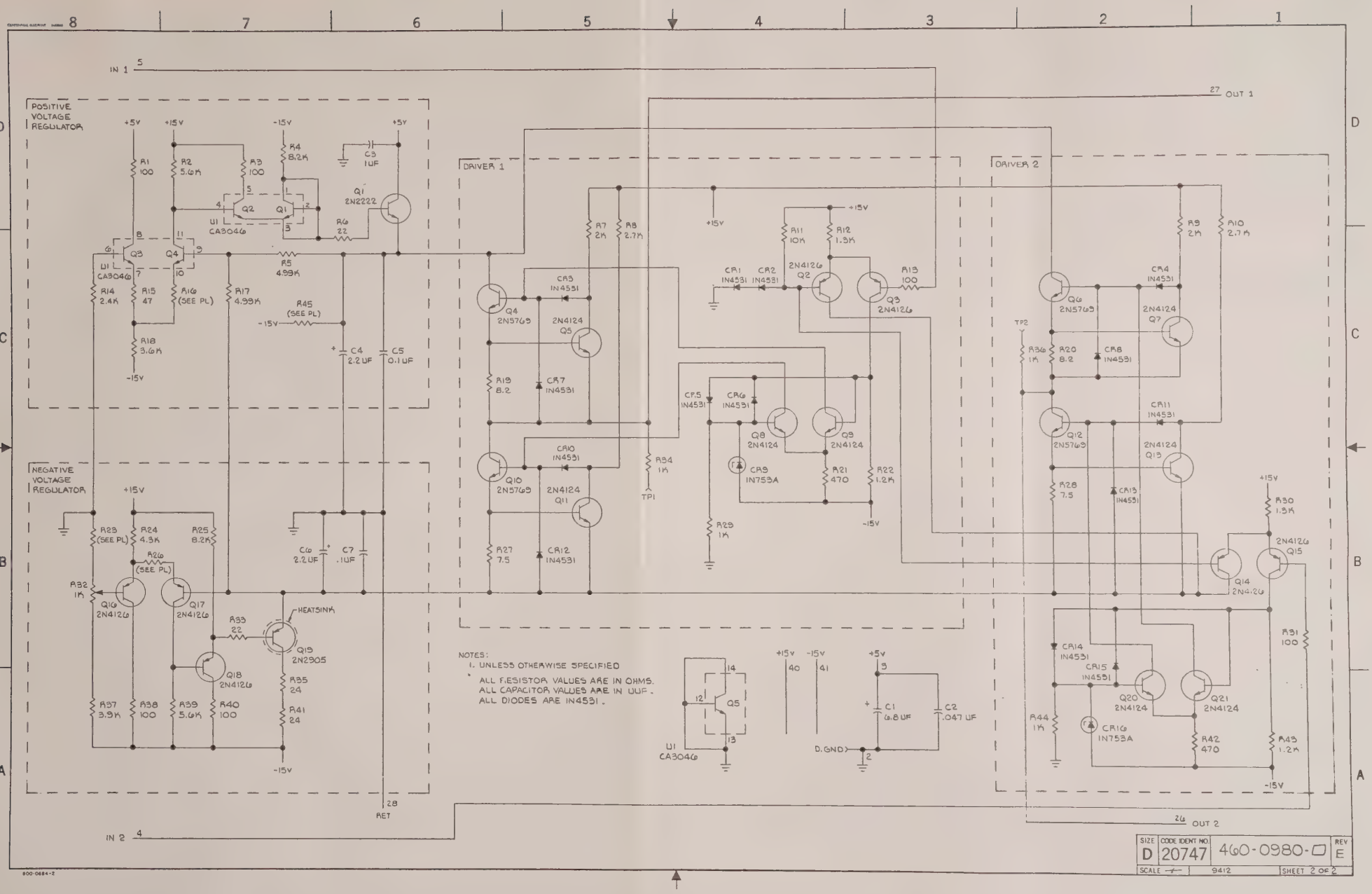
CARD ASSEMBLY
LINE DRIVERS
LDR024-1,-2

NEXT ASSY	USED ON
	9412
APPLICATION	

SIZE	CODE IDENT NO	- 501	REV
D	20747	460-0980-502	E

SCALE 2:1 SHEET 1 OF 2

800 0684 1


POSITIVE VOLTAGE REGULATOR
NEGATIVE VOLTAGE REGULATOR
DRIVER 1
DRIVER 2
IN 1
IN 2
OUT 1
OUT 2
RET
+5V
+15V
-15V
R1 100
R2 5.6K
R3 100
R4 8.2K
C3 1UF
Q1 2N2222
U1 CA3046
R6 22
R5 4.99K
R14 2.4K
R15 47
R16 (SEE PL)
R17 4.99K
R18 3.6K
R45 (SEE PL)
C4 2.2 UF
C5 0.1 UF
R23 (SEE PL)
R24 4.3K
R25 8.2K
R26 (SEE PL)
R32 1K
Q16 2N4126
Q17 2N4126
C6 2.2 UF
C7 .1UF
R33 22
HEATSINK
Q19 2N2905
Q18 2N4126
R35 24
R41 24
R37 3.9K
R38 100
R39 5.6K
R40 100
R7 2K
R8 2.7K
CR3 IN4531
Q4 2N5769
2N4124 Q5
R19 8.2
CR7 IN4531
Q10 2N5769
2N4124 Q11
CR10 IN4531
R34 1K
TP1
R27 7.5
CR12 IN4531
R29 1K
R11 10K
R12 1.3K
CR1 IN4531
CR2 IN4531
2N4126 Q2
Q3 2N4126
R13 100
CR5 IN4531
CR6 IN4531
Q8 2N4124
Q9 2N4124
CR9 IN753A
R21 470
R22 1.2K
R9 2K
R10 2.7K
CR4 IN4531
Q6 2N5769
2N4124 Q7
TP2
R36 1K
R20 8.2
CR8 IN4531
CR11 IN4531
Q12 2N5769
2N4124 Q13
R28 7.5
CR13 IN4531
R30 1.3K
Q14 2N4126
2N4126 Q15
R31 100
CR14 IN4531
CR15 IN4531
Q20 2N4124
Q21 2N4124
R44 1K
CR16 IN753A
R42 470
R43 1.2K
NOTES:
1. UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE IN OHMS.
ALL CAPACITOR VALUES ARE IN UUF.
ALL DIODES ARE IN4531.
U1 CA3046
Q5
C1 6.8 UF
C2 .047 UF
D. GND
40
41
SIZE D
CODE IDENT NO. 20747
460-0980-□
REV E
SCALE —
9412
SHEET 2 OF 2

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			5	23	A	103-304-001	2N4126	04713	TRANSISTOR	Q1,Q2,Q8-Q10
			2	24	A	103-440-001	2N5769	07263	TRANSISTOR	Q3,Q4
			3	25	A	103-408-001	2N4124	04713	TRANSISTOR	Q5-Q7
			1	26	A	103-314-202	2N2905	04713	TRANSISTOR	Q11
				27						
				28						
				29						
			10	30	A	100-017-102	RC05GF102J	81349	RES, 1K, 1/8W, 5%	R1-R8, R13, R17
			3	31	A	100-017-101	RC05GF101J	81349	RES, 100Ω, 1/8W, 5%	R9, R28, R29
			1	32	A	100-003-102	RC07GF102J	81349	RES, 1K, 1/4W, 5%	R10
			1	33	A	100-003-103	RC07GF103J	81349	RES, 10K, 1/4W, 5%	R11
			1	34	A	100-003-302	RC07GF302J	81349	RES, 3K, 1/4W, 5%	R12
			1	35	A	100-017-240	RC05GF240J	81349	RES, 24Ω, 1/8W, 5%	R14
			1	36	A	100-017-391	RC05GF391J	81349	RES, 390Ω, 1/8W, 5%	R15
			1	37	A	100-017-3R9	RC05GF3R9J	81349	RES, 3.9Ω, 1/8W, 5%	R16
			1	38	A	100-017-431	RC05GF431J	81349	RES, 430Ω, 1/8W, 5%	R18
			1	39	A	100-017-751	RC05GF751J	81349	RES, 750Ω, 1/8W, 5%	R19
			1	40	A	100-222-2491	RN50C2491F	81349	RES, 2.49K, 1/20W, 1%	R20
			1	41	A	100-222-3241	RN50C3241F	81349	RES, 3.24K, 1/20W, 1%	R21
			1	42	A	100-017-152	RC05GF152J	81349	RES, 1.5K, 1/8W, 5%	R22
			1	43	A	100-017-151	RC05GF151J	81349	RES, 150Ω, 1/8W, 5%	R23
			2	44	A	100-017-332	RC05GF332J	81349	RES, 3.3K, 1/8W, 5%	R24, R25

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST LDR 023	20747	PL460-0949-501 SHEET 3 OF	E

800-0438A

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
			1	45	A	100-017-100	RC05GF100J	81349	RES, 10Ω, 1/8W, 5%	R26
			1	46	A	100-005-240	RC20GF240J	81349	RES, 24Ω, 1/2W, 5%	R27
				47						
				48						
				49						
			2	50	A	139-051-400	SN74H00N-10	01295	I.C. TTL	U1, U2
			4	51	A	139-055-813	N8T13B	18324	I.C. DUAL LINE DRIVER.	U3-U6
			4	52	A	139-051-401	SN74H01N-10	01295	I.C. TTL	U7-U10
				53						
				54						
				55						
			1	56	A	131-021-001	10076	07047	PAD, TRANSISTOR	USE WITH Q11
				57						
			1	58	A	116-002-003	TXBF-032-025B	98978	HEAT SINK (TO-5 CASE)	USE WITH Q11
				59						
				60						
			9	61	A	121-202-005	8041-1G7	91506	TEST JACK, GREEN	
			1	62	A	121-202-010	8041-1G6	91506	TEST JACK, BLACK	GND
				63						
				64						
				65						
			AR	66	A	120-101-001	SN63BS	81349	SOLDER	QQ-S-571

DRAWN / DATE	CHECKED / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		PARTS LIST LDR 023	20747	PL460-0949-501 SHEET 4 OF	E

800-[illegible]9A
1431

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 460-0980B		10/25/72	F. HINKLE
C	REVISED PER ECO 02082		7/16/77	J. MATHER
D	REVISED PER ECO 02654		12.9.77	F. HINKLE
E	REVISED PER ECO 04220 DP		7-18-79	F Hinkle

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	E	E	E	E																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE: PARTS LIST
LINE DRIVERS
LDR024-1,-2

CODE IDENT 20747
CONTRACT NO. 9412

DRAWN	M. GRIES	8-8-72	ENGINEER	R. WASSERMAN	10-9-72	DWG NO.	-501	REV
CHECKED	J. SAMPEDRO	10-2-72	APPROVED	R. CLEGG	10-25-72	PL460-0980-502		E
DRAFTING	J. SAMPEDRO	10-2-72				SHEET 1 OF 4		

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		–	REF	1	D	460-0980-501	———	20747	CARD ASSY & SCHEM	
		REF	–	2	D	460-0980-502		20747	CARD ASSY & SCHEM	
				3						
				4						
		1	1	5	C	400-1171	———	20747	BOARD, PRINTED WIRING	
				6						
		1	1	7	A	108-203-040	7022-040-000-001	91662	CONNECTOR, FINGERBLOCK	
				8						
				9						
				10						
		1	1	11	A	102-313-685	150D685X0006A2	56289	CAP., 6.8UF, 6V, 20%	C1
		1	1	12	A	102-001-473	230B1B473	14752	CAP., .047UF, 100V, 20%	C2
		3	3	13	A	102-419-104	8131M10065104M	72982	CAP., .1UF, 100V, 20%	C3, C5, C7
		2	2	14	A	102-305-225	150D225X0020A2	56289	CAP., 2.2UF, 20V, 20%	C4, C6
				15						
				16						
				17						
		14	14	18	A	104-503-014	IN4531	01295	DIODE	CR1-CR8 CR10-CR15
		2	2	19	A	104-056-105	IN753A	04713	DIODE, ZENER	CR9, CR16
				20						
				21						
				22						

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
M. GRIES DATE 8·8·72	J. SAMPEDRO DATE 10·2·72	PARTS LIST LDR024	20747	PL460-0980-□ SHEET 2 OF	E

800-4311

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	23	A	103-019-001	2N2222	04713	TRANSISTOR	Q1
		7	7	24	A	103-304-001	2N4126	04713	TRANSISTOR	Q2, Q3, Q14-Q18
		4	4	25	A	103-440-001	2N5769	07263	TRANSISTOR	Q4, Q6, Q10,
		8	8	26	A	103-408-001	2N4124	04713	TRANSISTOR	Q5, Q7, [illegible]
				27						Q9, Q11, Q[illegible] Q20, Q21
		1	1	28	A	103-314-202	2N2905	04713	TRANSISTOR, TO-5	Q19
				29						
		1	-	30	A	100-017-242	RC05GF242J	81349	RES., 2.4K, 1/8W, 5%	R45
		2	-	31	A	100-003-2R7	RC07GF2R7J		, 2.7Ω, 1/4W, 5%	R16, R23
		6	6	32	A	100-003-101	RC07GF101J		, 100Ω, 1/4W, 5%	R1, R3, R13, R31, R38, R40
		2	2	33	A	100-003-562	RC07GF562J		, 5.6K, 1/4W, 5%	R2, R39
		2	2	34	A	100-003-822	RC07GF822J		, 8.2K, 1/4W, 5%	R4, R25
		2	2	35	A	100-003-8R2	RC07GF8R2J		, 8.2Ω, 1/4W, 5%	R19, R20
		2	2	36	A	100-215-4991	RN55D4991F		, 4.99K, 1/10W, 1%	R5, R17
		2	2	37	A	100-003-220	RC07GF220J		, 22Ω, 1/4W, 5%	R6, R33
		2	2	38	A	100-003-202	RC07GF202J		, 2K, 1/4W, 5%	R7, R9
		2	2	39	A	100-003-272	RC07GF272J		, 2.7K, 1/4W, 5%	R8, R10
		1	1	40	A	100-003-103	RC07GF103J		, 10K, 1/4W, 5%	R11
		2	2	41	A	100-003-132	RC07GF132J		, 1.3K, 1/4W, 5%	R12, R30
		1	1	42	A	100-003-242	RC07GF242J		, 2.4K, 1/4W, 5%	R14
		1	1	43	A	100-003-470	RC07GF470J		, 47Ω, 1/4W, 5%	R15
		1	1	44	A	100-003-362	RC07GF362J	81349	RES., 3.6K, 1/4W, 5%	R18

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
M. GRIES DATE 8-8-72	J. SAMPEDRO DATE 10-2-72	PARTS LIST LDR 024	20747	PL460-0980-[illegible] SHEET 3 OF	E

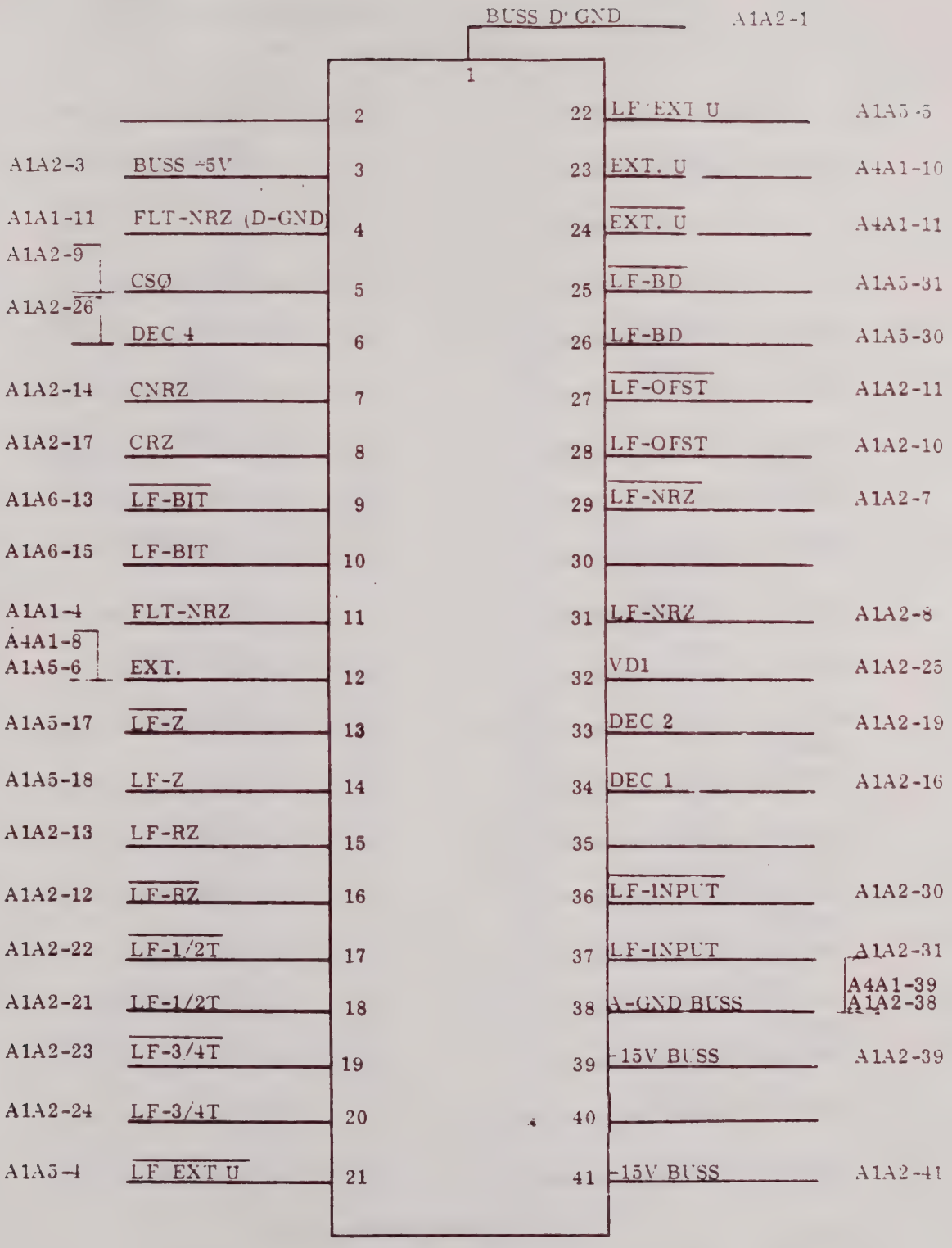
800-0438A

AYDIN MONITOR SYSTEMS

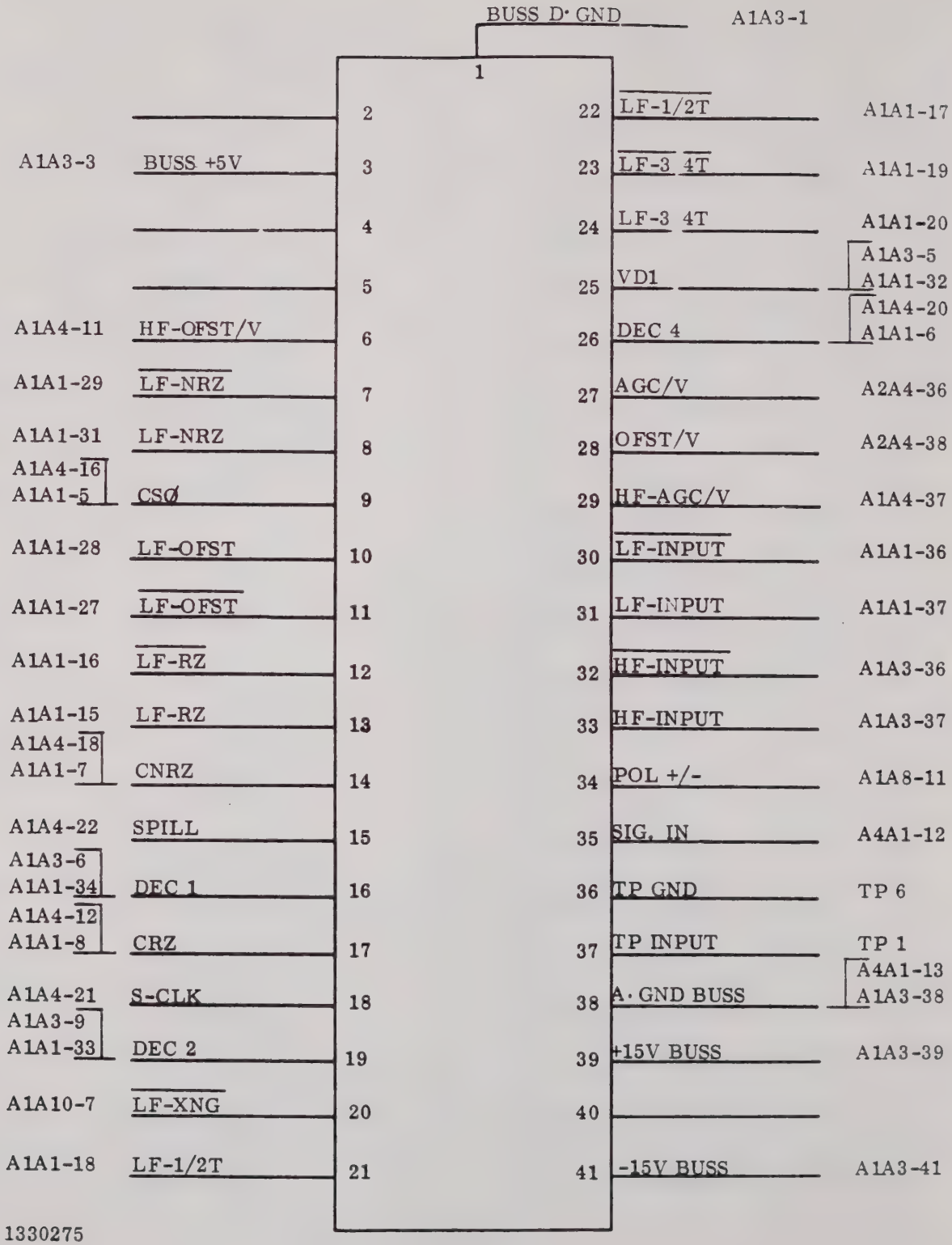
QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		2	2	45	A	100-003-471	RC07GF471J	81349	RES., 470Ω, 1/4W, 5%	R21, R42
		2	2	46	A	100-003-122	RC07GF122J		,1.2K, 1/4W, 5%	R22, R43
		–	2	47	A	100-003-221	RC07GF221J		,220Ω, 1/4W, 5%	R23, R26
		1	1	48	A	100-003-432	RC07GF432J		,4.3K, 1/4W, 5%	R24
		2	2	49	A	100-003-7R5	RC07GF7R5J		,7.5Ω, 1/4W, 5%	R27, R28
		4	4	50	A	100-003-102	RC07GF102J		,1K, 1/4W, 5%	R29, R34, R36, R44
		2	2	51	A	100-005-240	RC20GF240J		,24Ω, 1/2W, 5%	R35, R41
		1	1	52	A	100-003-392	RC07GF392J	81349	,3.9K, 1/4W, 5%	R37
		1	1	53	A	101-115-102	77P	73138	, VAR., 1K	R32
		1	–	54	A	100-003-151	RC07GF151J	81349	,150Ω, 1/4W, 5%	R26
		–	1	55	A	100-003-470	RC07GF470J	81349	RES., 47Ω, 1/4W, 5%	R16
				56						
		1	1	57	A	139-209-002	CA3046	86684	I.C.	U1
				58						
		1	1	59	A	116-002-003	TXBF-032-025B	98978	HEATSINK, TO-5	
		1	1	60	A	131-021-001	10076	07047	TRANSISTOR PAD, TO-5	
				61						
				62						
		2	2	63	A	121-202-005	8041-1G7	91506	TEST JACK, GREEN	TP1, TP2
		1	1	64	A	121-202-010	8041-1G6	91506	TEST JACK, BLACK	GND
				65						
		AR	AR	66	A	120-101-001	SN63BS	81348	SOLDER	QQ-S-571

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
M. GRIES DATE 9-8-72	J. SAMPEDRO DATE 10-2-72	PARTS LIST LDR024	20747	PL460-0980-0 SHEET 4 OF	E

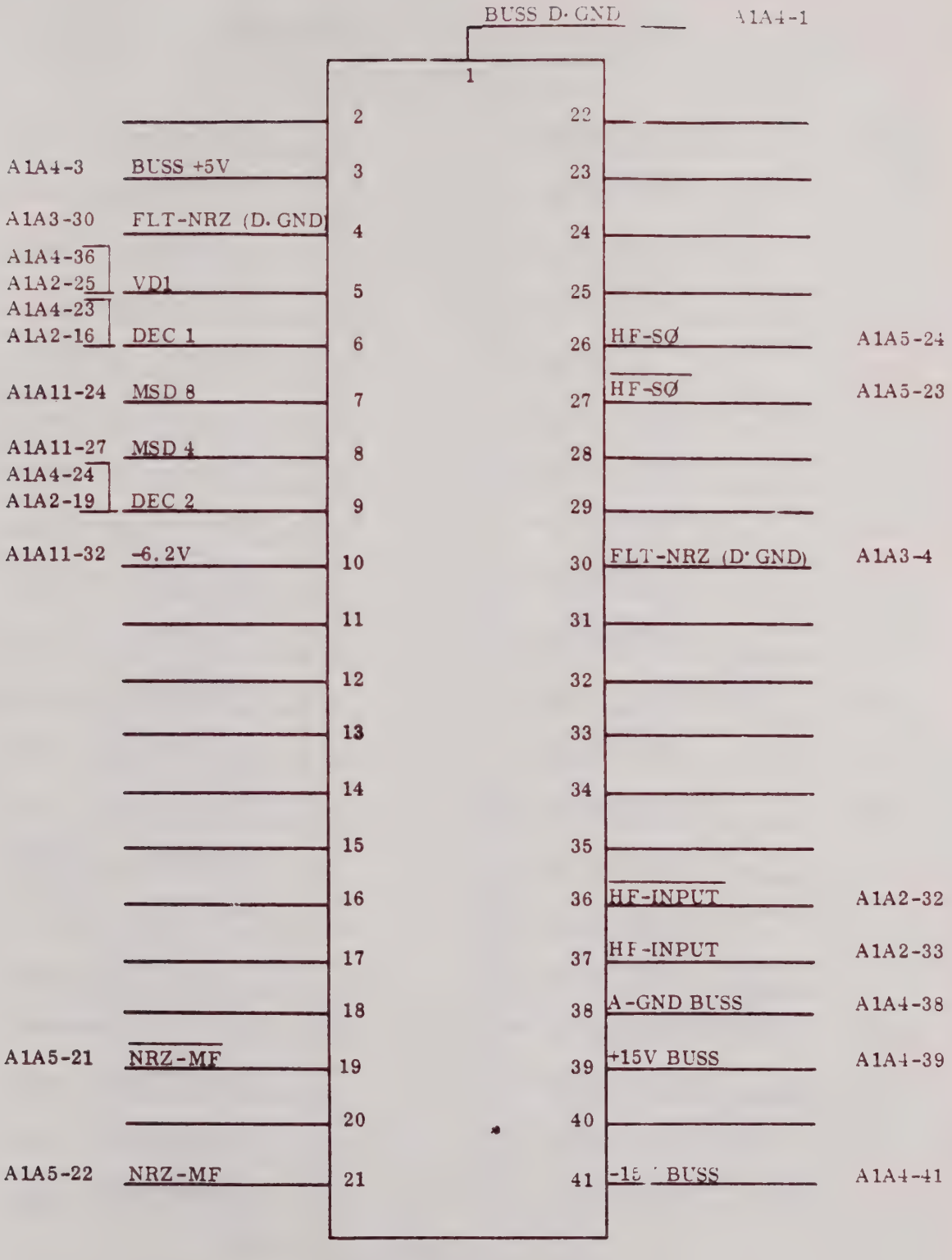
800 431 JA



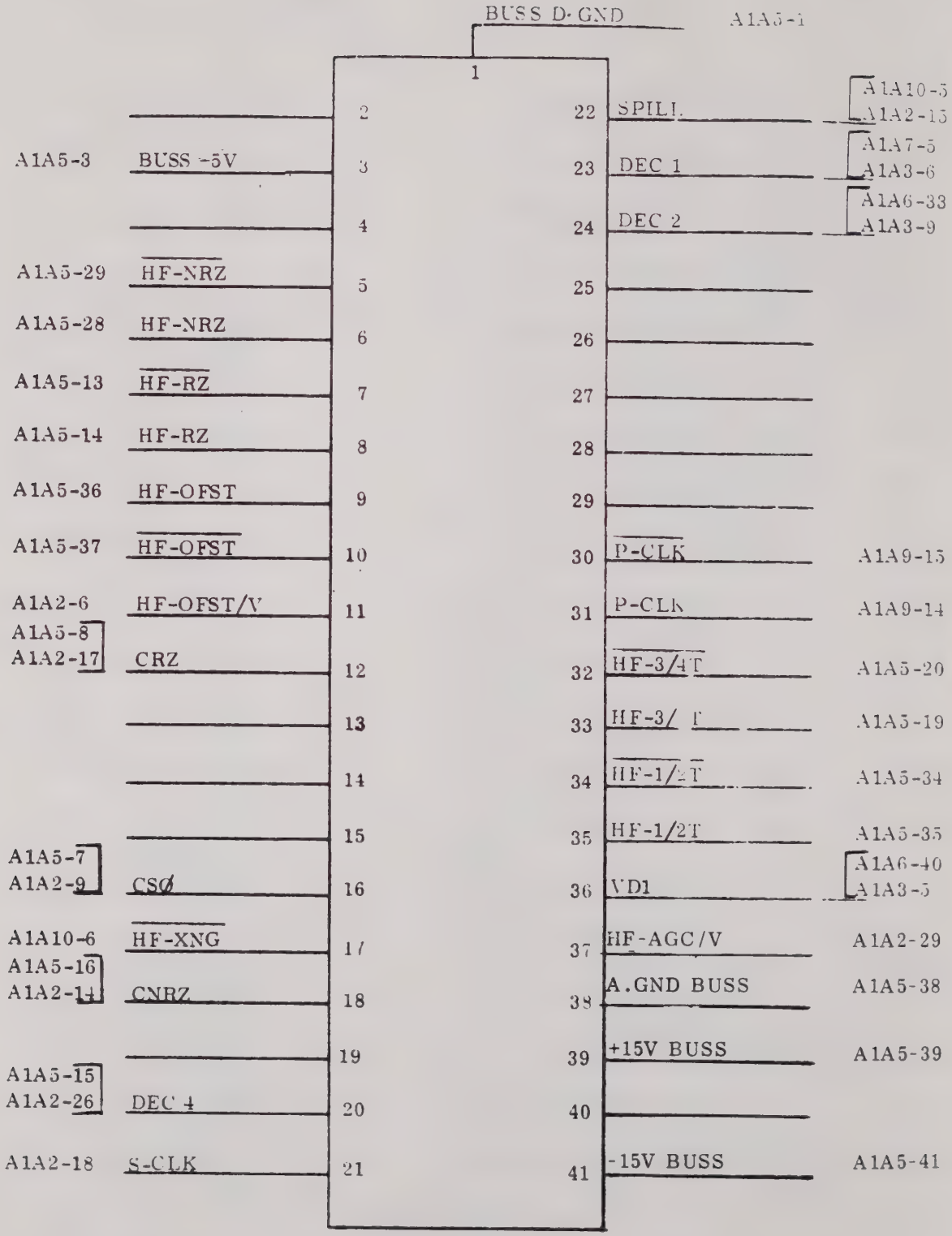
Type VAF027 Low Frequency Matched Filter PC Card
A1A1, Interconnection Wiring Diagram



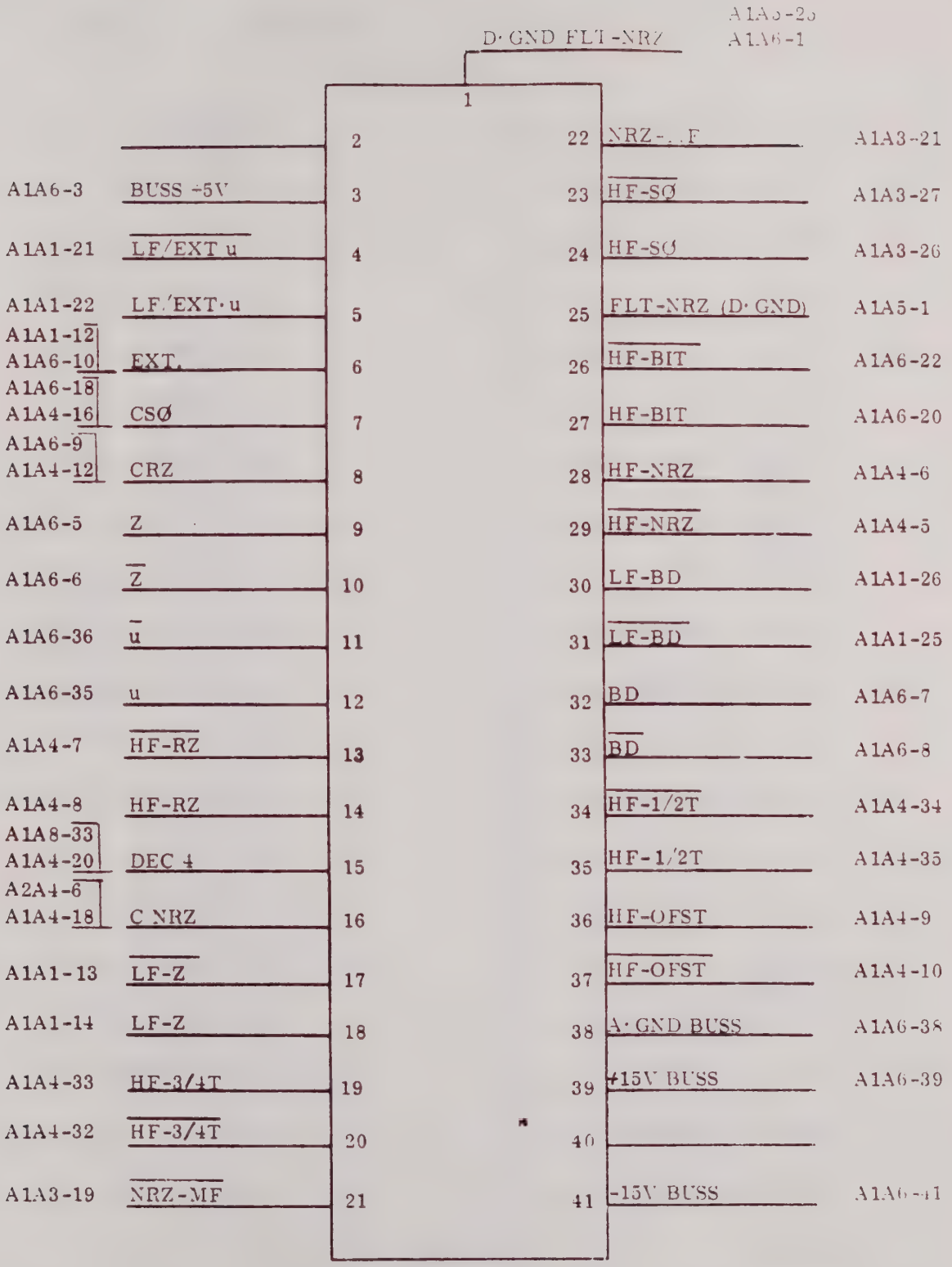
Type SLC029 Signal Level Control PC Card
A1A2, Interconnection Wiring Diagram



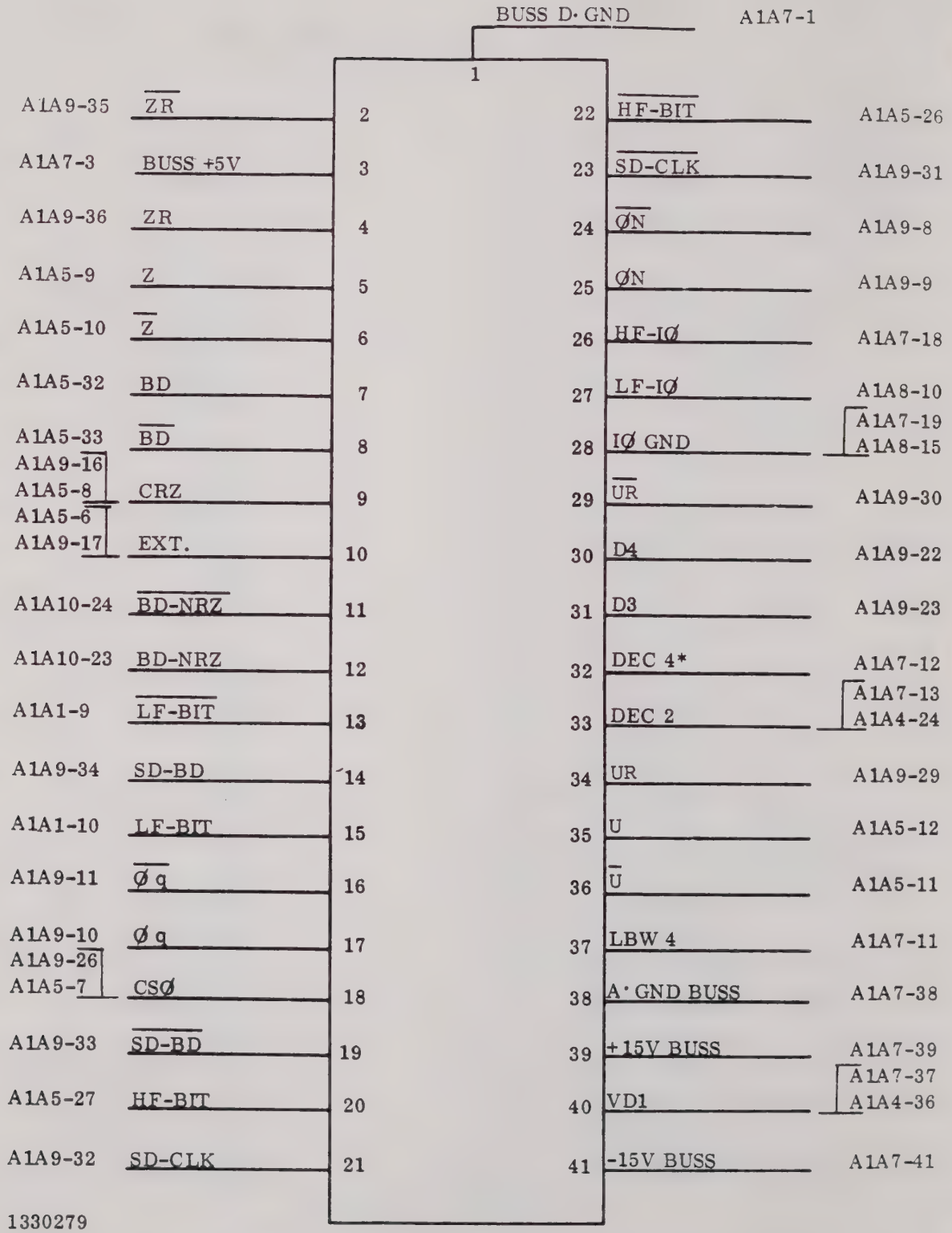
Type VAF026 High Frequency Matched Filter PC Card
A1A3, Interconnection Wiring Diagram



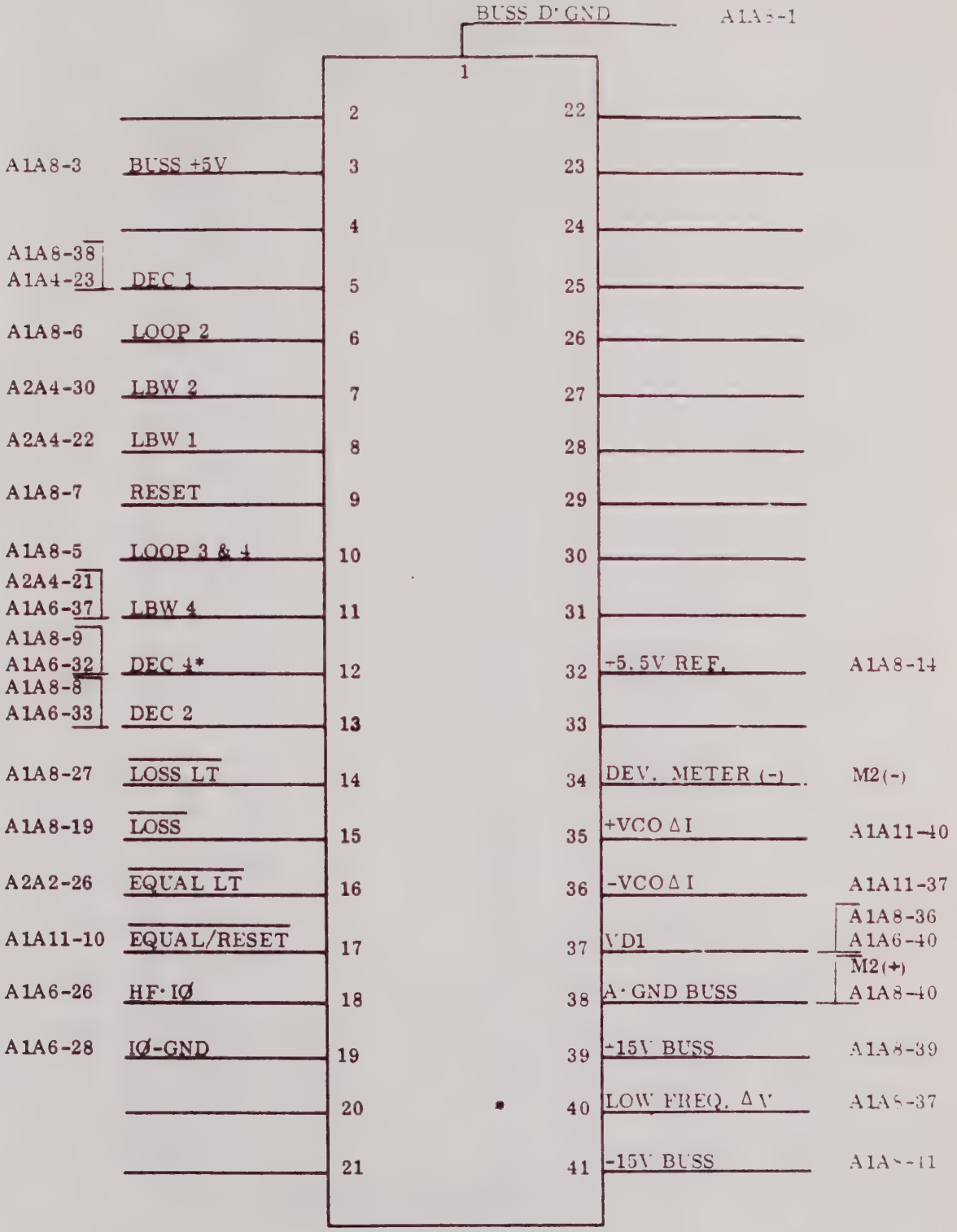
Type SLC030 Signal Level Control PC Card
A1A4, Interconnection Wiring Diagram



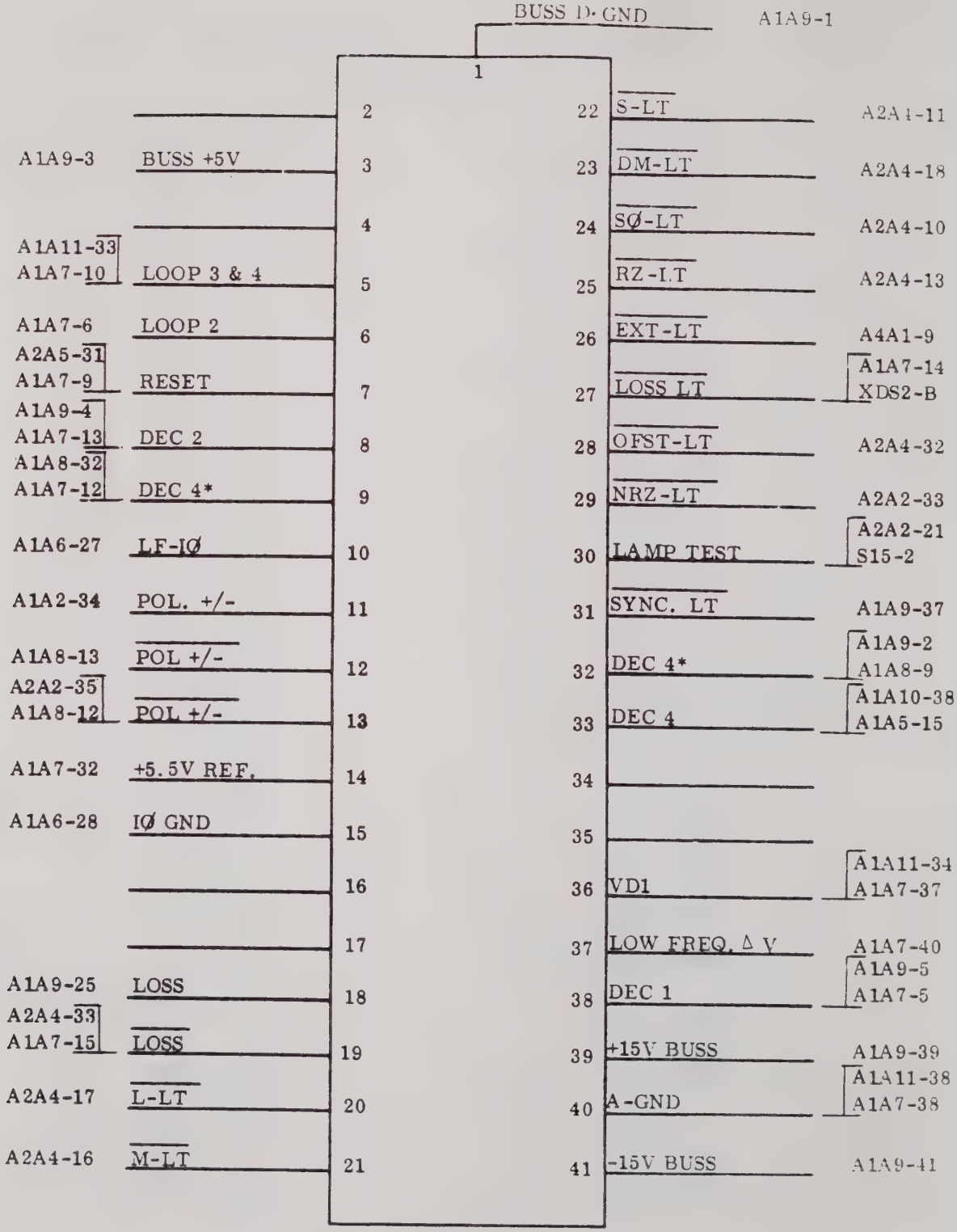
Type THD001 High Frequency Threshold Detector PC Card
A1A5, Interconnection Diagram



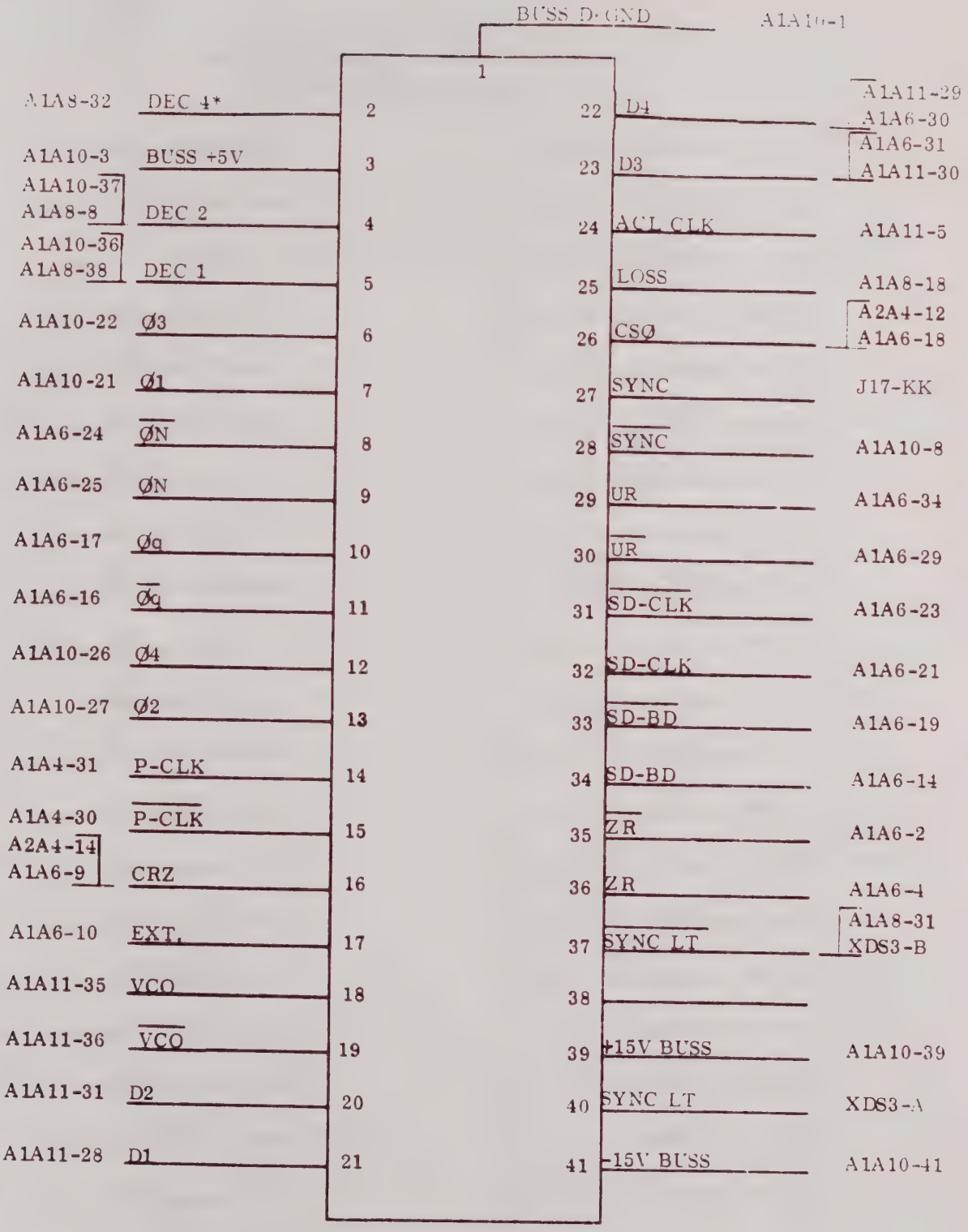
Type PDT020 Phase Detector PC Card
A1A6, Interconnection Wiring Diagram



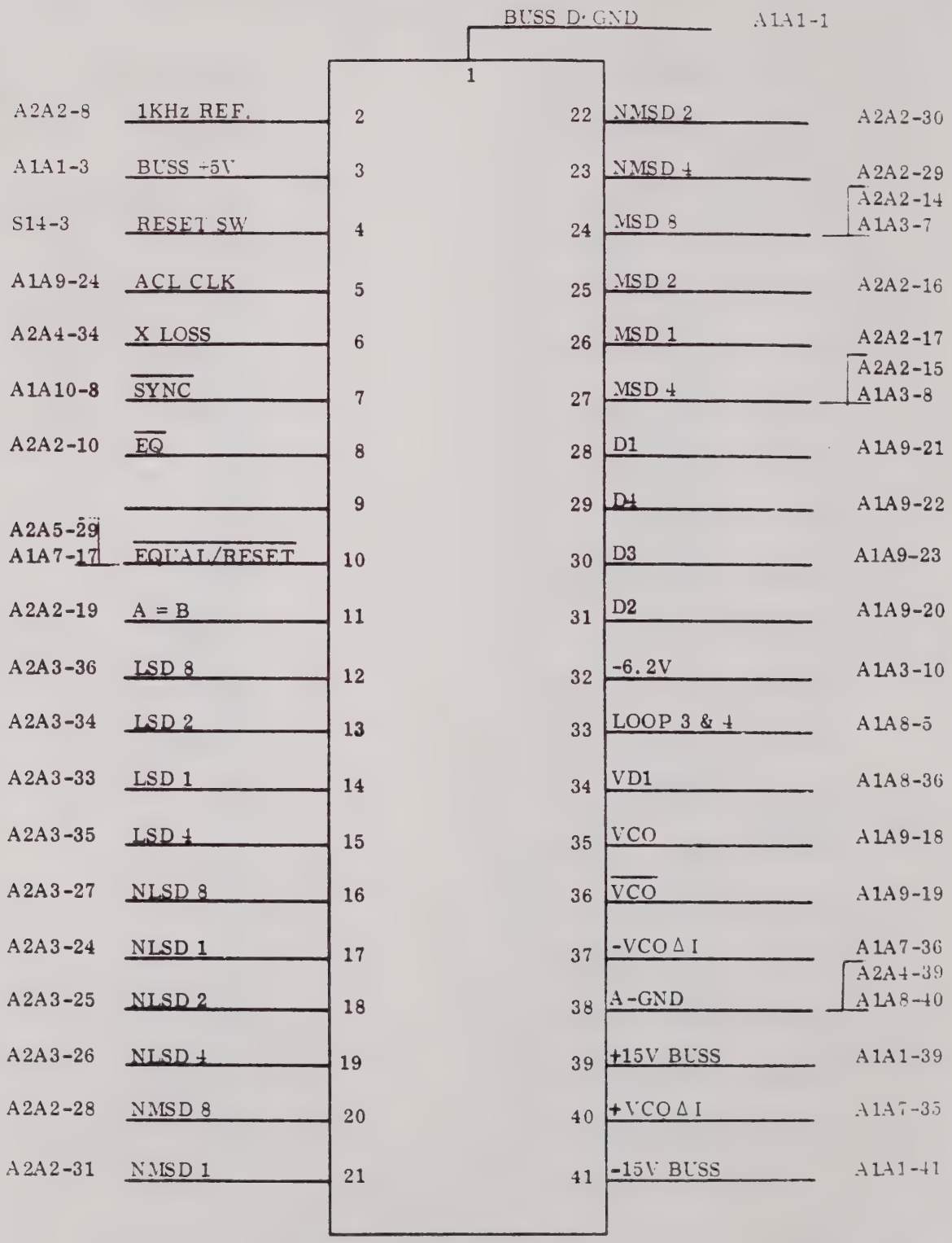
Type HLF001 High Frequency Tracking Loop Filter
PC Card A1A7, Interconnection Wiring Diagram



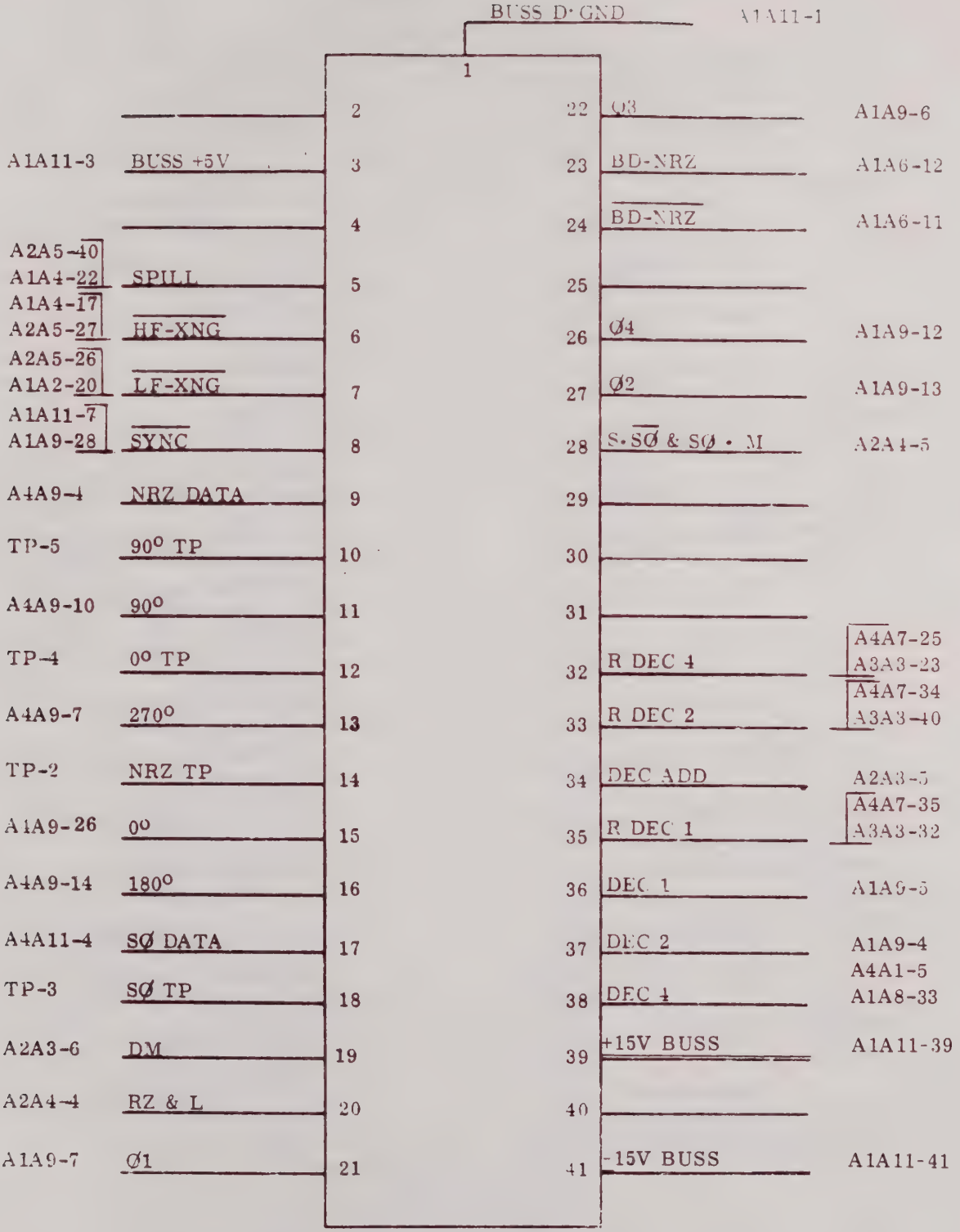
Type PLL102 Low Frequency Phase Lock Loop PC Card
A1A8, Interconnection Wiring Diagram



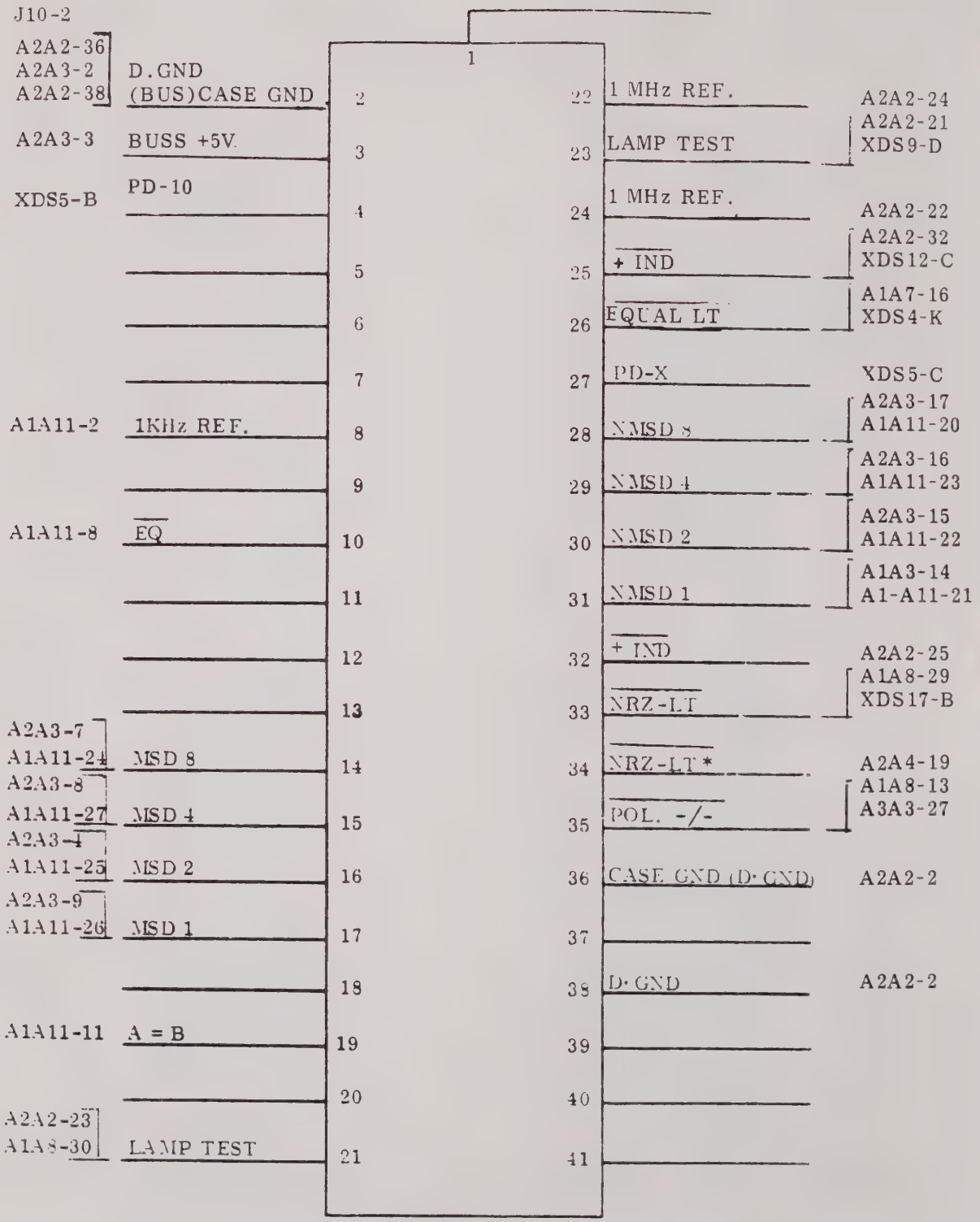
Type CSD002 Countdown and Sync Detector PC Card A1A9, Interconnection Wiring Diagram



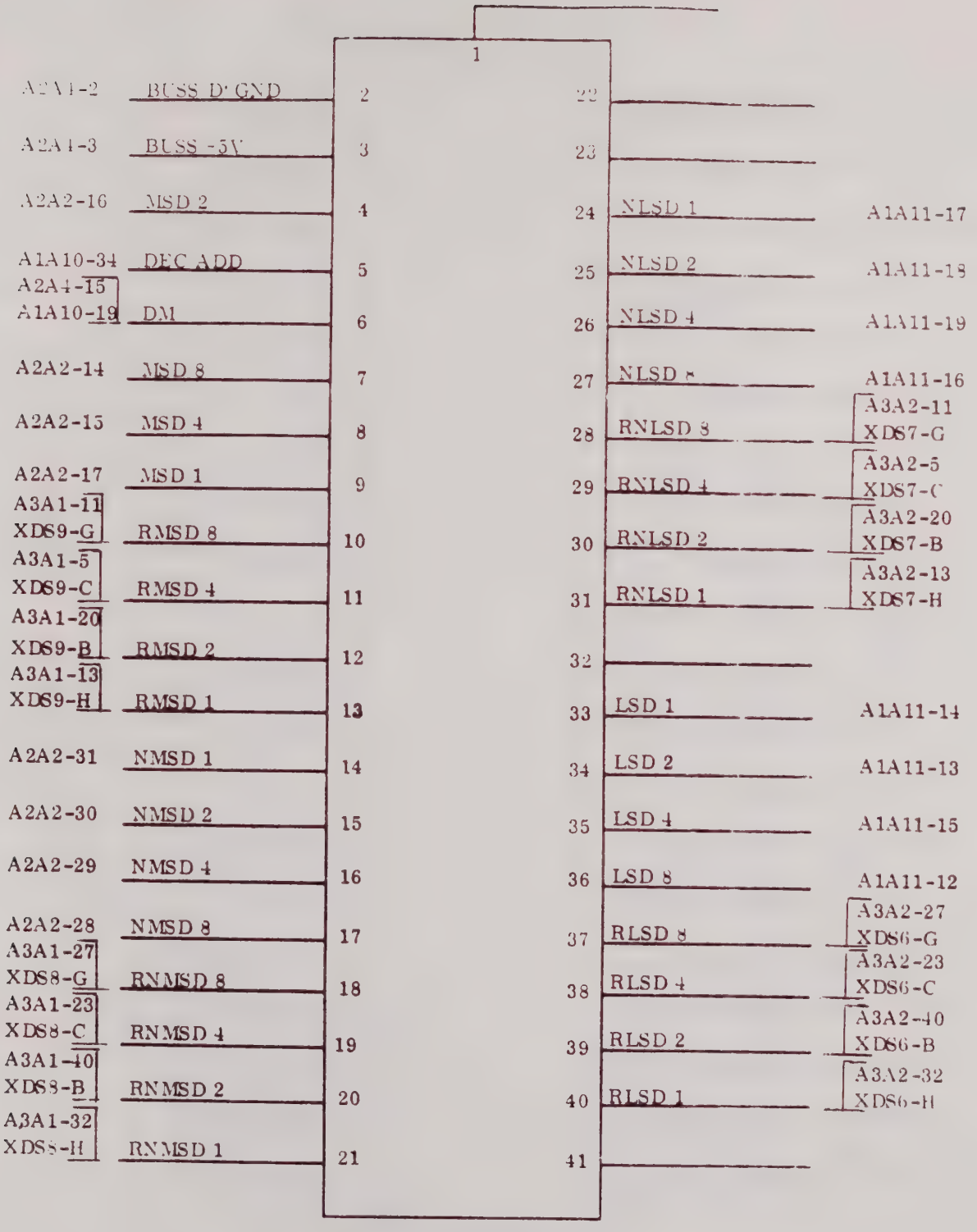
Type ACL009 Automatic Calibration PC Card
A1A11, Interconnection Wiring Diagram



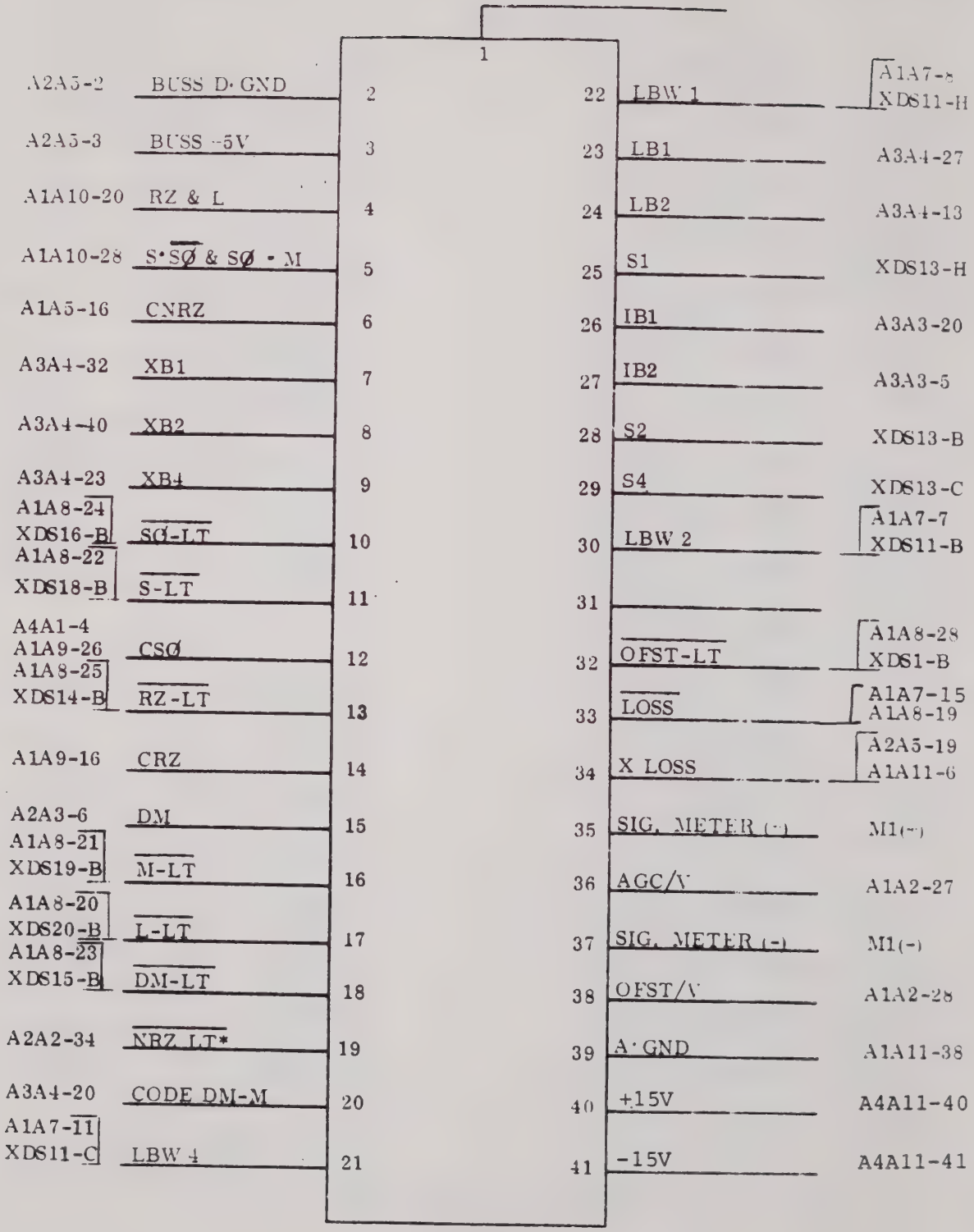
Type CCR036 Code Converter PC Card
A1A10, Interconnection Wiring Diagram



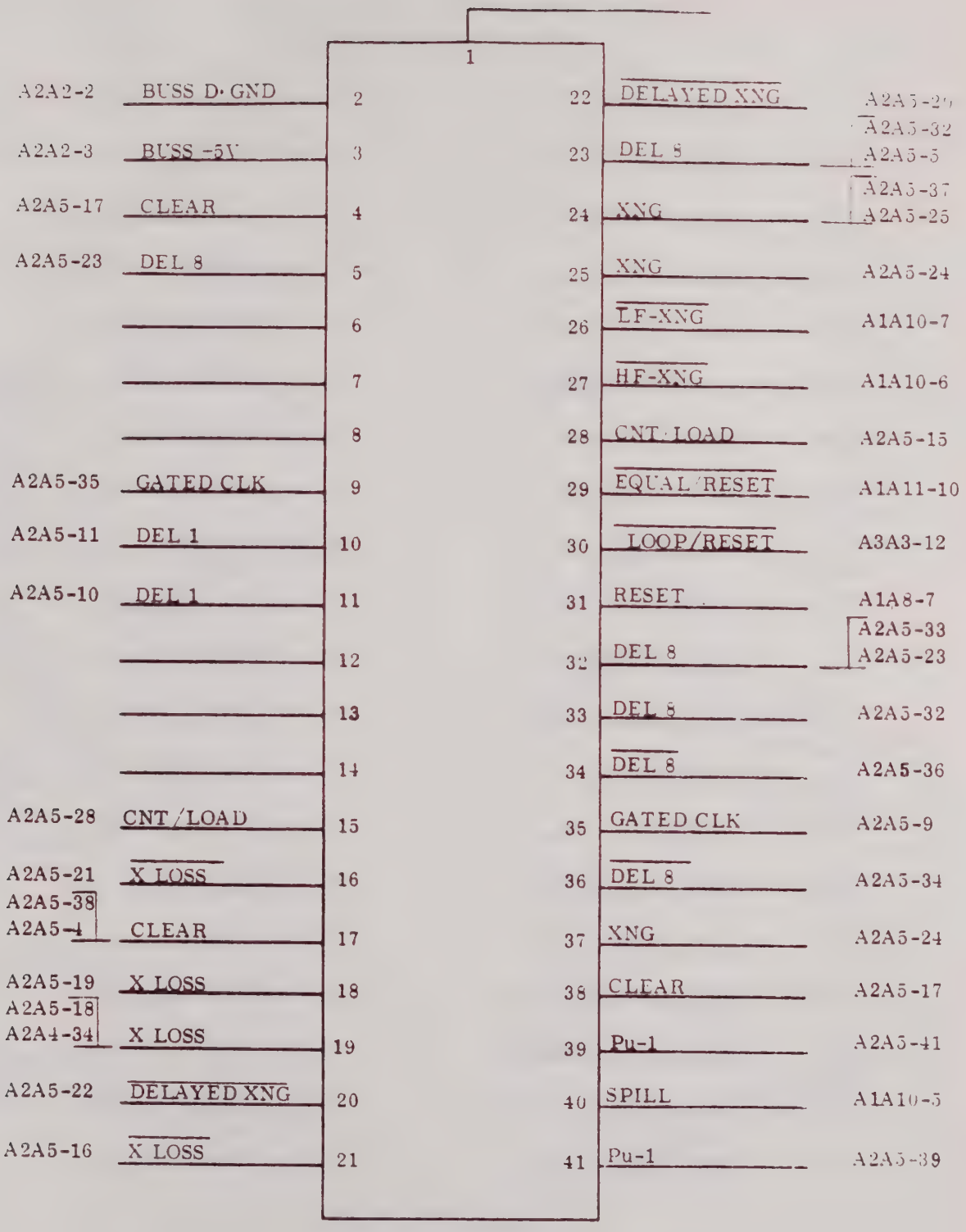
Type XTL028 Crystal Oscillator PC Card
A2A2, Interconnection Wiring Diagram



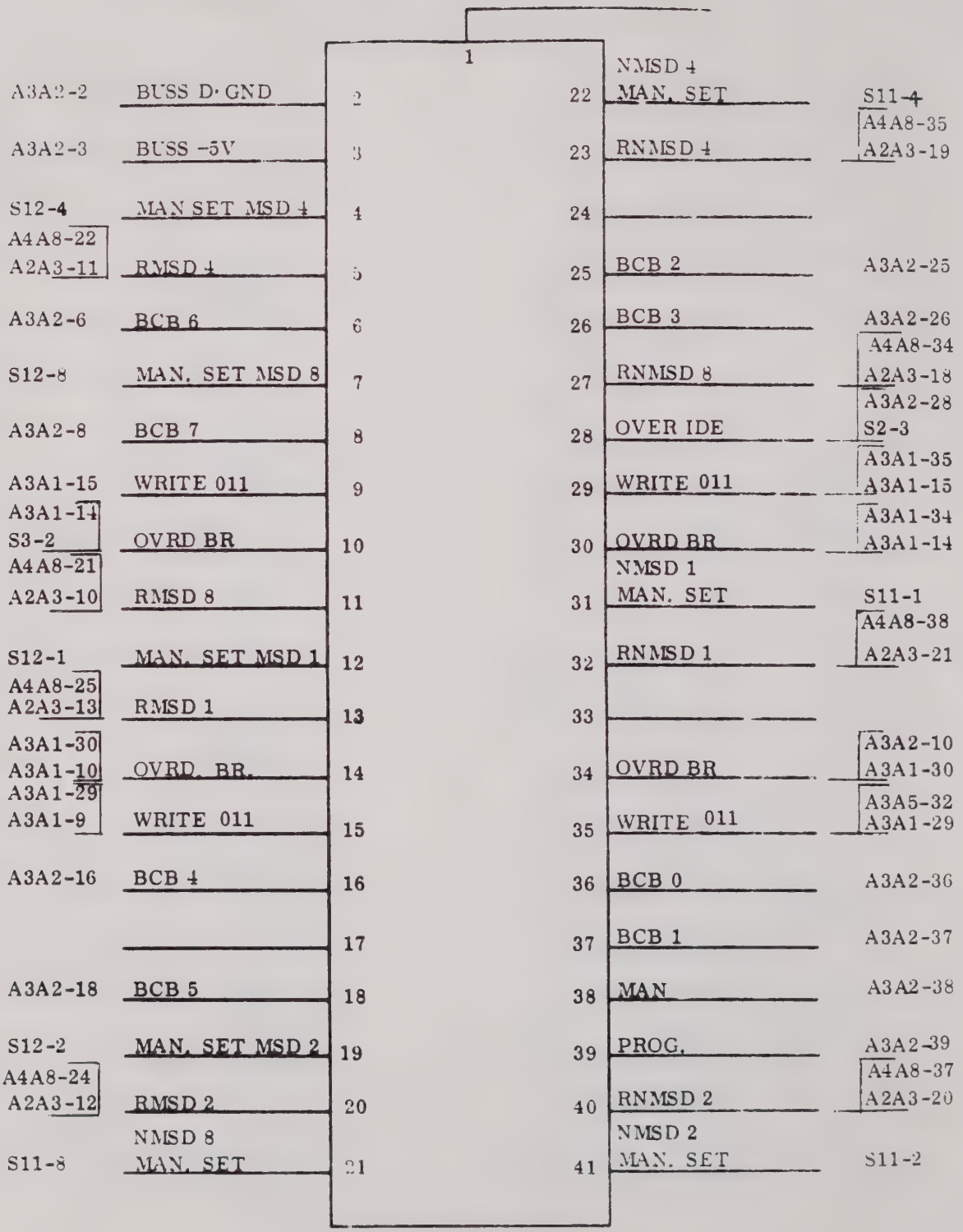
Type BCD001 Binary-Coded-Decimal Multiplier
PC Card A2A3, Interconnection Wiring Diagram



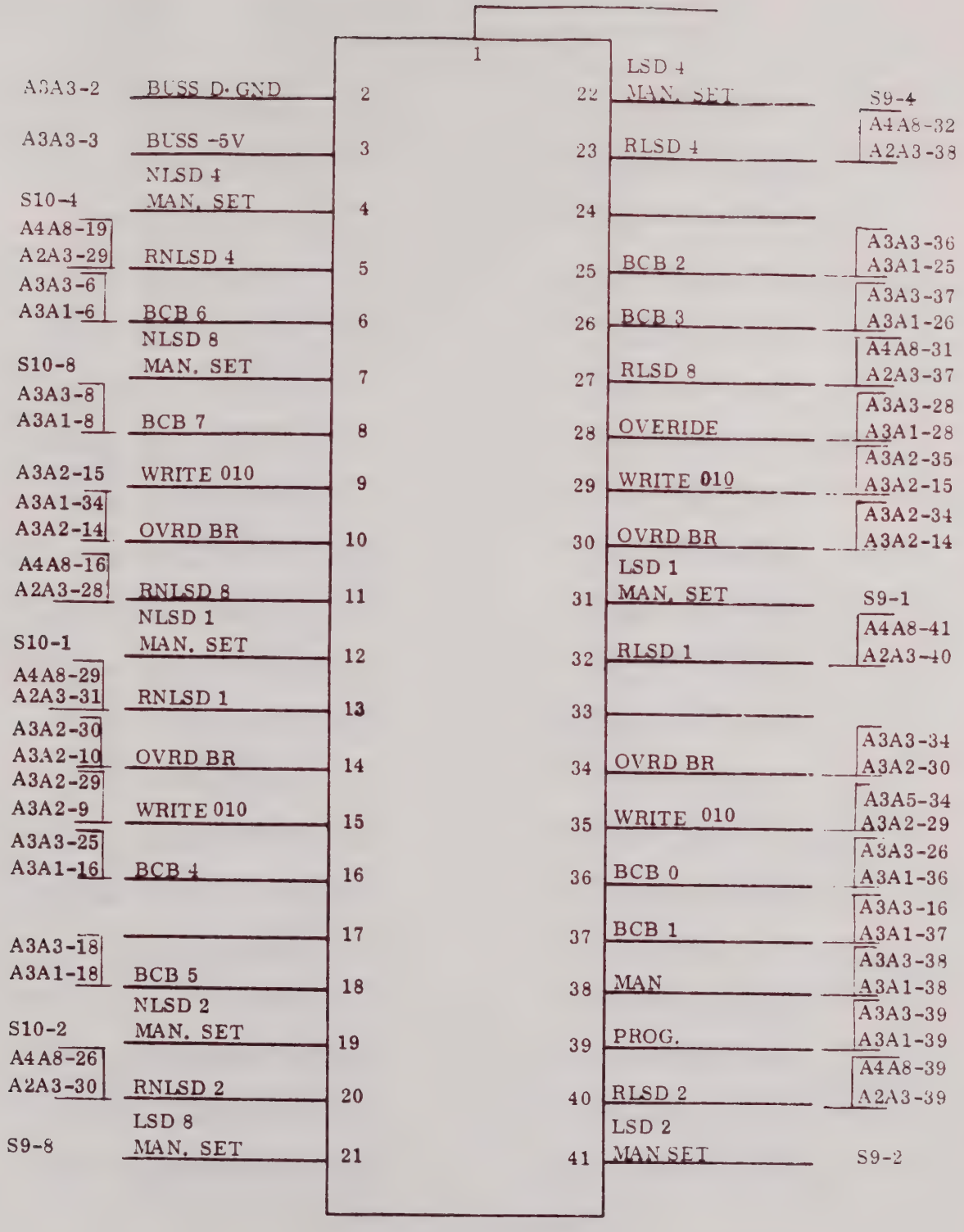
Type PDC001 Program Decode PC Card
A2A4, Interconnection Wiring Diagram



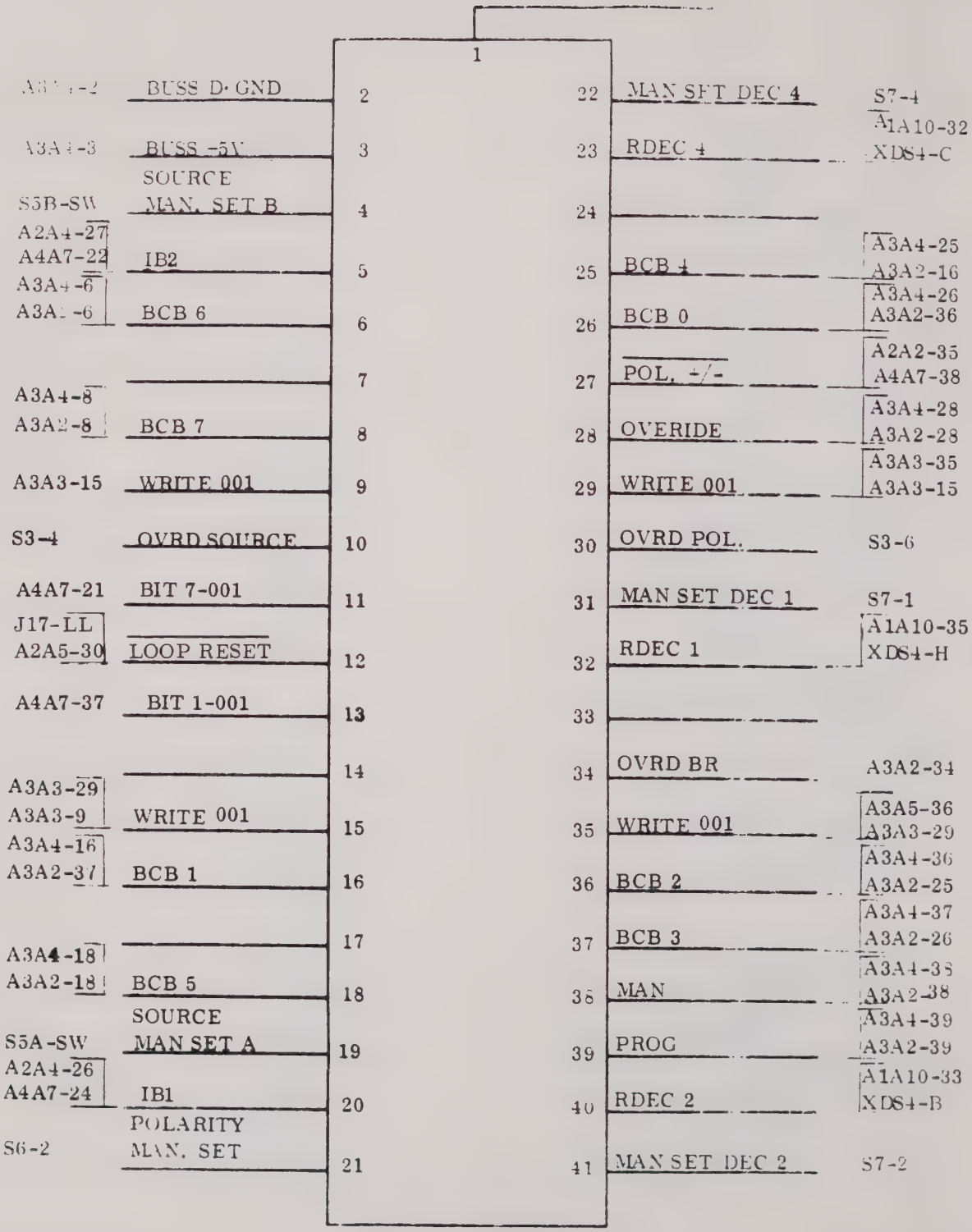
Type LDY001 Transition Loss Delay Generator
PC Card A2A5, Interconnection Wiring Diagram



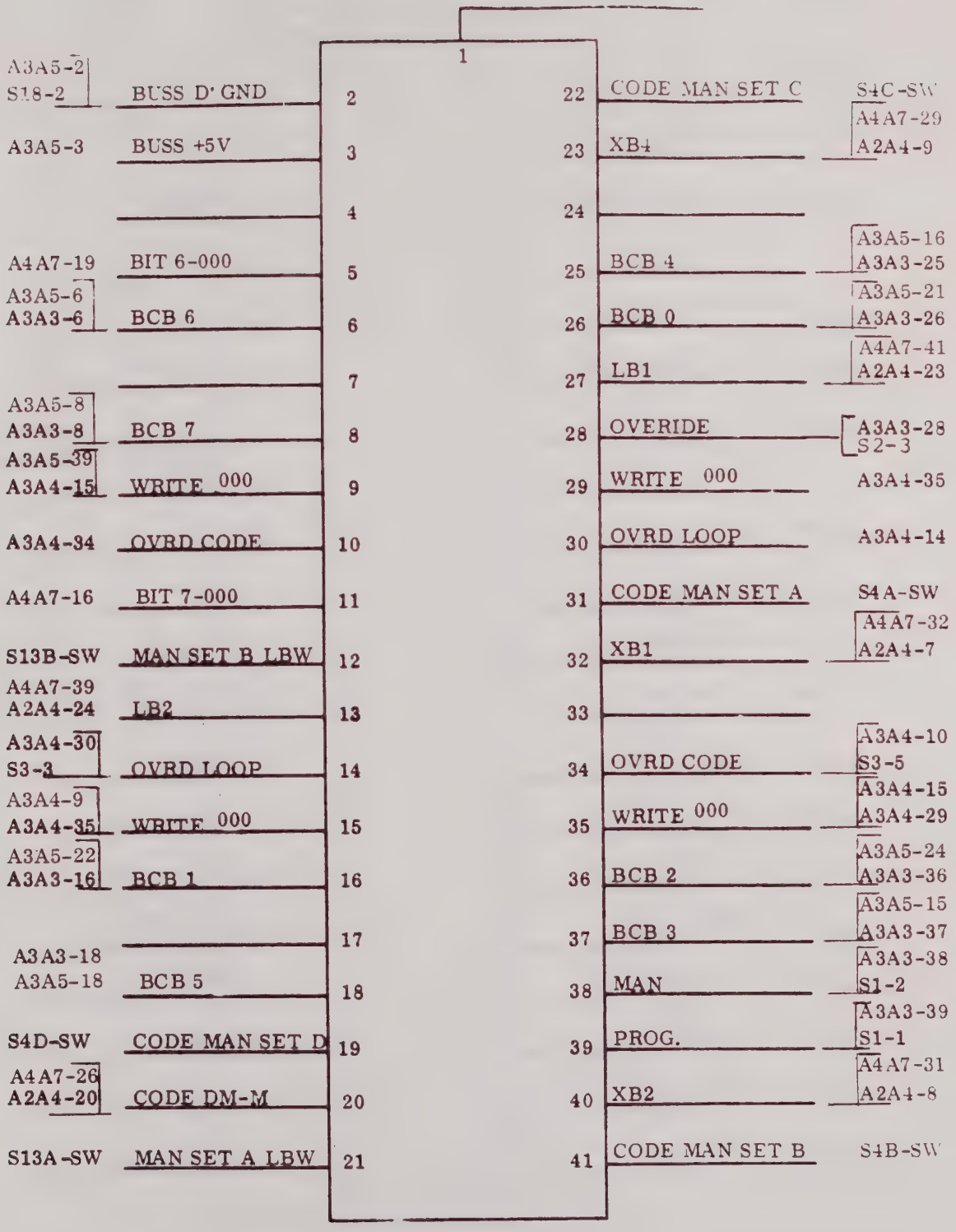
Type PSR021 Program Storage Register PC
Card A3A1, Interconnection Wiring Diagram



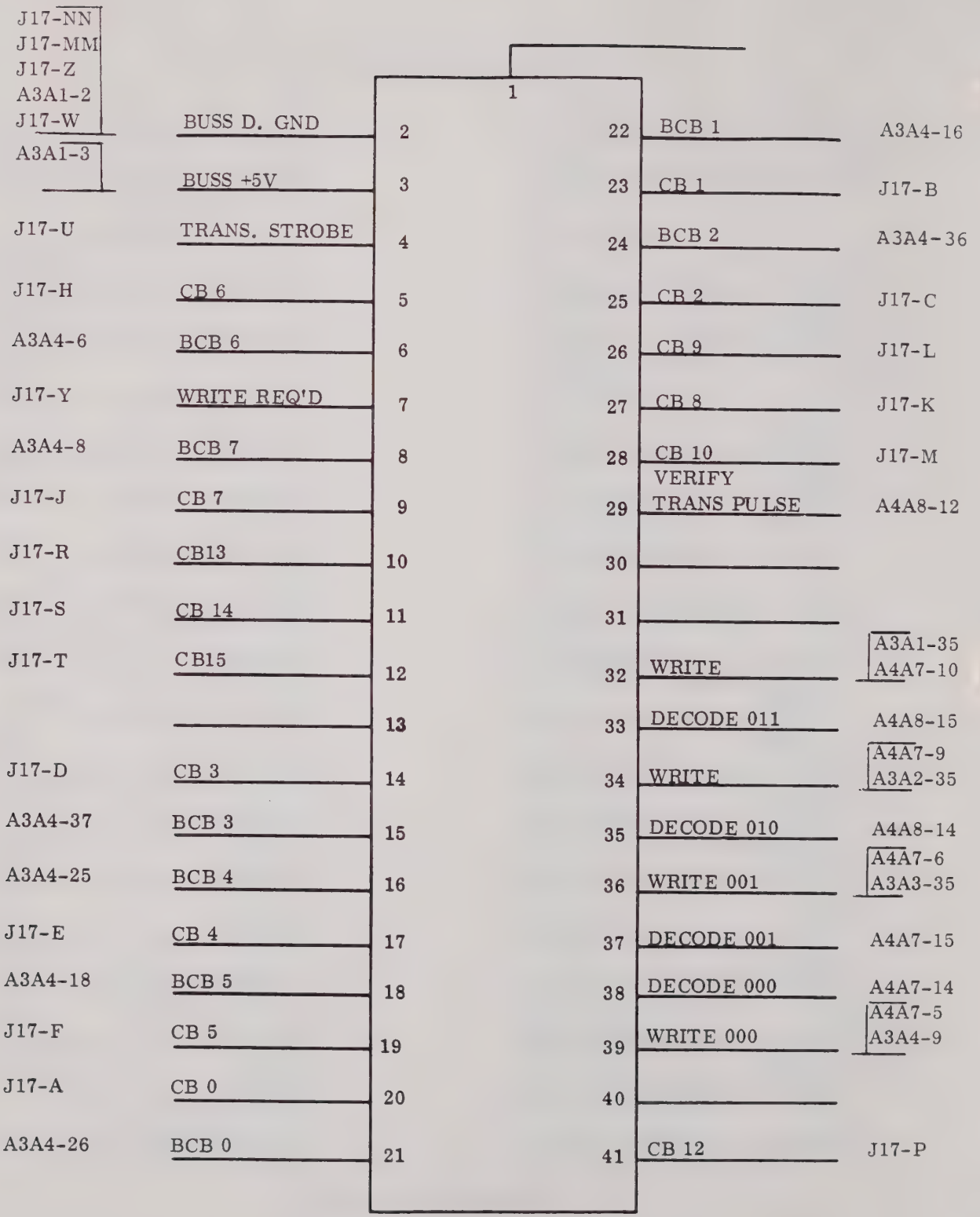
Type PSR021 Program Storage Register PC
Card A3A2, Interconnection Wiring Diagram



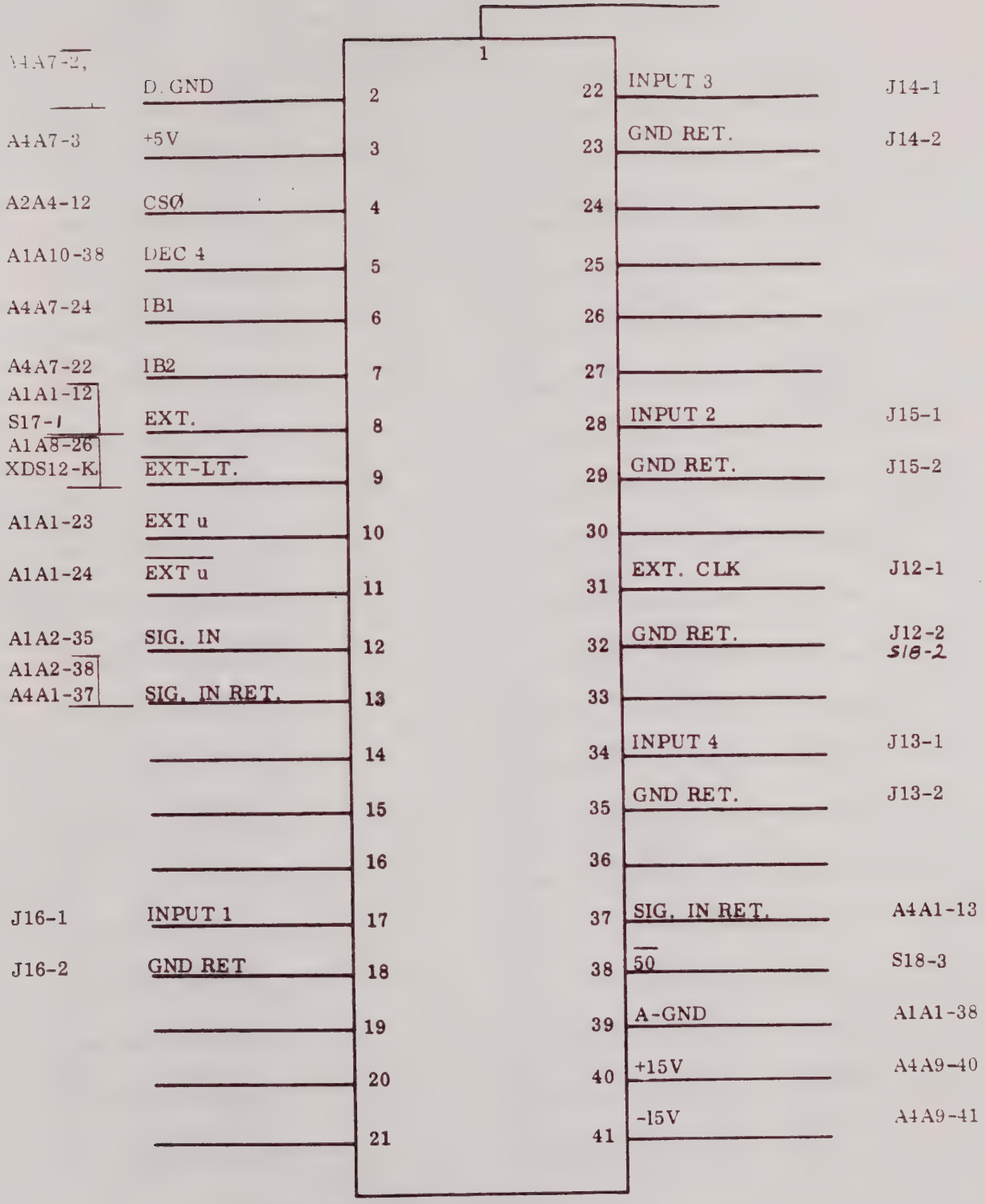
Type PSR021 Program Storage Register PC
Card A3A3, Interconnection Wiring Diagram



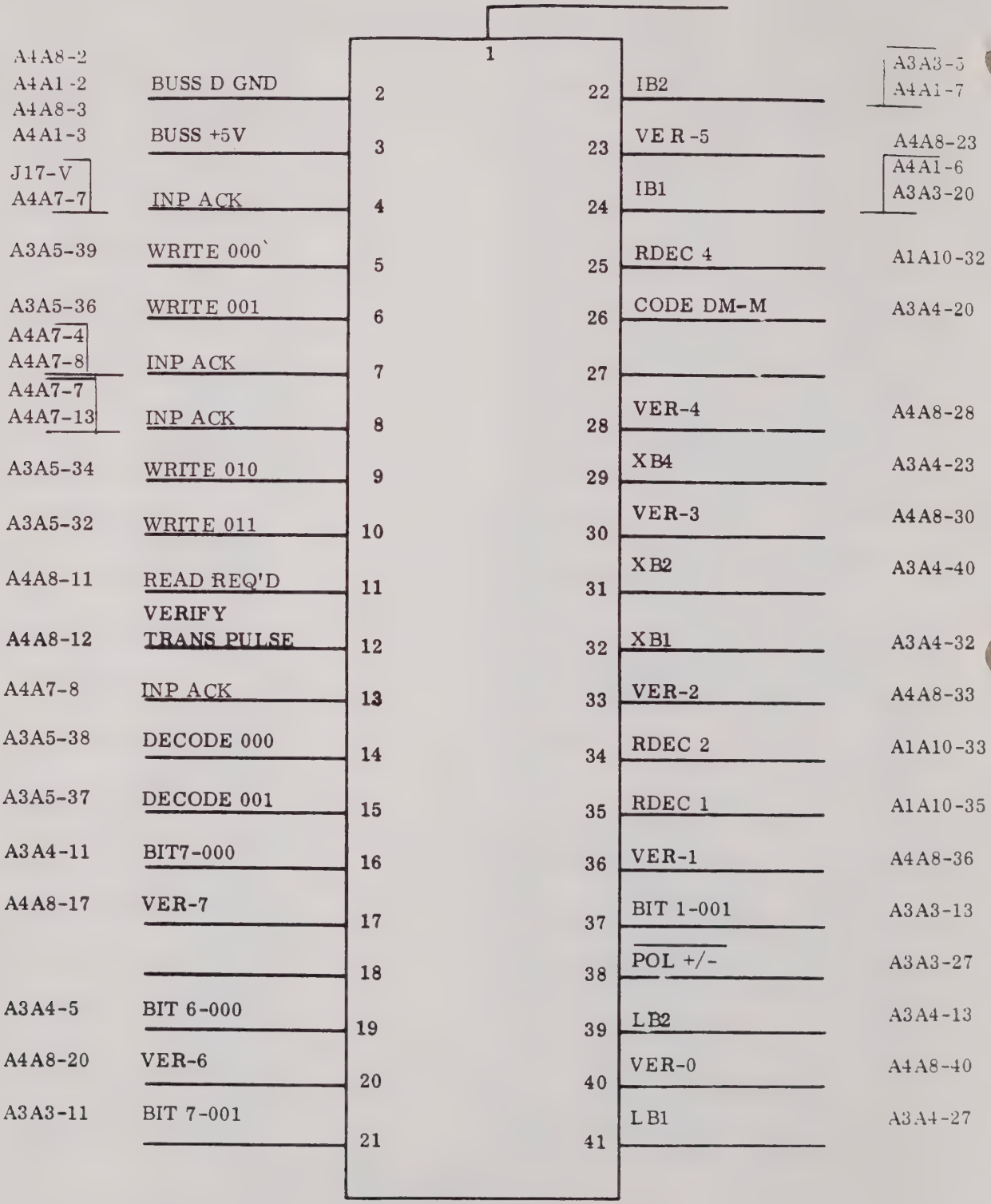
Type PSR021 Program Storage Register PC
Card A3A4, Interconnection Wiring Diagram



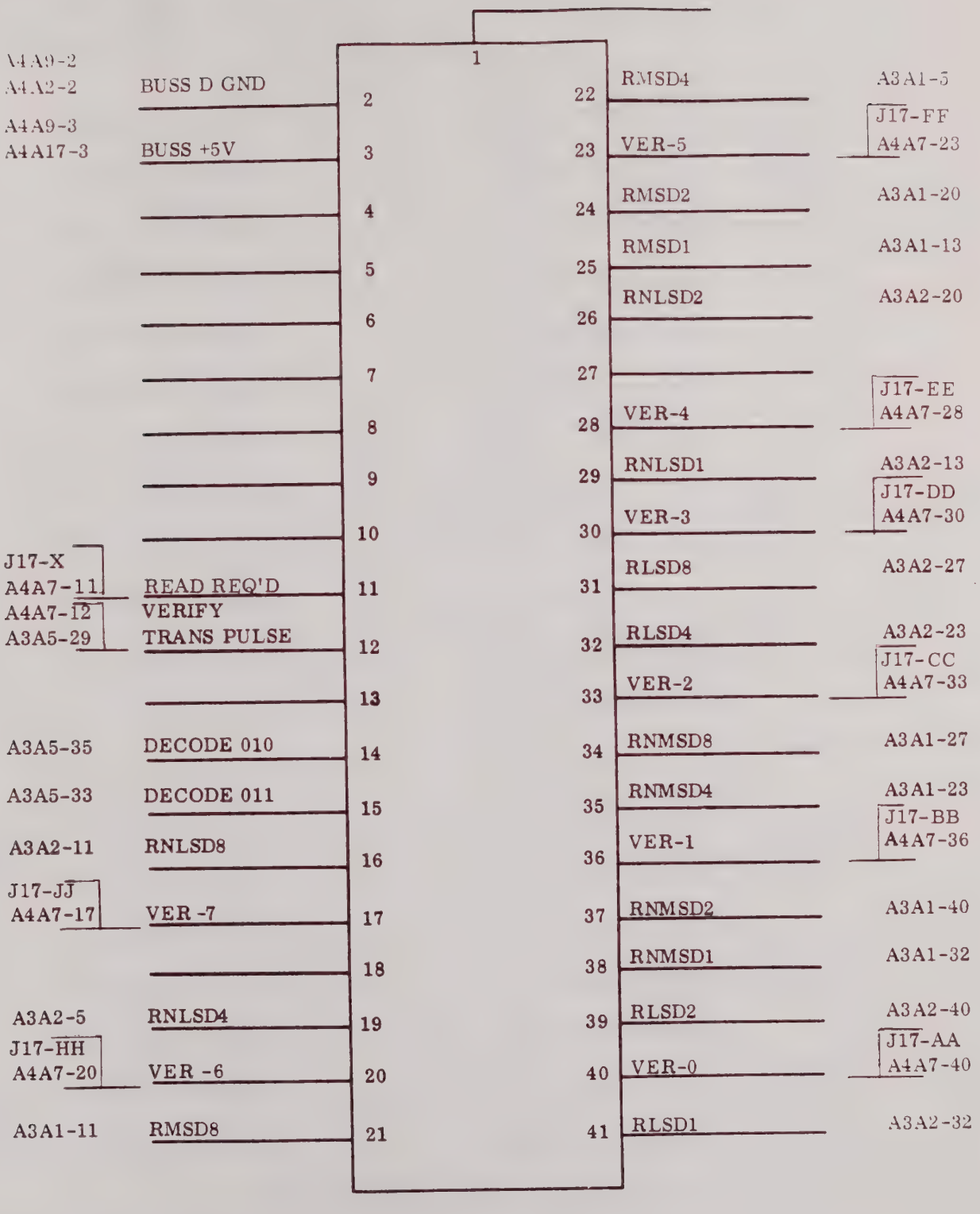
Type DDR022 Decoder Driver PC Card
A3A5, Interconnection Wiring Diagram



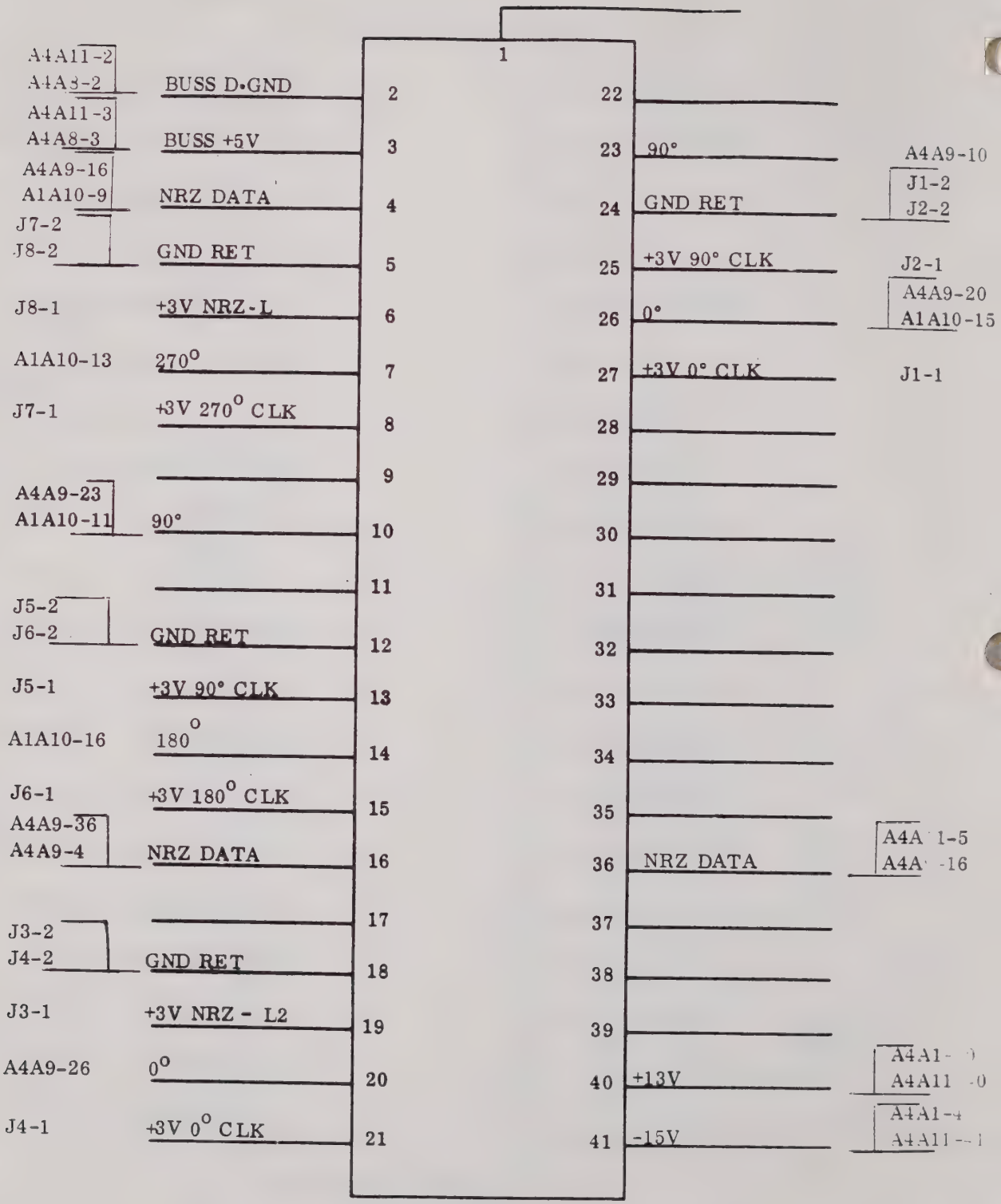
Type INP050 Input Select PC Card A4A1,
Interconnection Wiring Diagram



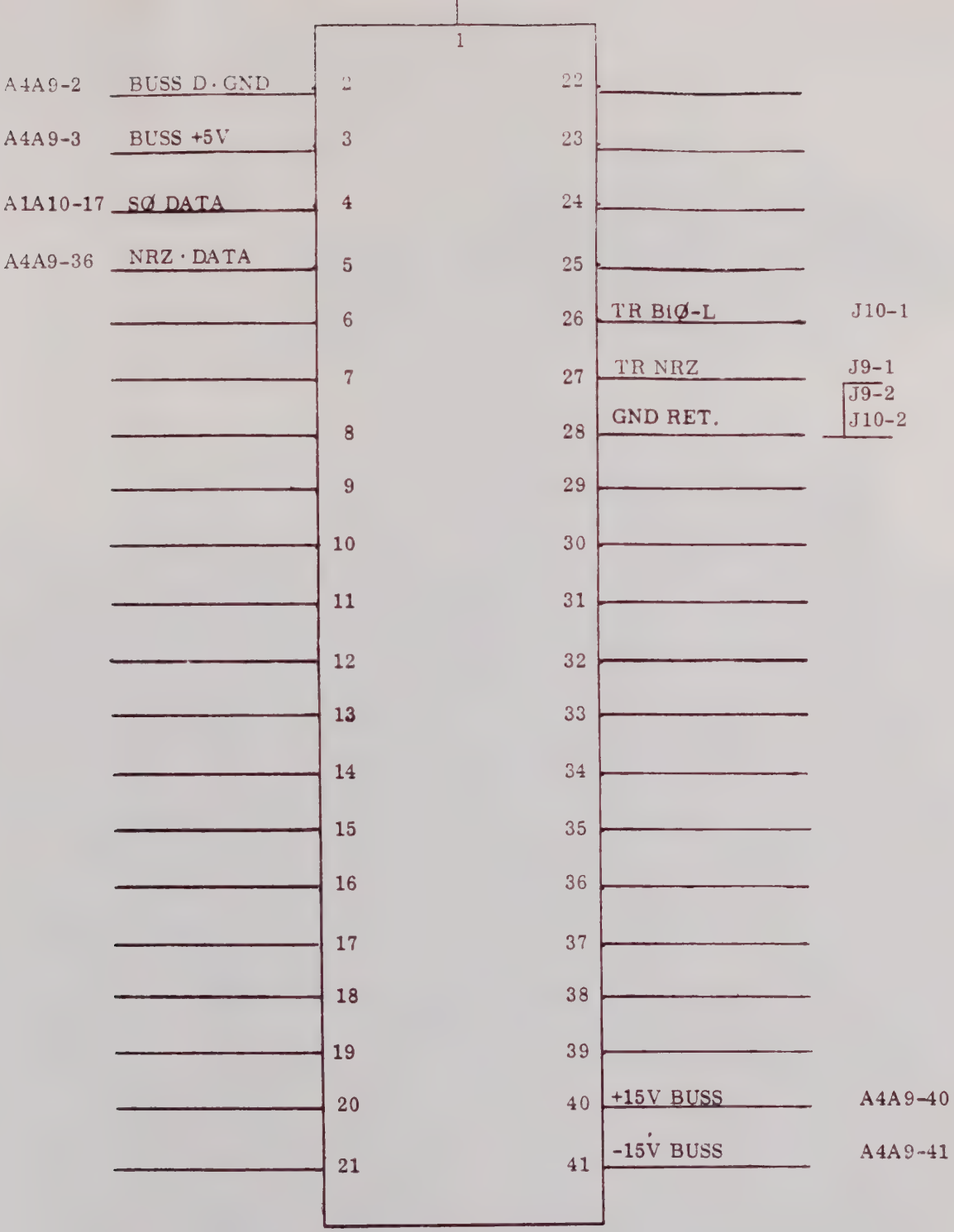
Type DDR030 Program Verify PC Card
A4A7, Interconnection Wiring Diagram



Type DDR030 Program Verify PC Card
A4A8 Interconnection Wiring Diagram



Type LDR023 Line Driver PC Card A4A9,
Interconnection Wiring Diagram



Type LDR024 Line Driver PC Card A4A11,
Interconnection Wiring Diagram

APPENDIX A

Power Supply
acdc electronics, inc. P/N [illegible]502-1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

SEE SHEET 2

MONITOR PART NUMBER	A C D C PART NUMBER (FSCM 08742)		DESCRIPTION
136-079-001	ETV401-1		*
136-079-002	ET601-1		5V@12A & ±12V@3A
136-079-003	ET602-1		5V@12A & ±15V@3A
136-079-004	———		———
136-079-005	———		———
136-079-006	———		———
136-079-007	USE 136-134-002		———
136-079-008	USE 136-134-004		———
136-079-009	EC5N9.5-1		SINGLE 5V@9.5A
136-079-010	EC5N3B		SINGLE 5V@3.0A

* THE COMBINATION 12/15V POWER SUPPLY IS SET FOR 12V AT THE FACTORY (INCLUDING OVP) THE 15V OPTION MUST BE ADJUSTED @ AMS (INCLUDING OVP). THE POWER SUPPLY WILL BE TESTED AT RECEIVING INSPECTION IN THE 12V MODE.

THIS SPECIFICATION IS NOT COMPLETE WITHOUT SHEETS 2 THRU 12.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ± /, DECIMALS ±, ANGLES ±

MATERIAL

FINISH

CONTRACT NO 2668

		DATE
DRAWN	E. SUNDBERG	4-1-76
CHECKED	E. STUCKER	4-6-76
APPROVED	J. WALTZ	4-6-76
APPROVED, QA	J. SLAVICS	4-6-76
APPROVED, ENG	T. LOCASALE	4-5-76

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNSYLVANIA

SPECIFICATION,
POWER SUPPLY,
SINGLE, DUAL & TRIPLE OUTPUT

SIZE	CODE IDENT NO.		REV.
A	20747	136-079-□	H

SCALE ——— SHEET 1 OF 12

800-0529

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPV'D
B	ADDED -004 & -005		2-24-77	EJS
C	ADDED -006		10-25-77	R. WASSERMAN
D	ADDED -007		1-31-78	J. RONEY
E	ADDED -003		2-23-79	J. MATHER
F	ADDED -009		1-30-80	[illegible]
G	ADDED -010		3-25-80	[illegible]
H	REVISED PER ECO 08534 R.P.K.		10-27-83	[illegible]

MONITOR SYSTEMS INC.

800-0637

CODE IDENT NO.	DWG NO.	REV
20747	130-079-□	H
	SHEET 2 OF	

Universal Series

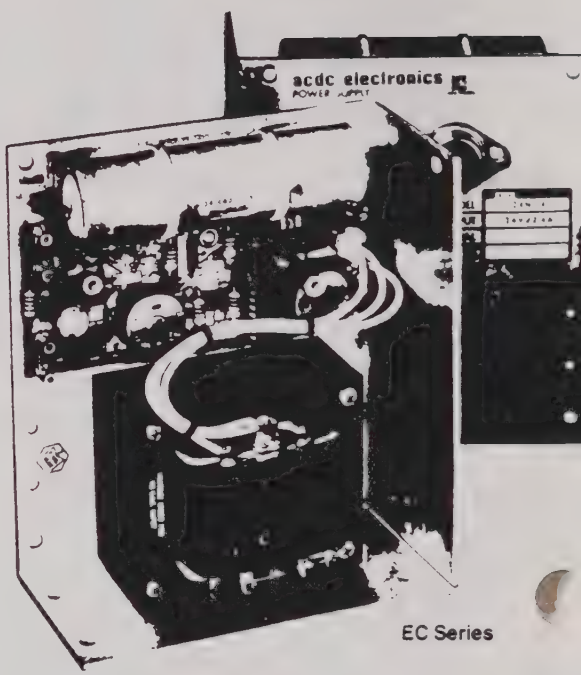
ECV/ETV MODELS

With the price/performance, quality and reliability you expect from ACDC Electronics, the Universal Open Frame Series offers a cost effective solution to your general power supply needs. The first truly universal open frame linear power supplies on the market, all ECV/ETV models operate at 47-440 Hz with input voltages of 100 VAC, 117VAC, 220 VAC, 230 VAC, or 240 VAC. The five-terminal input is compatible with CORCOM VSF Series line filters. The Universal Open Frames meet your system voltage requirements for Japan, Europe, and the UK, including stringent VDE 0804 high voltage and leakage requirements. Earth ground terminal and Faraday shield are included on most models.

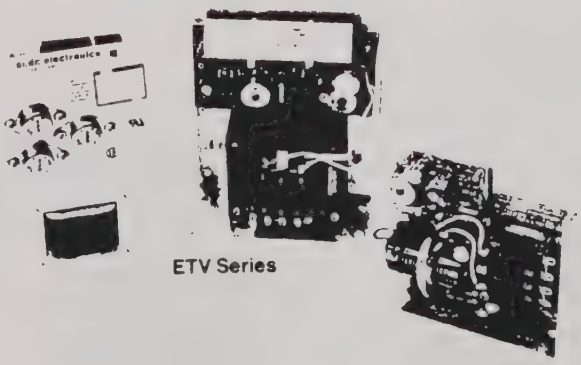
Designed to meet industry standard outline and mounting dimensions, the ECV single and multi-output models are completely interchangeable with competitive models, but offer many features not available from most other vendors. These Universal Power Supplies provide improved performance — at lower cost

All models are available for immediate delivery from a world-wide network of franchised electronic distributors and representatives. Many value-added services are also provided; this includes local warranty service on equipment installed or purchased in Europe.

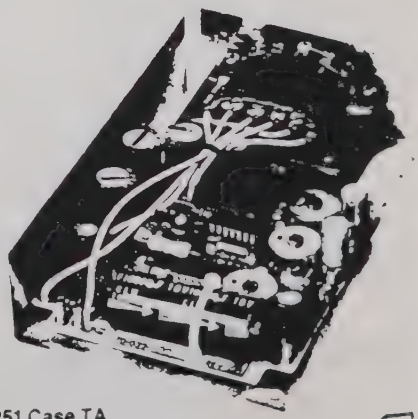
The next time you have a power supply requirement, contact your local distributor. Consult your local sales office for OEM price quotations or for requirements not shown below



EC Series



ETV Series



ETV 251 Case TA
Triple Output

136-079-□
SHEET 3

SINGLE OUTPUT EC/ECV SERIES MODEL SELECTION CHART—

MODEL NUMBER ADD-1 FOR OVP[1]	CASE SIZE	NOMINAL OUTPUT VOLTAGE	MAXIMUM CURRENT (AMPS)
ECV5N3-1	A		3.0
ECV5N6-1	B		6.0
ECV5N9-1	C	5	9.0
ECV5N12-1	D		12.0
†‡EC5N17	E		17.0
†‡EC5N25	F		25.0
ECV12N1.7	A		1.7
ECV12N3.4	B		3.4
ECV12N5	C	12	5.0
ECV12N6.8	D		6.8
†EC12N10	E		10.0
†EC12N16	F		16.0
ECV15N1.5	A		1.5
ECV15N3	B		3.0
ECV15N4.5	C	15	4.5
ECV15N6	D		6.0
†EC15N9.5	E		9.5
†EC5N14	F		14.0
ECV24N1.2	A		1.2
ECV24N2.4	B		2.4
ECV24N3.6	C	24	3.6
ECV24N4.8	D		4.8
†EC24N7.5	E		7.5
†EC24N10	F		10.0

ECV/EC DUAL OUTPUT MODEL SELECTION CHART—

MODEL NUMBER ADD-1 FOR OVP[1]	CASE SIZE	NOMINAL OUTPUT VOLTAGE	MAXIMUM CURRENT (AMPS)
ECV12D1	DA	± 12/15	1.0/0.8
		or + 12/–5	1.0/0.4
		or + 15/–5	0.8/0.4
ECV12D1.7	DB	± 12/15	1.7/1.5
		or + 12/–5	1.7/0.7
		or +15/–5	1.5/0.7
ECV12D3.4	DC	± 12/15	3.4/3.0
†EC12D5	E	± 12	5.0
†EC15D5	E	± 15	5.0

TRIPLE OUTPUT ET/ETV SERIES MODEL SELECTION CHART—

MODEL NUMBER ADD-1 FOR OVP[1]	CASE SIZE	OUTPUT NUMBER	NOMINAL OUTPUT VOLTAGE	MAXIMUM CURRENT (AMPS)
ETV251	TA	1	+5	2.0
		2	+9 to 15	0.4
		3	-9 to 15	0.4
			or -5	0.4
ETV351	TB	1	+5	3.0
		2	+12/+15	1.0/0.8
		3	-12/-15	1.0/0.8
			or -5	0.4
ETV401 -001	TD	1	+5	6.0
		2	+12 to 15	1.0
		3	-12 to 15	1.0
			or -5	0.4
ETV451	TC	1	+5	6.0
		2	+12/+15	1.7/1.5
		3	-12/-15	1.7/1.5
			or -5	0.7
ETV551	TE	1	+5	6.0
		2	+12/+15	1.7/1.5
		3	-12/-15	1.7/1.5
			or -5	
ETV651	TF	1	+5	12.0
		2	+12/+15	1.7/1.5
		3	-12/-15	1.7/1.5
			or -5	0.7
†ET601 -002	F	1	+5	12.0
		2	+12	3.0
		3	-12	3.0
†ET602 -003	F	1	+5	12.0
		2	+15	3.0
		3	-15	3.0

* EC, ET models have standard 105-125 VAC/210-250 VAC input. Optional universal transformers available for 208/220/240 VAC. Consult factory for price.

†‡ OVP standard on all 5 volt single output models except Case E and F.

* REQUIRES 50 CFM OF FORCED AIR COOLING

[1] All main 5V outputs on all models have built in OVP. Optional OVP

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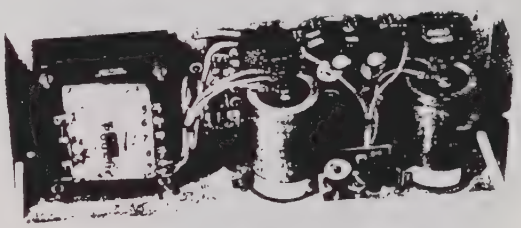
DISK MEMORY POWER SUPPLIES				
MODEL NUMBER ADD–1 FOR OVP [1]	CASE SIZE	OUTPUT NUMBER	NOMINAL OUTPUT VOLTAGE	MAXIMUM CURRENT (AMPS)
ECV15	D5	1	+5	2.0
		2	+12	4.0
ETV701	TK	1	+5	6.0
		2	-12	1.0
		3	+24	3.5/5.5 peak
ETV751	TG	1	+5	3.2
		2	5	[illegible]
		3	-24	5.0/6.0 peak
*ETV801	TL	1	+5	10.0
		2	-12/-5	1.6/1.0
		3	+24	2.0/5.5 peak
ETV851	TM	1	+5	2.2
		2	-5	0.2
		3	+24	1.2/3 peak
		4	+7 to 10	1.2 amp unregulated

AIM 65 POWER SUPPLY				
MODEL NUMBER ADD–1 FOR OVP [1]	CASE SIZE	OUTPUT NUMBER	NOMINAL OUTPUT VOLTAGE	MAXIMUM CURRENT (AMPS)
ETV201	TA	1	+5	2.0
		2	-24	0.5 average 1.7 peak

* REQUIRES 50 CFM OF FORCED AIR COOLING

[1] All main 5V outputs on all models have built-in OVP. Optional OVP



I.C Case E
Dual Output with OVP

Special Features—

- 3750 VRMS isolation primary to secondary
- 1500 VRMS isolation primary to case
- Leakage current less than 50 micro-amps
- Input and grounding circuitry as required for most international installations
- 100% vacuum varnish impregnated transformer with U.L. Class A insulation system
- Hermetically sealed power semi-conductors
- Computer grade, 10 year life electrolytic capictors
- IC regulator socket mounted
- Overvoltage protection standard on all 5V outputs
- Remote sense on all outputs — 30W or greater
- Channel Two on duals — Three on triples programmable to -5V
- U.L. recognized — File No. E48765
- CSA Certified — File No. LR47337
- Two year warranty
- Comprehensive product manual available

Electrical Specifications—

AC Input

Nominal Selectable transformer input taps for 100/117/220/230/240 VAC.

Operating Range 47-400Hz (Derate 10% for 50Hz operation).

Frequency, Phases Single Phase 47-440Hz.

Fusing External — input VA marked on all units.

Efficiency Up to 60%; 40% typical.

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SHEET 5

DC Output

Nominal Voltage	Refer to Model Selection Chart
Adjustments and Ranges	±5% nominal output, minimum
Regulation (Line)	±0.05% for ±10% line change.
Regulation (Load)	±0.05% for 50% load change.
Ripple (RMS)	2mV RMS Max.
Ripple (Pk-Pk)	3mV P-P typical; 10 mV P-P maximum.
Trans. Response	Output voltage returns to within regulation limits typically with 30 microsec in response to a 50% load step.
Overshoot	No turn-on or turn-off overshoot.
Overload Protection	Inherently protected against overload and short circuit by a foldback type of characteristic. Recovery is automatic
Overvoltage Protection	Standard on all +5V outputs. Preset at 6.2 ±0.4V (fixed). Overvoltage protection optional. Universal OVP module available for any model. Adjustable 4.5-36V. Typical setting 10-20% above operating voltage.

Dual Output Models

Crowbars both outputs. Typical setting 3-4V above sum of operating voltage.

Triple Output Models

OVP Universal on +5V outputs. Optional on outputs 2 and 3 as above. Overvoltage modules do not add to outline dimensions.

Remote Sense	Standard on most models to compensate for up to 0.25 volt drop in the load cable. Open sense lead protection is built in on all units.

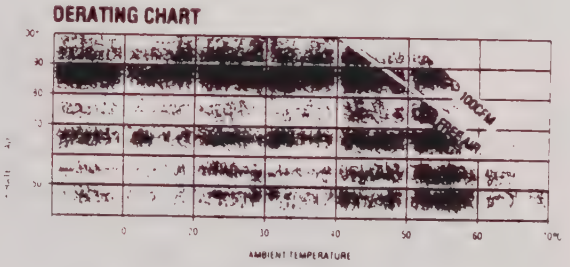
Environmental

Operating Temperature	0-70°C. Full rating to 50°C. See derating chart.
Storage Temperature	-55°C to 85°C.
Temperature Coefficient	0.02%/°C.
Stability	Typically ±0.15% for 24 hours after initial warm-up.
Cooling	Natural convection
Humidity	Up to 95% R.H., Non-Condensing

Standard Options—

Universal Overvoltage Protection — This SCR crowbar module can be added within the published outline to any universal series power supply with an output voltage of other than 5V. On multi-output models it is usually installed across both outputs (output 2 & 3 on triples) and is adjusted to trip and short both outputs if their sum exceeds a predetermined level.
This overvoltage module can be used on any regulated power supply output with a load rating less than 15A which has fold-back type current limiting. It is adjustable from 4.5V to 36V.

DERATING CHART

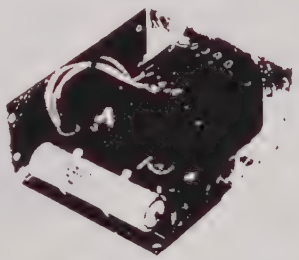


Ordering Information:

Order by specific model from selection chart. If OVP is desired on a single output model other than 5V, or on a multi-out model, add a -1 to the model number.

The OVP module with mounting hardware is shipped as a separate item in the container. Installation and adjustment procedures are included.

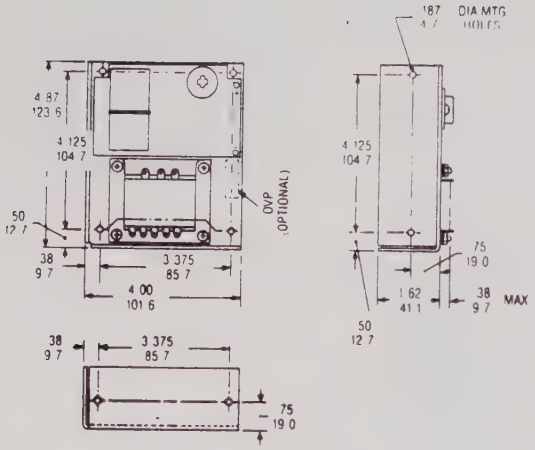
Your local distributor can ship these models from stock and perform many value added services, such as installing OVP's. See listing of distributors at rear of this catalog.



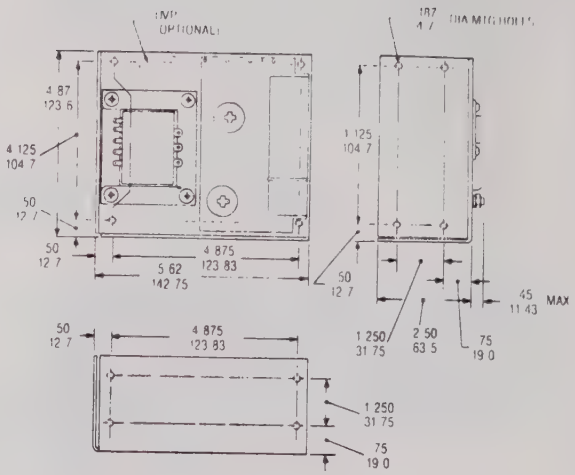
ECV Single Output
Case B

136-079-□
SHEET 6

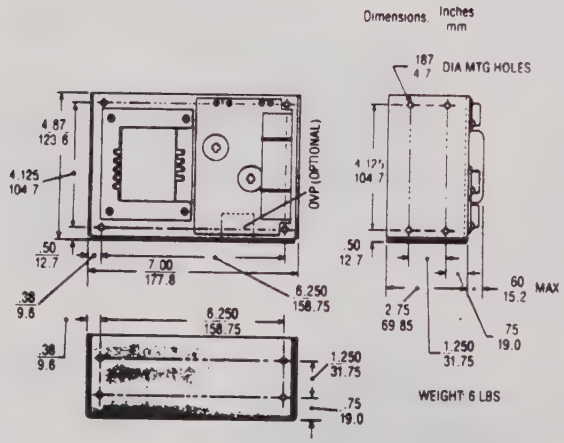
Mechanical Specifications—



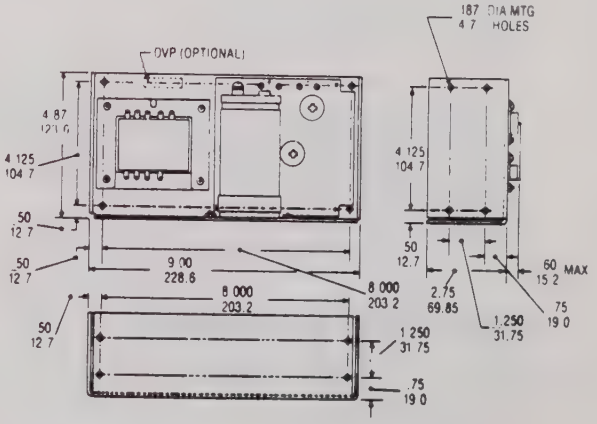
ECV Case A



ECV Case B



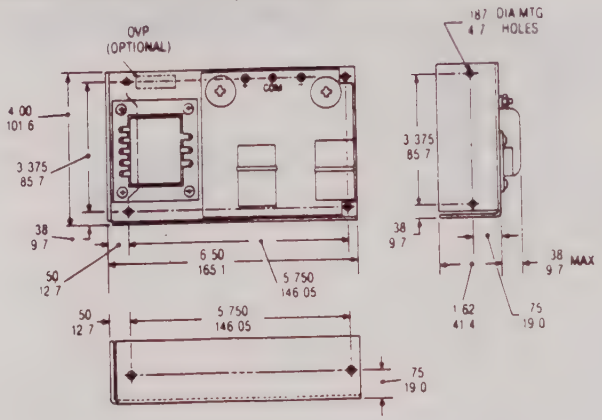
ECV Case C



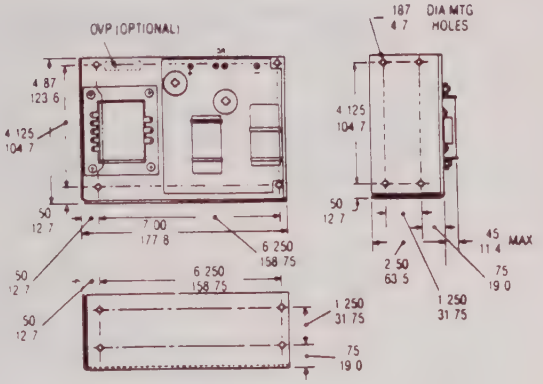
ECV Case D

136-079-□
SHEET 7

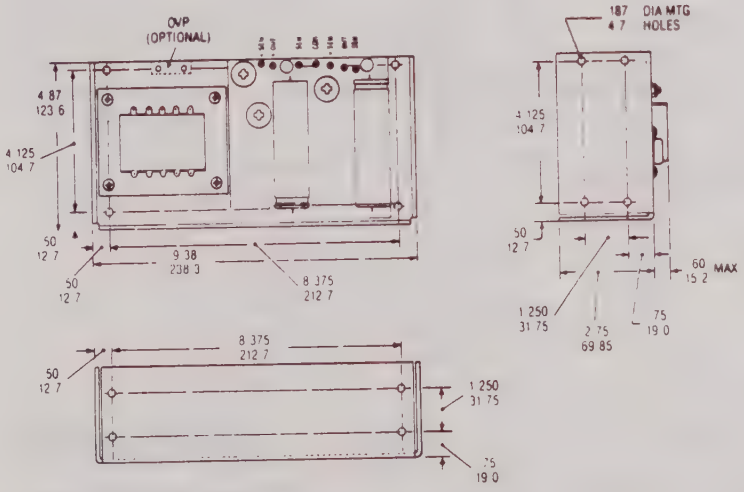
Mechanical Specifications—



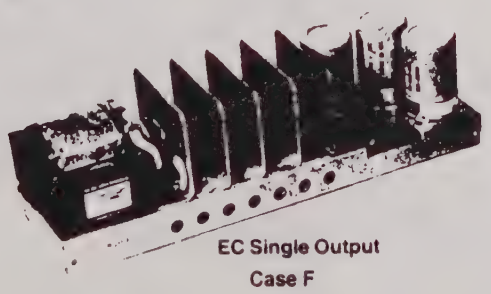
ECV Case DA/TA



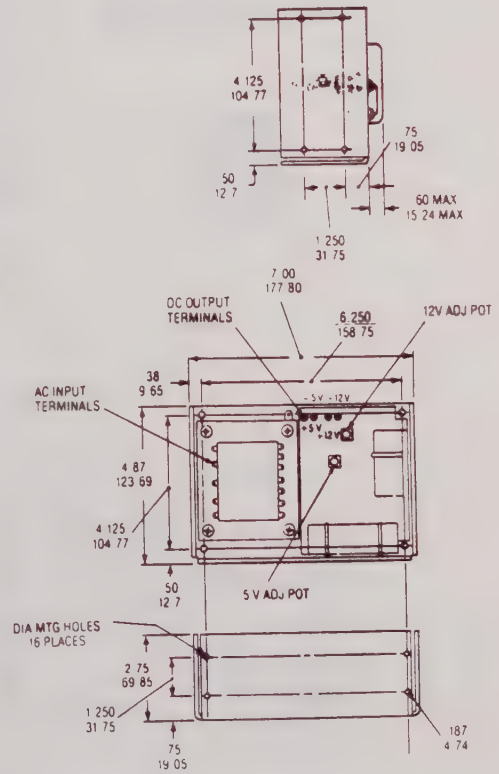
ECV Case DB



ECV Case DC



EC Single Output
Case F



ECV Case D5

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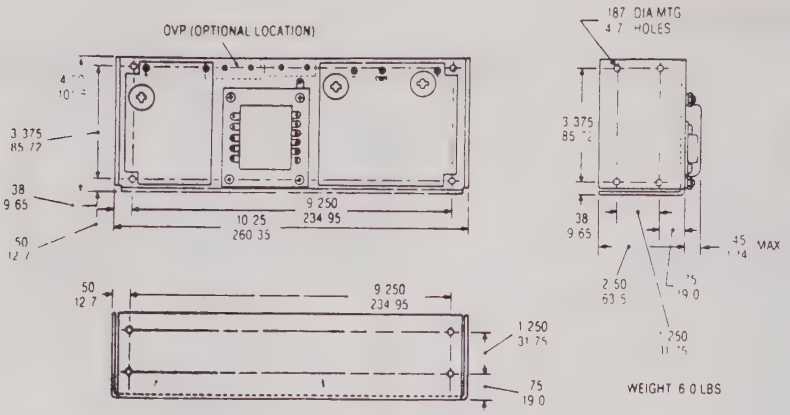
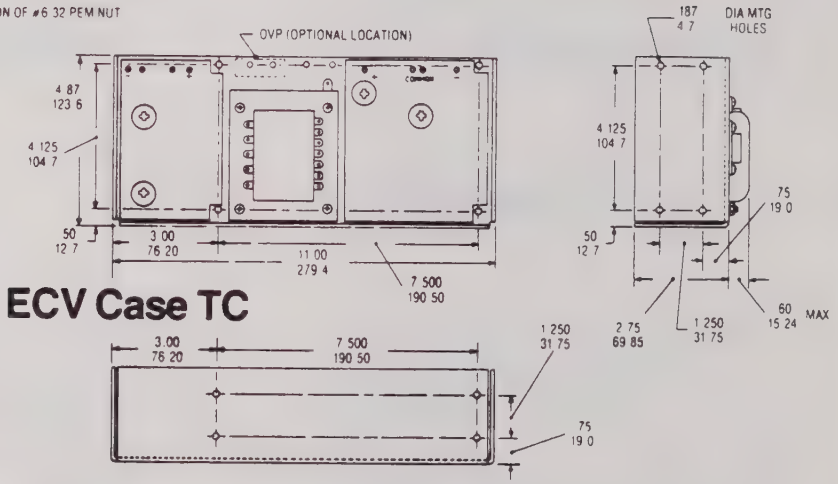
ECV Case TB

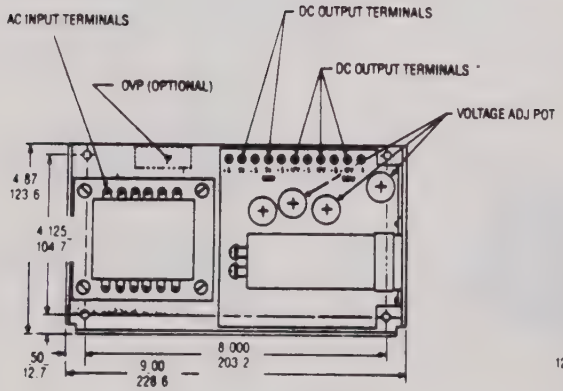


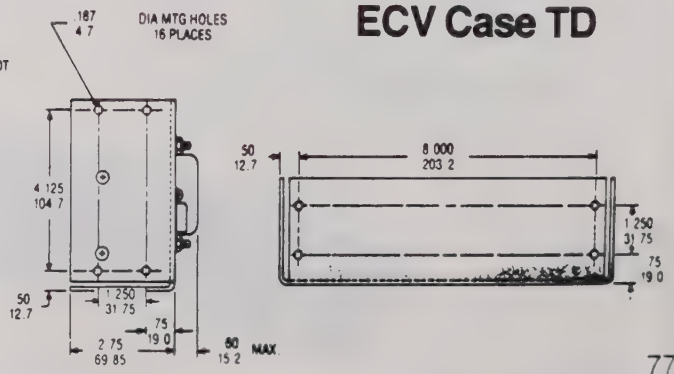
2 MTG HOLES ARE CORRECT SIZE FOR INSTALLATION OF #6-32 PEM NUT

ECV Case TC



ECV Case TD





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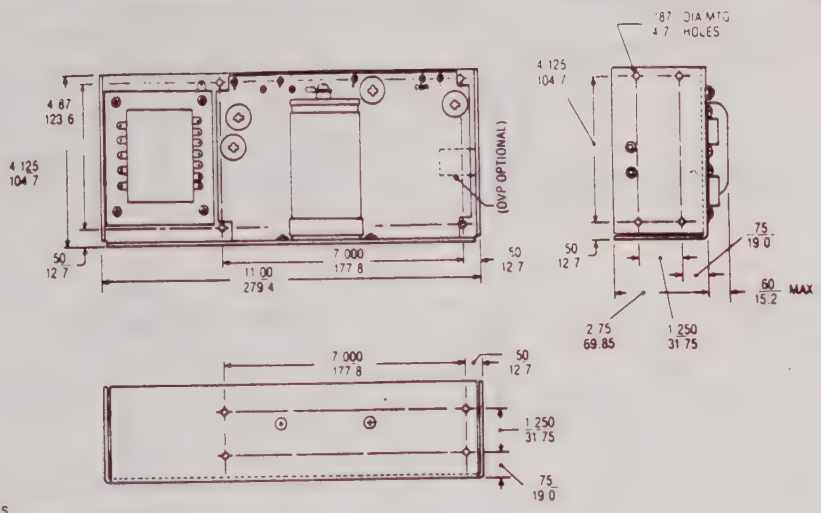
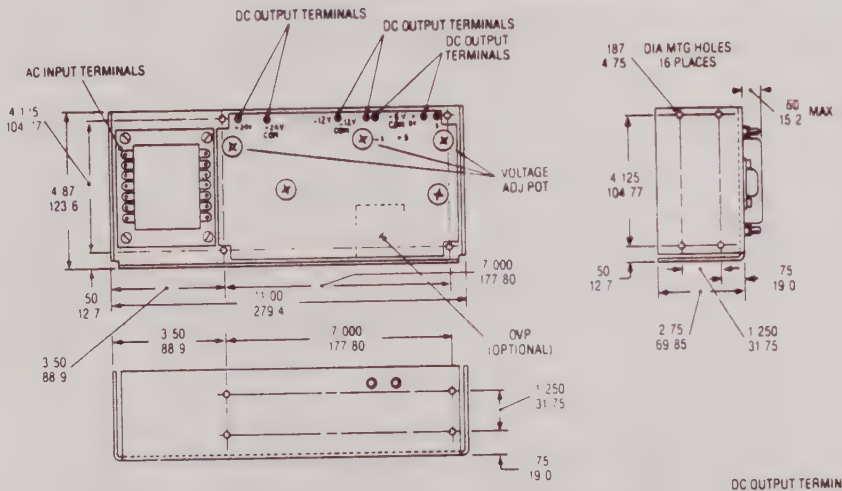
SHEET 9

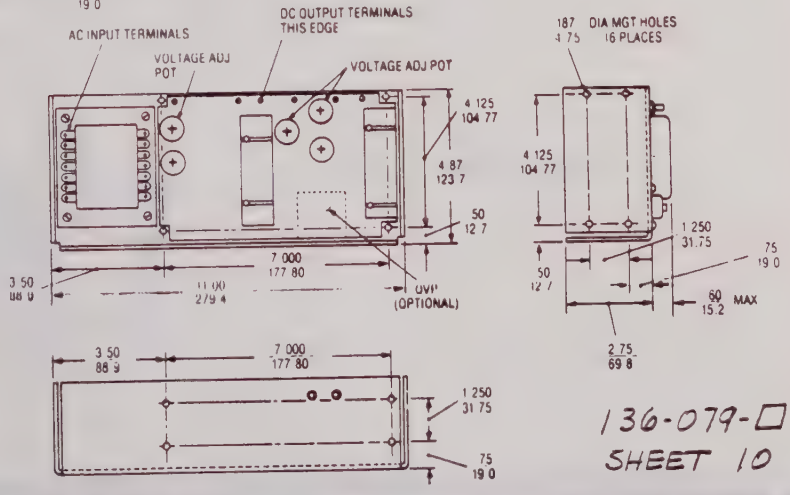
ECV Case TE/TG



ECV Case TK



ECV Case TL



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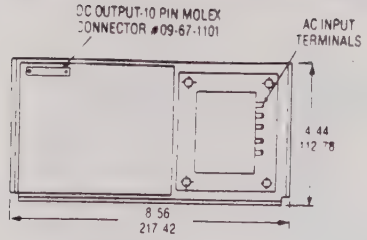
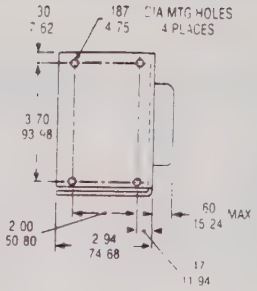
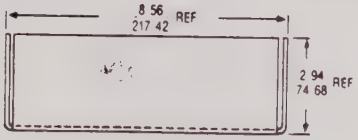
SHEET 10

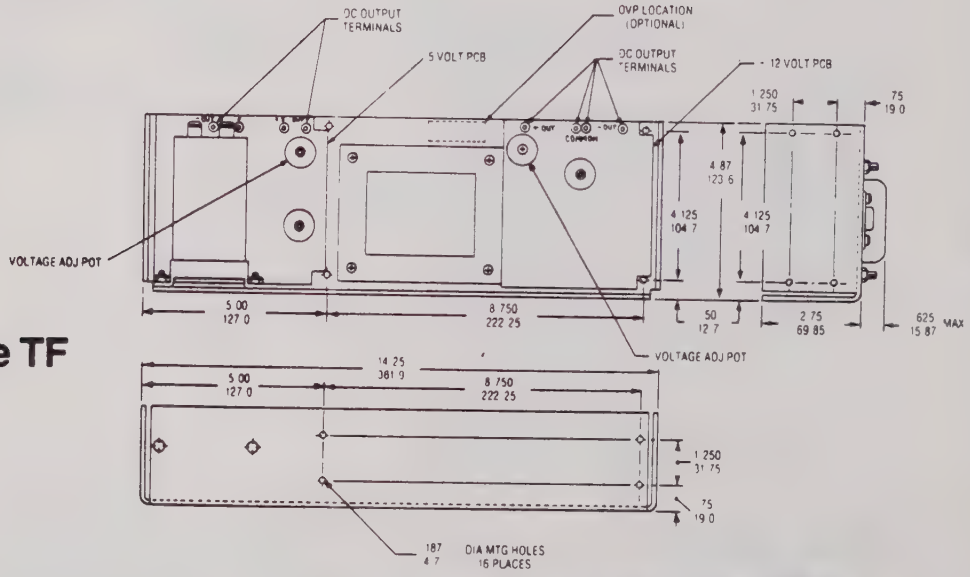




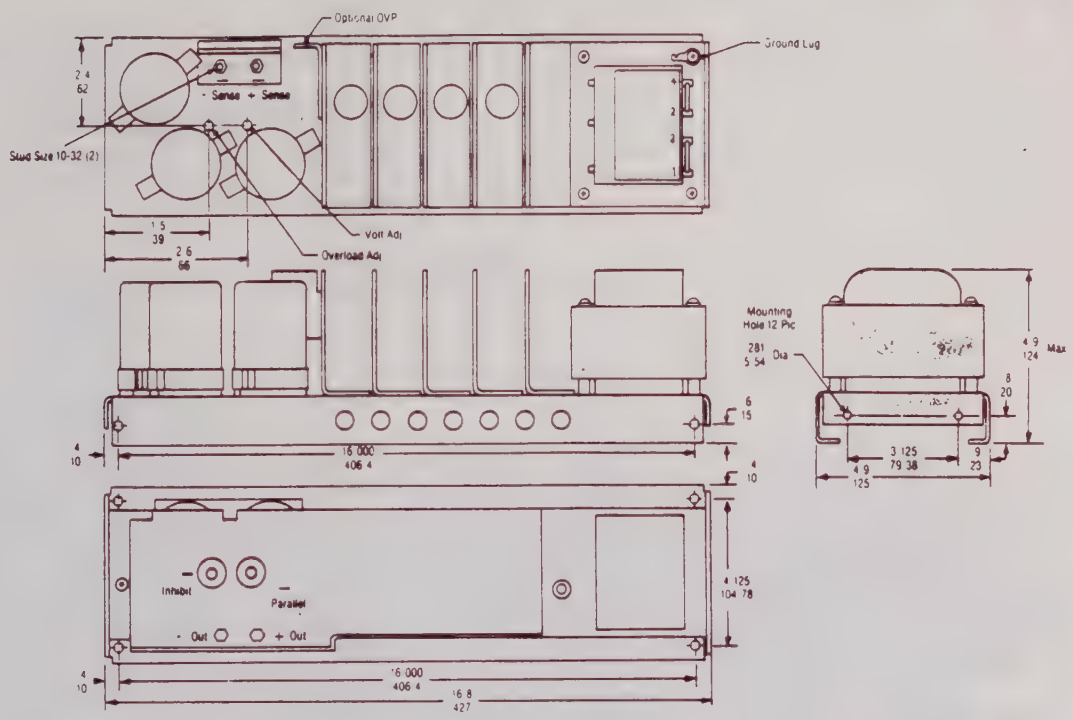


ECV Case TM

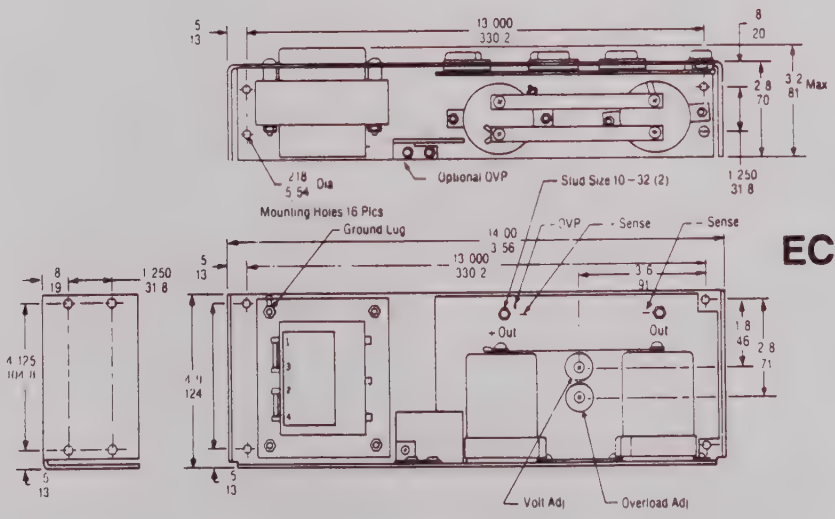
ECV Case TF



136-079-□
SHEET 11



EC Series Case F



EC Series Case E

136-079-□
SHEET 12

APPENDIX B

Model 1126B Interface
Option 11, Model Number 356-0002-502

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This appendix contains the information needed to supplement the manual, in order to operate and maintain a Model 335 PCM Bit Synchronizer, part number 356-0002-502, suppled with an interface for the Model 1126B PCM Decommutator (option 11).

1.2 PHYSICAL DESCRIPTION

Figure B1-1 shows the modified rear panel for the -502 unit. The front panel is not changed by the addition of the interface. Figure B1-2 shows the top view of the -502 unit.

Circuit modifications to the standard bit synchronizer are made with the addition of circuit card type UX801-30 to card slot A4A5.

1.3 BASIC FUNCTIONAL DESCRIPTION

The functional changes to the bit synchronizer that make it compatible with the Model 1126B are as follows:

a. The separate READ and WRITE requests are changed to a READ/WRITE controlled by a single line (0 volts indicates READ control and +5 volts indicates WRITE control).

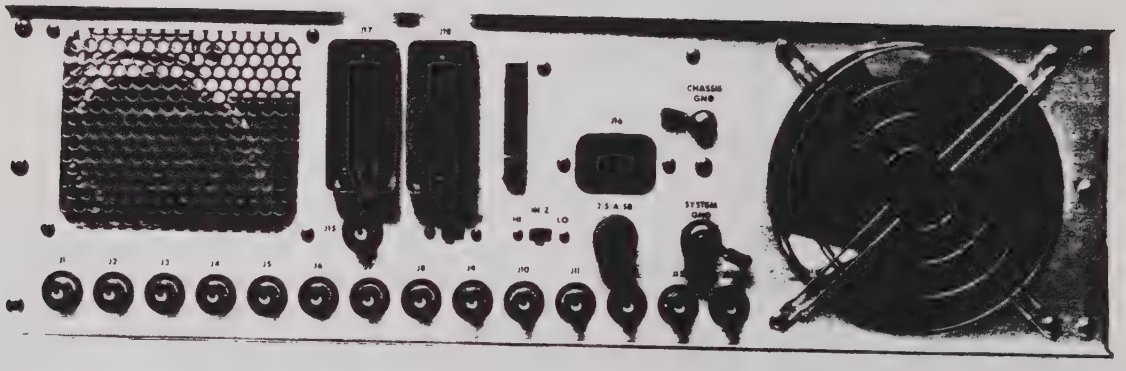
b. The control of the WRITE request by the input acknowledge, is changed to control of the R/W acknowledge by the TRANSFER and VERIFY strobes.

c. LOCAL/$\overline{\text{REMOTE}}$ status is added.

d. Continuous source status is added.

e. Continuous loss status is added.

f. Continuous sync status is added.



B-1701

Figure B1-1. Model 335 Bit Synchronizer, -502, Rear View

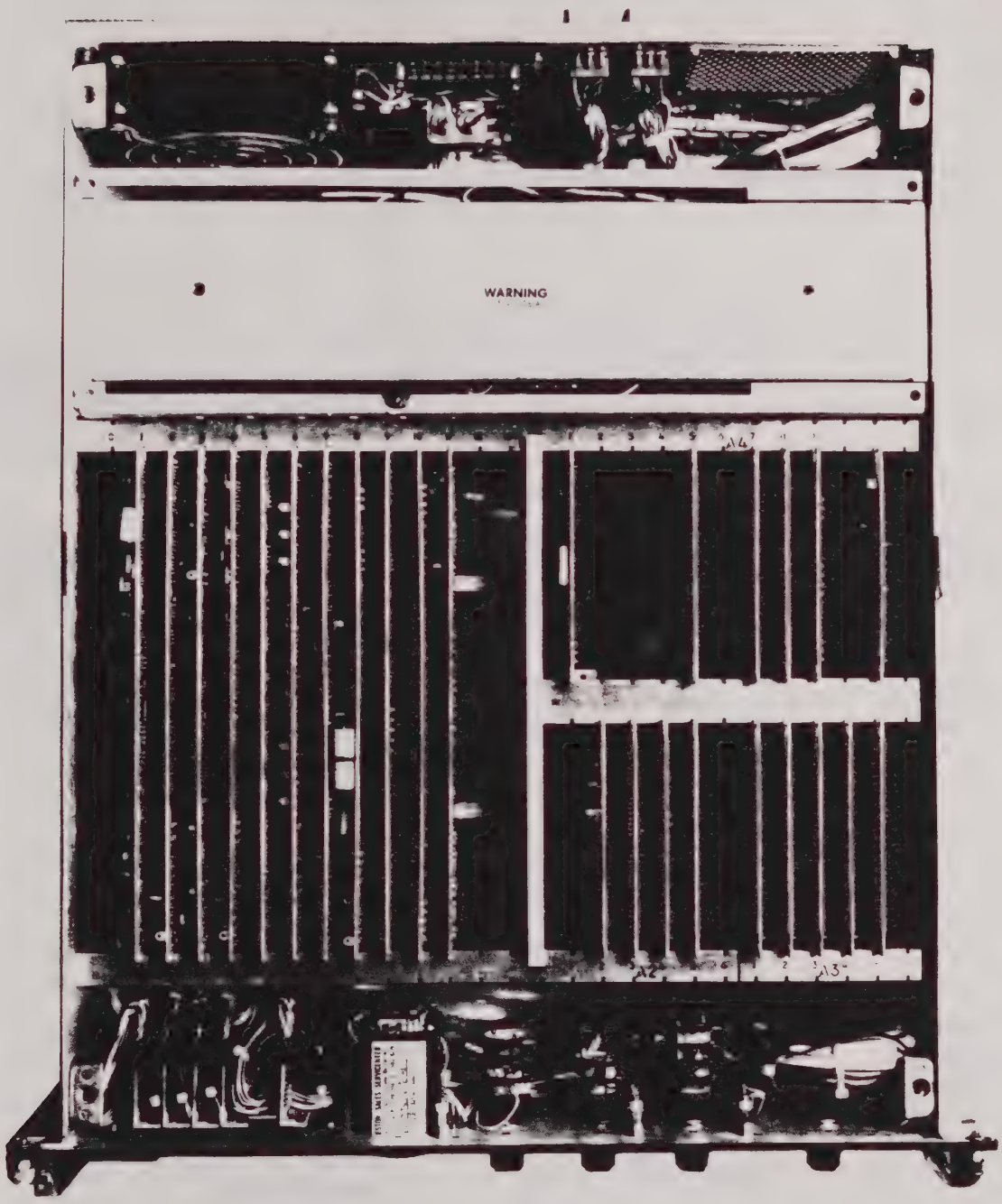


Figure B1-2. Model 335 Bit Synchronizer, -502, Top View

SECTION II

INSTALLATION

2.1 GENERAL

The additional pc card associated with this option is factory installed.

2.2 WIRING CHANGES

Logic/schematic drawing 481-0026-30 in section VI indicates wiring instructions for the UX801-30 card. Also included in section VI is drawing 730-2011, an add and delete wire list for this modification to the bit synchronizer.

2.3 REAR PANEL CONNECTIONS

The function of each rear panel BNC connector is given in table B2-1.

Table B2-1. BNC Rear Panel Connectors

DESIGNATION	FUNCTION
J1	+3v 0° Clock 2 Output
J2	+3v 90° Clock 2 Output
J3	+3v NRZ 2 Output
J4	+3v 0° Clock 1 Output
J5	+3v 90° Clock 1 Output
J6	+3v 180° Clock Output
J7	+3v 270° Clock Output
J8	+3v NRZ 1 Output
J9	Tape Recorder NRZ-L Output
J10	Tape Recorder BiØ-L Output
J11	Data Input 4
J12	Data Input 3
J13	Data Input 2
J14	Data Input 1
J15	External Clock Input

SECTION III

OPERATION

3.1 GENERAL

This section contains information on operation and programming the bit synchronizer with the optional interface.

3.2 REMOTE PROGRAMMING

Table B3-1 gives the function of each J17/J18 pin connection. Table B3-2 contains the setup and programming instructions for the bit synchronizer. With this optional interface, the bit synchronizer can be programmed through its front panel or through the Model 1126B.

Table B3-1. J17/J18 Remote Programming Connectors

PIN	SIGNAL	REMARKS
A	CB0/VR0	Instruction/Verify
B	CB1/VR1	
C	CB2/VR2	
D	CB3/VR3	
E	CB4/VR4	
F	CB5/VR5	
H	CB6/VR6	
J	CB7/VR7	
K	CB8	Function Address
L	CB9	
M	CB10	
P	CB12	Unit Address
R	CB13	
S	CB14	
T	CB15	

PIN	SIGNAL	REMARKS
AA	SOURCE 2^0	Program Status
BB	SOURCE 2^1	
DD	SIGNAL $\overline{\text{LOSS}}$/PRESENCE	
CC	SYNC LOCK	
EE	LOCAL/$\overline{\text{REMOTE}}$	
U	TRANSFER STROBE	Remote Program Control
V	R/W ACK. PULSE	
W	TRANSFER STROBE RETURN	
X	$\overline{\text{R/W}}$ REQUEST	
Z	D-GND	
LL	LOOP RESET	
MM	D-GND	
NN	D-GND	

NOTE: Remaining pins are wired between J17 and J18, but are unused internally in the Model 335.

Table B3-2. 16-Bit Setup Word Format

	UNIT ADDRESS				FUNCTION ADDRESS			INSTRUCTION							
BIT NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIN NO. J17/J18	T	S	R	P		M	L	K	J	H	F	E	D	C	B	A
WORD 1	0	0	0	1	-	0	1	1	MSD				NMSD			
WORD 2	0	0	0	1	-	0	1	0	NLSD				LSD			
WORD 3	0	0	0	1	-	0	0	1	SOURCE			MULTIPLIER			-	POL
WORD 4	0	0	0	1	-	0	0	0	-	-	CODE				LOOP	

With SN7437N as a driver, the continuous status outputs are TTL compatible logic levels. Refer to the chart below for the continuous status output parameters.

Status Outputs \ J17/J18	AA	BB	CC	DD	EE
Source 1	0	0			
Source 2	1	0			
Source 3	0	1			
Source 4	1	1			
Sync Lock	X	X	1	X	X
Out of Sync	X	X	0	X	X
Signal Present	X	X	X	1	X
Loss of Signal	X	X	X	0	X
Local	X	X	X	X	1
Remote	X	X	X	X	0

SECTION IV

THEORY OF OPERATION

Refer to logic drawing 481-0026-30 in section VI. With one exception, the NAND gates in A1 and A3 act as inverters, converting signals to be output to rear panel remote programming outputs J17/J18. The exception is A1-3, which gates the VERIFY STROBE and TRANS STROBE to produce the R/W acknowledge pulse described in paragraph 1.3 (a high indicates WRITE control and a low indicates READ control).

SECTION V

MAINTENANCE

No additional maintenance procedures are necessary with the 1126B interface.

SECTION VI

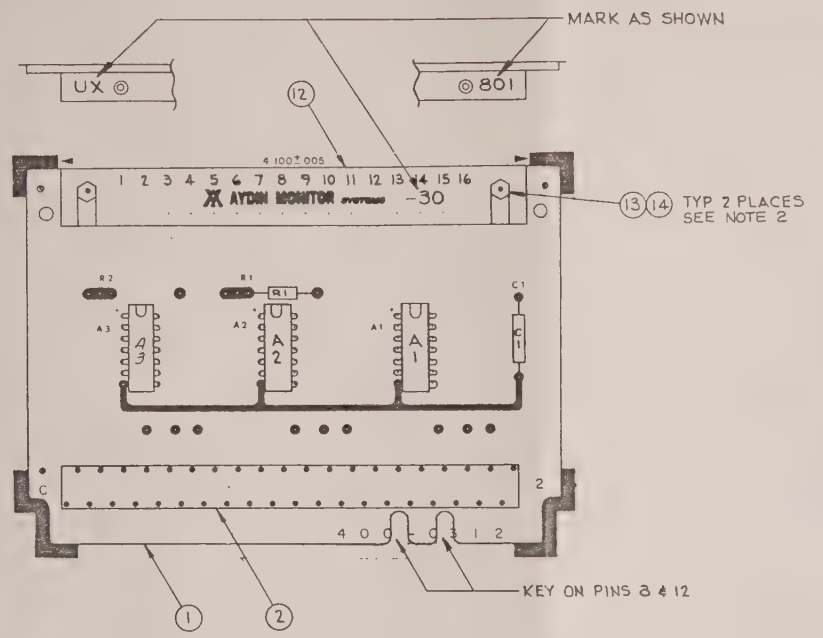
DRAWINGS AND PARTS LIST

This section contains drawings and parts lists associated with the -502 unit. See table B6-1 for a list of the drawings. See table 6-2 in the main manual for the manufacturers' codes used in the parts list.

Table B6-1. Drawings and Parts List

DRAWING	NUMBER
Card Assembly Monilogic Type UX801-30, assembly drawing, schematic/logic drawing and parts list	481-0026-30
Model 335 Mod. for 1126B Interface	730-2011

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 03474 JSG	8/21/78	[illegible]
	C	REVISED PER ECO 04120 JST	5-14-79	[illegible]
	D	REVISED PER ECO 05185 WKH 6-12-80	6/12/80	JFD
	E	REVISED PER ECO 06177 BAKER 6 APR 81	1 APR 81	PSW
	F	REVISED PER ECO 06583 BAKER 20 JUN 81	20 JUN 81	PSW



QTY 501	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
AR	16	81348	120-101-001	SN63BS	SOLDER	QQ-S-571
	15					
2	14	72962	129-001-003	92-1660-40	NUT, HEX, MINIATURE, #4-40	
2	13	96906	127-109-104	MS51957-104	SCREW, PAN HD, 4-40×5/16	
1	12	97954	108-900-001	UTP-16	CONNECTOR, TEST POINT	
	11					
	10					
	9					
1	8	81349	100-003-102	RC07GF102J	RESISTOR, 1K, 1/4W, 5%	R1
	7					
1	6	01295	139-046-400	SN7400	INTEGRATED CKT, TTL	A1
1	5	01295	139-198-113	SN74LS113	INTEGRATED CKT, TTL	A2
1	4	01295	139-046-437	SN7437	INTEGRATED CKT, TTL	A3
1	3	14752	102-001-473	230B1B473	CAP, .047 UF, 100V, 20%	C1
1	2	91662	108-203-040	7022-040-000-001	CONNECTOR, FINGER BLOCK	
1	1	20747	400-0312	——	BOARD, PRINTED WIRING	

LIST OF MATERIALS

NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG NO. 401-0010.
2. TEST POINT BLOCK MOUNTING SCREW AND NUT (ITEM 13 & 14) ARE OPTIONAL, MANDATORY ONLY WHEN SPECIFIED ON MA OR ERN.

DRAWN J. BAKER	DATE 12-28-77
CHECKED F. HINKLE	12-29-77
DRAFTING ES	12-29-77
ENGINEER F. HINKLE	12-29-77
MFG. G.L. BROWN	1-3-78
APPROVED D.D. Mount	12-30-77
APPROVED [illegible]	1/2/78

AYDIN MONITOR SYSTEMS
PORT WASHINGTON, PENNA. 19034

CARD ASSEMBLY
MONILOGIC TYPE
UX801-30

NEXT ASSY	USED ON
352-0557-506	2782

APPLICATION

SIZE D | CODE IDENT NO. 20747 | 481-0026-30 | REV F

SCALE 2/1 | SHEET 1 OF 2

REVISIONS				
REV.	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO #06063 JSG		4MAR	BVL

GENERAL NOTES

1. For additional information see Assembly Drawing 356-0002-501
2. Unless otherwise indicated, all wire is MIL-W-16878, type B, #26 AWG white.
3. Chains must be run in order shown.

NOTE - TO GENERATE MODEL 356-0002-502
Dete wires shown on Sh 2
add wires shown on Sh 3+4

SHEET	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	
REVISION																				
SHEET	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
REVISION																				
SHEET	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REVISION																				
SHEET	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
REVISION																				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REVISION	B	B	A	B																

MONITOR
an AYDIN company
FORT WASHINGTON, PENNSYLVANIA

TITLE MODEL 335 MOD.
FOR 1126B INTERFACE.

CODE IDENT 20747
CONTRACT NO.

DRAWN	[illegible]	7-1-80	ENGINEER	[illegible]	[illegible]	DWG NO. 730-3011	REV B
CHECKED			APPROVED	BVL	16 OCT 80		
DRAFTING			MFG	[illegible]		SIZE A	SHEET 1 OF 4

FORM NO. 800-0126B

LINE	FUNCTION NAME/CODE	Remove WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
1	READ	J17-X	A4A7-11	A4A2-11			GRN/W
2	WRITE	J17-Y	A3A5-7				BRN/W
3	ACK.	J17-V	A4A7-4				RED/W
4		J17-AA	A4A8-40				BLK
5		J17-BB	A4A8-36				RED
6		J17-CC	A4A8-33				WHT
7		J17-DD	A4A8-30				GRN
8		J17-EE	A4A8-28				ORG
9		J17-FF	A4A8-23		BUNDLE TOGETHER & PUT SLEEVING OVER ENDS.		BLU
10		J17-HH	A4A8-20				BRN
11		J17-JJ	A4A8-17				YEL
12		J17-KK	A1A9-27		PUT SLEEVING OVER END.		VIO

NOTE: J17 WIRES WILL BE REPOSITIONED, DO NOT REMOVE WIRES FROM J17

REMOVE THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST # 760-0219 AND CABLE WIRE LIST #730-1702 TO GENERATE MODEL 352-0557-506/356-0002-502

MONITOR SYSTEMS INC.

DRAWN	TITLE MODEL 335 MOD. FOR 1126 B INTERFACE.	CODE IDENT NO. 20747	DWG NO. 730-2011	REV B
DATE			SHEET 2 OF 4	

800-0118

800-0118

LINE	FUNCTION NAME/CODE	A2D. WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
1	$\overline{R/W}$	J17-X	A3A5-7	A4A7-27			
2	LOCAL/REMOTE	J17-EE	A4A5-10				
3	$\overline{R/W}$ ACK.	J17-V	A4A8-4				
4		A4A7-18	A4A7-11	A4A8-11			
5	LOCAL/REMOTE	A3A1-39	A4A5-11	A4A5-12			
6		A4A7-12	A4A8-27				
7	VERIFY STROBE	A4A8-18	A4A5-15				
8	TRANS. STROBE	A3A5-4	A4A5-14				
9	R/W ACK	A4A5-13	A4A8-10				
10		A4A8-13	A4A8-5				
11	1B1	A2A4-26	A4A5-7	A4A5-8			
12	1B2	A2A4-27	A4A5-4	A4A5-5			
13	LOSS	A1A9-25	A4A5-32	A4A5-33			
14	$\overline{SYNC}$	A1A11-7	A4A5-29	A4A5-30			
15	$\overline{1B1}$	A4A5-9	A4A5-39	A4A5-40			
16	$\overline{1B2}$	A4A5-6	A4A5-36	A4A5-37			
17	2^0	J17-AA	A4A5-38				BLK.
18	2^1	J17-BB	A4A5-35				RED
19	SYNC STATUS	J17-CC	A4A5-31				WHT.
20	$\overline{LOSS}$	J17-DD	A4A5-34				GRN.

ADD THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST # 760-0219 AND CABLE WIRE LIST # 730-1702 TO GENERATE MODEL 352-0557-506/356-0002-502

MONITOR SYSTEMS INC.

DRAWN	TITLE MODEL 335 MOD. FOR 1126B INTERFACE	CODE IDENT NO.	DWG NO. 730-2011	REV
DATE		20747	SHEET 3 OF 4	A

800-0118

800-0118

LINE	FUNCTION NAME/CODE	ADD WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
21	CB0/VR0	A4A8-40	A3A5-20				
22	CB1/VR1	A4A8-36	A3A5-23				
23	CB2/VR2	A4A8-33	A3A5-25				
24	CB3/VR3	A4A8-30	A3A5-14				
25	CB4/VR4	A4A8-28	A3A5-17				
26	CB5/VR5	A4A8-23	A3A5-19				
27	CB6/VR6	A4A8-20	A3A5-5				
28	CB7/VR7	A4A8-17	A3A5-9				
29	+5V P/U	A4A5-24	A4A5-25	A4A5-26	A4A5-28		

ADD THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST # 760-0219 TO GENERATE MODEL 352-0557-506/356-0002-502

MONITOR SYSTEMS INC.

DRAWN	TITLE MODEL 335 MOD. FOR 1126 B INTERFACE	CODE IDENT NO. 20747	DWG NO. 730-2011	REV B
DATE			SHEET 4 OF 4	

800-0118

800-0118

APPENDIX C

Soft Bit Decision
Option 21; Model Number 356-0002-503

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This appendix contains the information needed to supplement the manual, in order to operate and maintain a PCM Bit Synchronizer Model 335, part number 356-0002-503, supplied with soft bit decision (option 21).

1.2 PHYSICAL DESCRIPTION

The front and rear views of the bit synchronizer are not changed with the addition of soft bit decision. Figure C1-1 shows the top view of the -503 unit.

Modifications to the standard bit synchronizer have been made by the addition of two circuit cards in library file A4.

A4A3 - BLD001-1, Bit Level Detector
A4A4 - BLD002-2, Bit Level Digitizer

1.3 OVERALL FUNCTIONAL DESCRIPTION

A simplified block diagram of the bit synchronizer with soft bit decision is shown in Figure C1-2. The soft bit decision processing section accepts the NRZ signals from the input processing section. The MSB, or HF-NRZ*, is fed back to the input processing section; this is the hard bit decision indicating the direction of zero crossing of the signal. To obtain the LSB and NMSB bits, the signal is sampled in the soft bit decision section as to the amount of noise carried on the signal. The result of this sampling is output to the line drivers, configured as 00, 01, 10 or 11, with 11 indicating a large amount of noise. Figure C1-3 is a chart showing the noise/bit association.

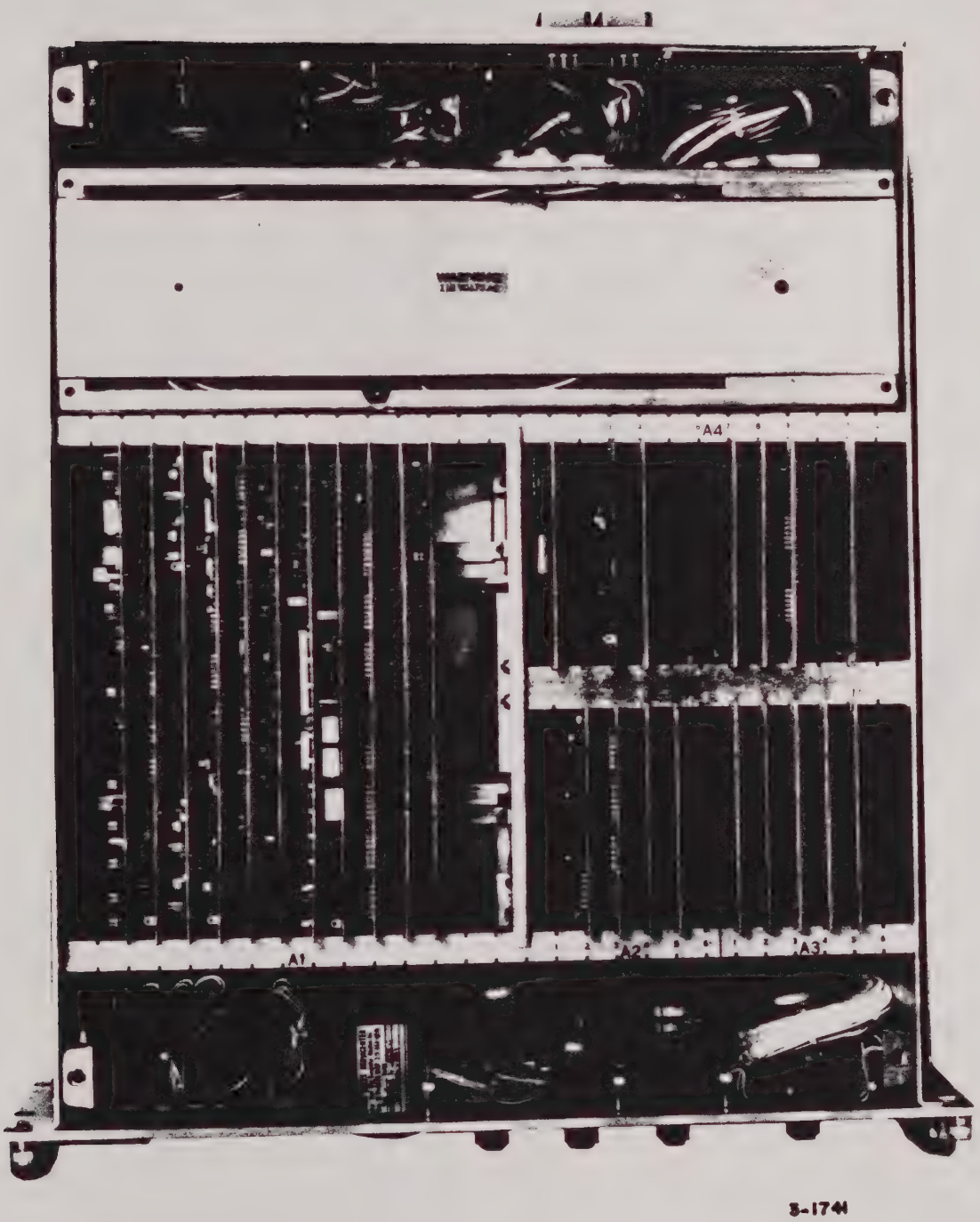


Figure C1-1. Model 335 Bit Synchronizer, -503, Top View

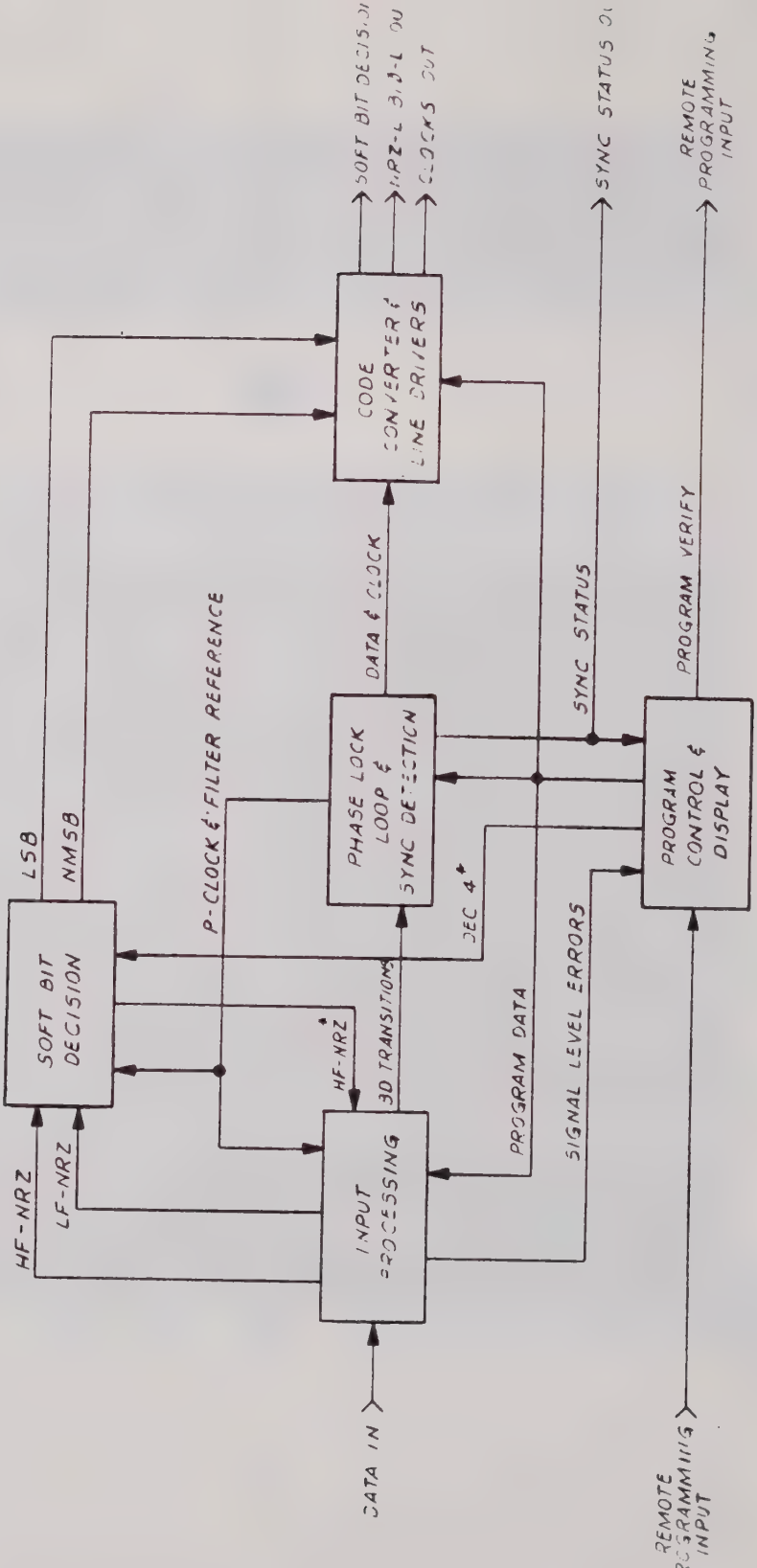


Figure C1-2. Model 335 Bit Synchronizer with Soft Bit Decision, Simplified Block Diagram

Figure C1-3. Soft Bit Decision Processor Section, Waveform Diagram

SECTION II

INSTALLATION

2.1 GENERAL

The two printed circuit cards associated with a -503 unit bit synchronizer are factory-installed.

2.2 REAR PANEL INPUT/OUTPUT CONNECTIONS

The function of each BNC connector is given in table C2-1.

Table C2-1. BNC Rear Panel Connectors

DESIGNATION	FUNCTION
J1	Parallel A/D LSB
J2	Parallel A/D NMSB
J3	Parallel A/D MSB
J4	+3v 0° Clock Output
J5	+3v 90° Clock Output
J6	+3v 180° Clock Output
J7	+3v 270° Clock Output
J8	+3v NRZ-L Output
J9	Tape Recorder NRZ-L Output
J10	Tape Recorder BiØ-L Output
J11	Data Input 4
J12	Data Input 3
J13	Data Input 2
J14	Data Input 1
J15	External Clock Input

Output logic levels:

J1 through J8 are 0v ±0.5v to 3.5v ±0.5v
J9 and J10 are adjustable from 2.0v p-p to 6.0v p-p
All outputs should be terminated into 50 ohms.

SECTION III

OPERATION

3.1 GENERAL

The operation procedures of the Model 335 Bit Synchronizer are not affected by the addition of soft bit decision circuitry.

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

The soft decision circuitry is located on card BLD001-1. PC Card BLD002-2 contains both the digital timing logic and the -5 volt power supply.

4.2 FUNCTIONAL DESCRIPTION

Figure C4-1 is a simplified block diagram of the functions within the soft bit decision processing section.

The AGCed signal from the input processing section is fed to the soft bit decision processing section through LF and HF line receivers. The line driver sends the hard bit decision (HF-NRZ*), which indicates the direction of zero crossing of the signal (see Figure C1-3), back to the input processing section. The HF-NRZ* then travels through the phase lock loop and code converter sections of the bit synchronizer, and emerges at the output as the MSB of the 3-bit soft bit decision.

DEC 4*, along with the LF-NRZ and HF-NRZ signals, is fed through the switching area, where the correct circuit elements are gated, according to whether a high frequency or a low frequency signal is being processed at a given time. The output of the switch is fed to the threshold detector, where it is compared with the reference voltages. The comparison voltages are fed to the OR gate section, where they are inverted and combined. The NMSB is determined here, with the ORing of +V2 and $-\overline{V2}$. The signals pass from the OR gates to the first flip-flop, which samples the results at the end of each bit period, and thus establishes which noise level for each bit period will be output as soft decision. V1, $\overline{V2}$, and $\overline{V3}$ are output from this flip-flop to the LSB logic section, where they are gated together to produce the LSB.

The NMSB and LSB are sent to the second flip-flop, which delays the signal by three bits. This ensures that the NMSB and LSB reach the bit synchronizer output concurrently with the MSB, which as stated previously, has been routed through the phase lock loop and code converter sections. (See figure C1-2.) Both flip-flops are clocked by the clock receiver, which obtains its signal from the phase lock loop section.

4.3 CIRCUIT DESCRIPTION - BLD001-1

See drawing 460-1161 in section VI for the schematic of this card.

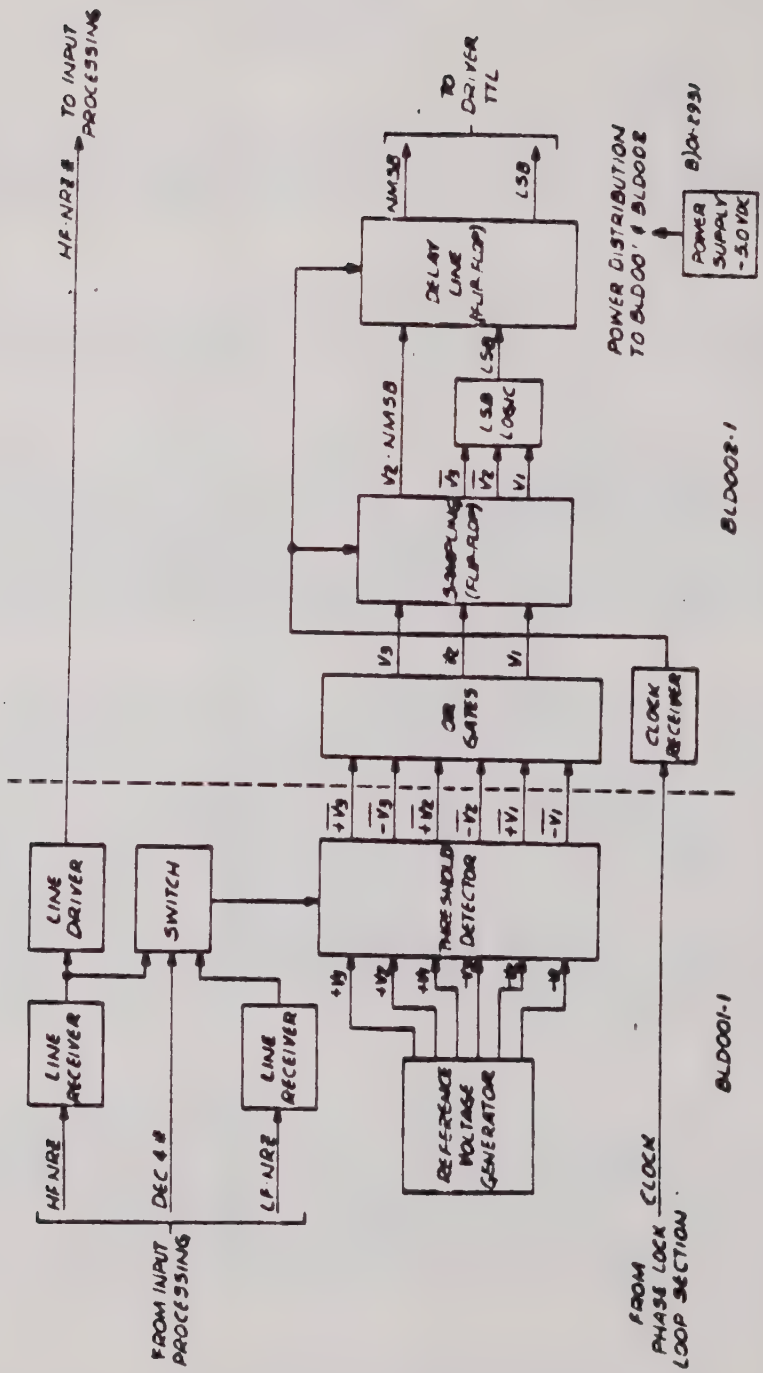


Figure C4-1. Soft Bit Decision Processing, Functional Block Diagram

The balanced push-pull output (HF-NRZ and $\overline{\text{HF-NRZ}}$, pins 37 and 38) from the high frequency (>10 Kbps) NRZ matched filter is terminated and converted to single-ended form by the differential amplifier consisting of Q1 and U1Q3 to U1Q5. Q2 and U2Q5 serve to stabilize the differential amplifier. R6 is adjusted to compensate for any unbalances and thus ensures that the single-ended signal is centered about ground. The single-ended signal which appears on the collector of U1Q4 is applied to the base of U1Q2, and to the phase splitter, consisting of U2Q3, U2Q4 and Q3. The original push-pull signal is regenerated (HF-NRZ* and $\overline{\text{HF-NRZ}}$*, pins 25 and 26) in the phase splitter, for use by the signal conditioning portion of the bit synchronizer.

The corresponding balanced push-pull output (LF-NRZ and $\overline{\text{LF-NRZ}}$, pins 32 and 33) from the low frequency (<10 Kbps) matched filter is buffered by U3 and converted to single-ended form by differential amplifier U4. R48 is adjusted to precisely match the amplitude of the low frequency to that of the high frequency signal, and R45 is adjusted to center the low frequency signal about ground. Unlike the HF-NRZ, the LF-NRZ signal is not terminated in the BLD001, but is instead bridge-tapped; therefore the LF-NRZ does not have to be regenerated.

U1Q1 & U1Q2 and U2Q1 & U2Q2 function as combined offset-compensated emitter followers and analog switches. For bit rates of 10^4 or higher, the DEC 4 (pin 34) is a logic 1 so that Q7 is conducting and Q6 is off. Consequently, Q5 is off and Q4 is on, thereby supplying current to the emitter of U1Q2. Therefore, the signal at the base of U1Q2 appears at the junction of U1Q1 and U2Q1 while any signal at the base of U2Q2 is blocked. For bit rates below 10^4, the situation is reversed. The signal at the junction of U1Q1 and U2Q1 is then transmitted through R17 to voltage comparators U6 through U8.

CR3 generates a stable reference voltage which is adjustable by R29. This voltage is buffered by U5 and divided into three equal increments which are applied to the voltage comparators U6 through U8. In addition, the buffered output of U5 is also inverted by U5, and divided into three equal increments before being applied to U6 through U8. If the signal which is applied through R17 is more positive than the voltage at the junction of R39 and R40, the output of U7 ($+V_2$, pin 11) is a logic 0. Similarly, if the signal is more negative than the voltage at the junction of R35 and R36, the output of U7 ($-V_2$, pin 10) is a logic 0. These digital signals are then transmitted to the BLD002.

4.4 CIRCUIT DESCRIPTION - BLD002-2

See drawing 460-1164-502 in section VI for the schematic of this card.

The incoming bit level information ($\overline{\pm V1}$, $\overline{\pm V2}$, and $\overline{\pm V3}$) from the Bit Level Detector (BLD001-1) is inverted and applied via OR gates U1A, B and D to three D inputs of quad flip-flops U2. The balanced push-pull clock signal 01 and 03 is converted to TTL level by line receiver

U6; the output from U6 clocks the multiple flip-flops U2 and U3 at the end of every bit. When the flip-flops are clocked, the information applied to the D inputs is transferred to the flip-flop outputs. Thus the 4Q output of U2 is a logic 1 if the $\overline{\pm V2}$ input is a logic 0 at the end of the bit. The 4Q output of U2 is then shifted through three stages of hex flip-flop U3; thus it is delayed by three bit periods, which brings it into alignment with the main NRZ-L output in the bit synchronizer. The output at card pin 4, designated NMSB, is therefore a logic 1 for the particular bit in which the matched filter signal exceeds the positive or negative threshold, and a logic 0 where it does not.

Simultaneously, the inverted V3 signal applied to the 3D input of quad flip-flop U2 is clocked to the $\overline{3Q}$ output. Thus, the 3Q output of U2 is a logic 1 if the incoming $\overline{\pm V3}$ signal is a logic 0 at the end of the bit.

The inverted V1 signal applied to the 2D input of quad flip-flop U2 is clocked to the 2Q output. Therefore, the 2Q output of U2 is a logic 1, if the incoming ±V1 signal is a logic 0 at the end of the bit.

The 2Q and $\overline{4Q}$ of U2 are gated through U1C. This output signal is gated with the signals $\overline{3Q}$ and 3Q of U2 through U6 and output at U6 pin 9 to the ID input of U3. This signal is delayed by three bit periods with respect to the input at ID, and is a logic 1 for the particular bit in which the matched filter signal exceeds the positive or negative thresholds, and a logic 0 where it does not. The output at card pin 7 is designated LSB.

U7, Q7 and associated components constitute a -5 volt power supply which supplies the line receiver U6, and the voltage comparators on the BLD001.

SECTION V

MAINTENANCE

5.1 GENERAL

Maintenance procedures as presented in the manual are unchanged by the addition of soft bit decision.

5.2 ADJUSTMENT PROCEDURES

Of the two additional cards, only the BLD001-1 requires adjustment. There are four potentiometers located in this card; to properly adjust them, this procedure must be followed:

a. Set bit rate to 100 Kbps, NRZ-L code, unit in sync.

b. With an oscilloscope observe TP1, matched filter signal. Note signal amplitude. (Approx. 2 volts p-p.)

c. Adjust pot R6 as required so that the signal present at TP1 is balanced about ground.

d. Set bit rate to 1 Kbps, NRZ-L, unit in sync.

e. With an oscilloscope monitoring TP1, adjust pot R45 so that signal present at TP1 is balanced about ground.

f. Continue to monitor TP1 and adjust R48 so that the signal amplitude is the same at 1 Kbps as it is at 100 Kbps.

g. Continue to monitor TP1 and with a second oscilloscope probe monitor TP3. Adjust R29 as required to select threshold levels, normally 90% of the peak signal level at TP1.

SECTION VI

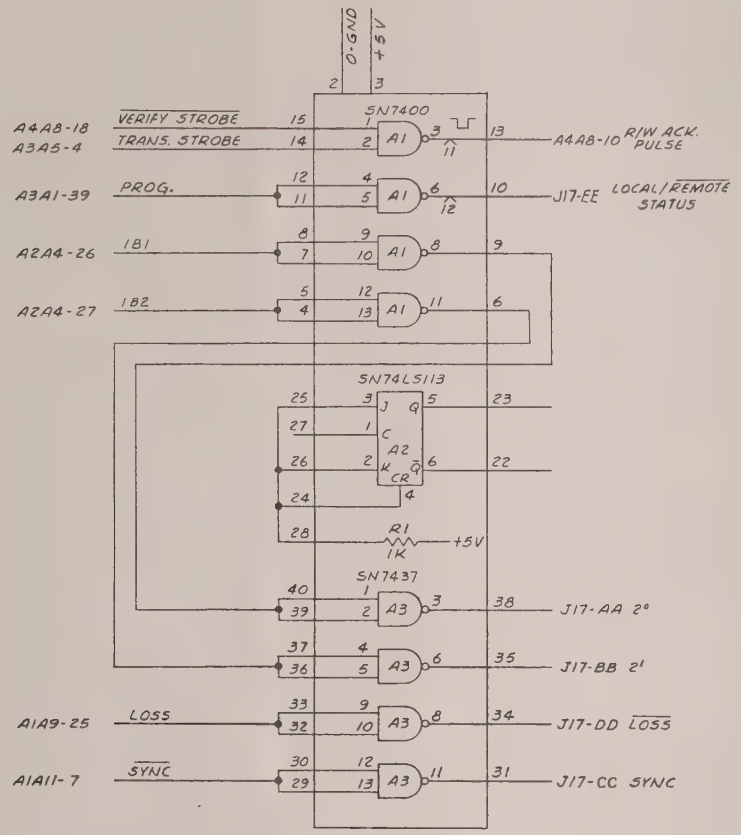
PARTS LISTS AND DRAWINGS

6.1 GENERAL

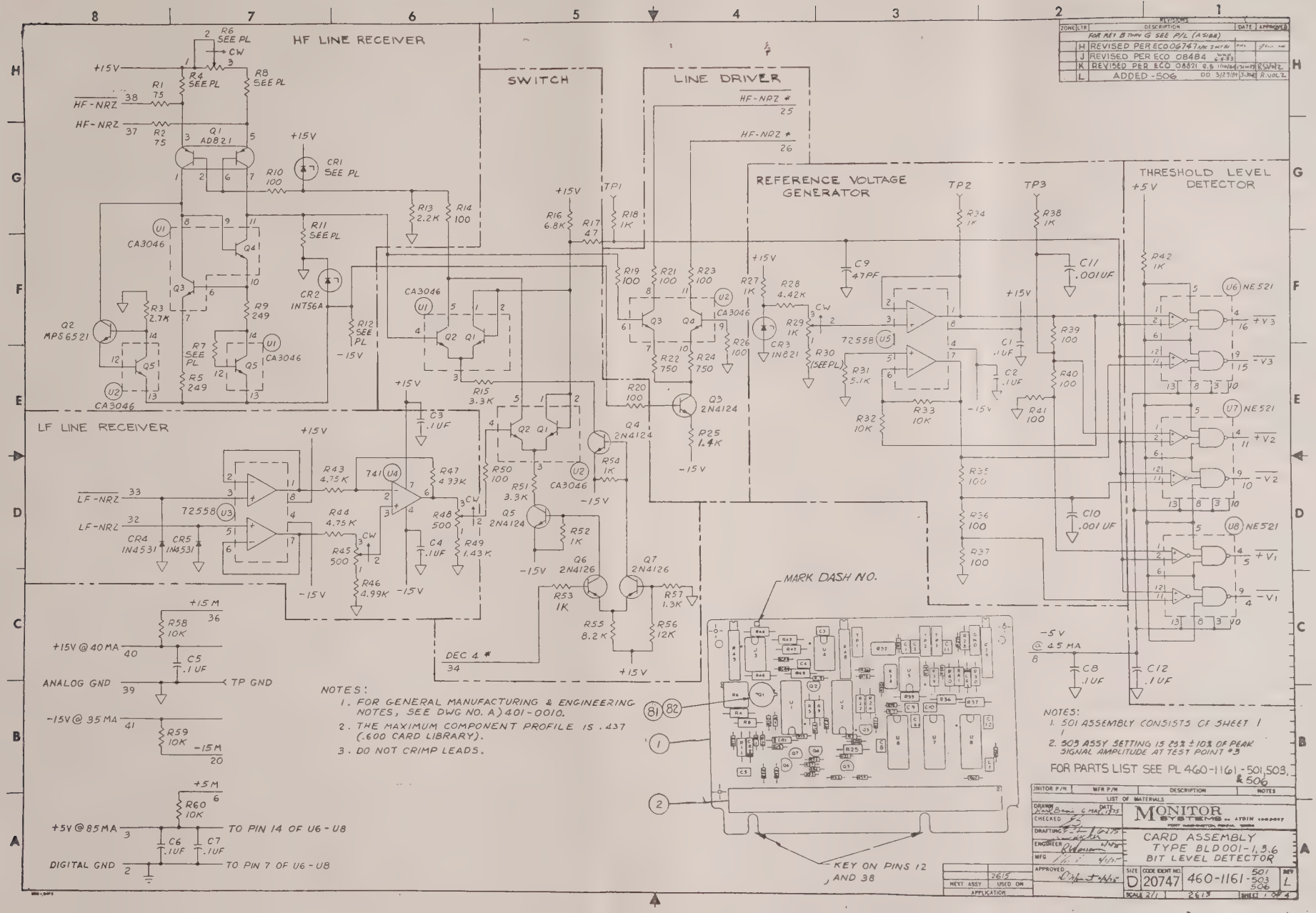
This section contains the parts lists, assembly drawings, schematics, and the delete/add wire list for the circuitry connected with the soft bit decision option. Table C6-1 contains a list of the drawings in this section. For interpretation of the manufacturers' codes used in the parts lists, see table 6-2 in the main body of the manual.

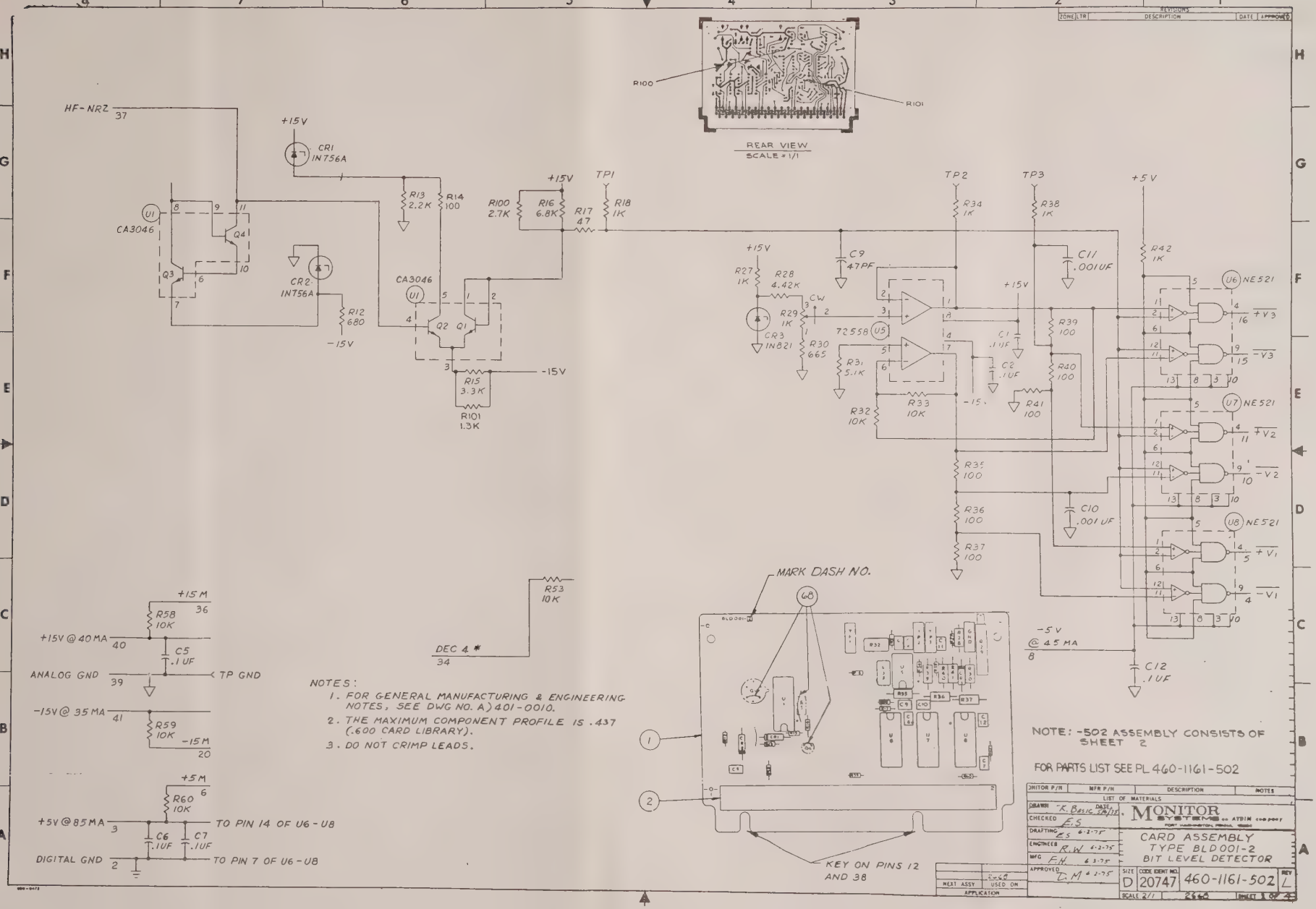
Table C6-1. Parts Lists and Drawings

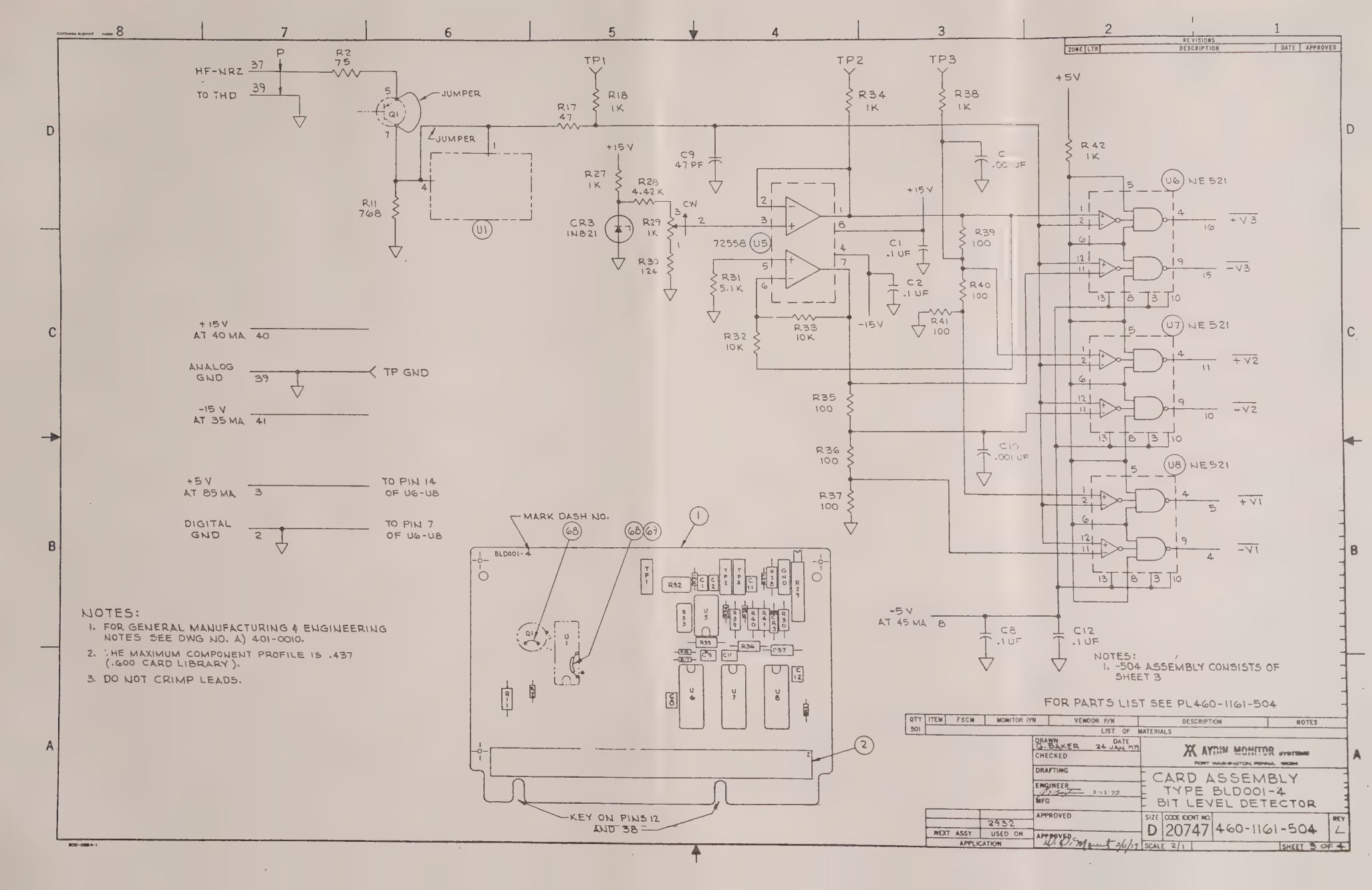
TITLE	NUMBER
PC Card Type BLD001-1, Assembly Drawing, Schematic and Parts List	460-1161-[ ]
PC Card Type BLD002-2, Assembly Drawing, Schematic and Parts List	460-1164-502
Model 335 Mod. for Soft Decision	730-2012



SIZE	CODE IDENT NO.		REV
D	20747	481-0026-30	F
SCALE ~		SHEET 2 OF 2	


HF LINE RECEIVER
SWITCH
LINE DRIVER
REFERENCE VOLTAGE GENERATOR
THRESHOLD LEVEL DETECTOR
LF LINE RECEIVER
MARK DASH NO.
KEY ON PINS 12 AND 38
+15V @ 40 MA
ANALOG GND
TP GND
-15V @ 35 MA
+5V @ 85 MA
TO PIN 14 OF U6-U8
DIGITAL GND
TO PIN 7 OF U6-U8
DEC 4 #
NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES, SEE DWG NO. A)401-0010.
2. THE MAXIMUM COMPONENT PROFILE IS .437 (.600 CARD LIBRARY).
3. DO NOT CRIMP LEADS.
NOTES:
1. 501 ASSEMBLY CONSISTS OF SHEET 1
2. 503 ASSY SETTING IS 25% ± 10% OF PEAK SIGNAL AMPLITUDE AT TEST POINT #3
FOR PARTS LIST SEE PL 460-1161-501,503, & 506
REVISIONS
FOR KEY B THRU G SEE P/L (A5184)
H REVISED PER ECO 06747
J REVISED PER ECO 08484
K REVISED PER ECO 08821
L ADDED -506
MONITOR SYSTEMS
CARD ASSEMBLY
TYPE BLD001-1,3,6
BIT LEVEL DETECTOR
SIZE D
CODE IDENT NO. 20747
460-1161-501 503 506
REV L
SCALE 2/1
2615
SHEET 1 OF 4


HF-NRZ
37
+15V
CR1
IN756A
U1
CA3046
Q4
Q3
CR2
IN756A
-15V
R13
2.2K
R14
100
R12
680
CA3046
U1
Q2
Q1
R15
3.3K
R101
1.3K
-15V
R100
2.7K
R16
6.8K
R17
47
R18
1K
+15V
TP1
R100
R101
REAR VIEW
SCALE = 1/1
TP2
TP3
+5V
R34
1K
R38
1K
R42
1K
C9
47PF
C11
.001UF
+15V
R27
1K
R28
4.42K
CW
R29
1K
R30
665
CR3
IN821
72558
U5
C1
.1UF
C2
.1UF
R31
5.1K
R32
10K
R33
10K
-15V
R39
100
R40
100
R41
100
U6 NE521
U7 NE521
U8 NE521
+V3
-V3
+V2
-V2
+V1
-V1
R35
100
R36
100
R37
100
C10
.001UF
C12
.1UF
-5V
@ 45 MA
8
+15M
36
R58
10K
+15V @ 40 MA
40
C5
.1UF
ANALOG GND
39
TP GND
-15V @ 35 MA
41
R59
10K
-15M
20
+5M
6
R60
10K
+5V @ 85 MA
3
C6
.1UF
C7
.1UF
DIGITAL GND
2
TO PIN 14 OF U6-U8
TO PIN 7 OF U6-U8
R53
10K
DEC 4 *
34
MARK DASH NO.
68
KEY ON PINS 12
AND 38
NOTE: -502 ASSEMBLY CONSISTS OF SHEET 2
FOR PARTS LIST SEE PL 460-1161-502
REVISIONS
ZONE LTR
DESCRIPTION
DATE
APPROVED
JNITOR P/N
MFR P/N
DESCRIPTION
NOTES
LIST OF MATERIALS
DRAWN K. Basic 6/2/75
CHECKED E.S
DRAFTING E.S 6-2-75
ENGINEER R.W 6-2-75
MFG E.H 6-3-75
APPROVED D.M 6-2-75
MONITOR SYSTEMS
CARD ASSEMBLY
TYPE BLD001-2
BIT LEVEL DETECTOR
SIZE D
CODE IDENT NO. 20747
460-1161-502
REV L
SCALE 2/1
SHEET 1 OF 2
NEXT ASSY
USED ON
APPLICATION



NOTES:
1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG NO. A) 401-0010.
2. THE MAXIMUM COMPONENT PROFILE IS .437 (.600 CARD LIBRARY).
3. DO NOT CRIMP LEADS.

NOTES:
1. -504 ASSEMBLY CONSISTS OF SHEET 3

FOR PARTS LIST SEE PL460-1161-504

QTY	ITEM	FSCM	MONITOR P/N	VENDOR P/N	DESCRIPTION	NOTES
501	LIST OF MATERIALS					

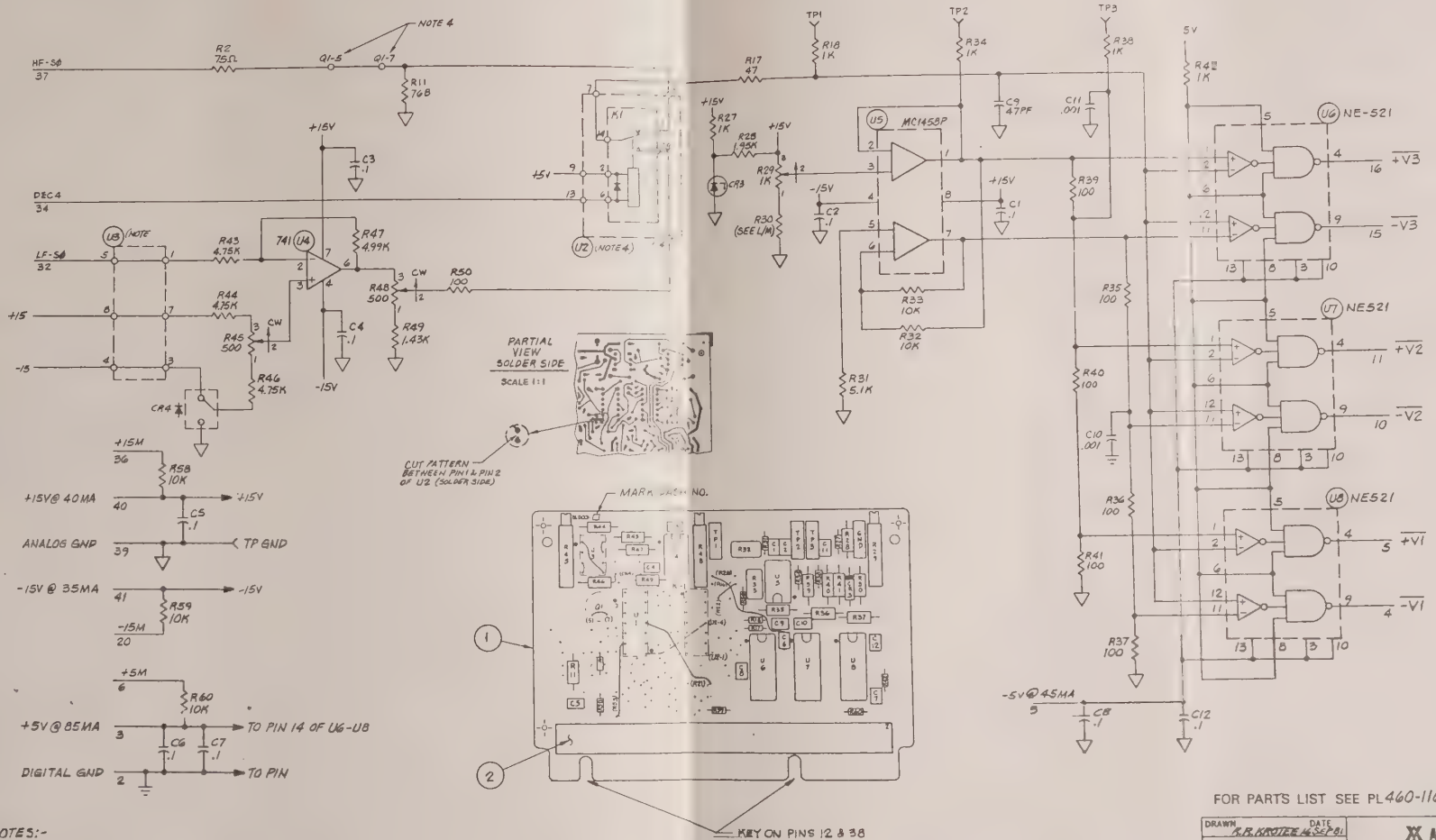
DRAWN G. BAKER DATE 24 JAN 77
CHECKED
DRAFTING
ENGINEER 2-13-77
MFG
APPROVED
APPROVED D. D. Mount 2/11/77

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

CARD ASSEMBLY
TYPE BLD001-4
BIT LEVEL DETECTOR

NEXT ASSY	USED ON
	2932
APPLICATION	

SIZE D | CODE IDENT NO. 20747 | 460-1161-504 | REV L
SCALE 2/1 | SHEET 3 OF 4



FOR PARTS LIST SEE PL460-1161-505

NOTES:-

1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO. A) 401-0010.
2. THE MAXIMUM COMPONENT PROFILE IS .437(.600 CARD LIBRARY)
3. DO NOT CRIMP LEADS.
4. JUMPER LOCATION ONLY (COMPONENT NOT USED)

DRAWN	R.R. KROTEE 16 SEP 81
CHECKED	
DRAFTING	
ENGINEER	
MFG	
APPROVED	
APPROVED	

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

CARD ASSEMBLY
TYPE BLD001-5
BIT LEVEL DETECTOR

NEXT ASSY	USED ON
APPLICATION	

SIZE	CODE IDENT NO.		REV
D	20747	460-1161-505	L

SCALE 1/1 SHEET 4 OF 4

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						R42
						R50
						R53
						R54
2	036	100-215-7500	RN55D7500F	G	RES 750 OHMS 1/8W 1%	R22
						R24
1	037	100-017-272	RC05GF272J	C	RES 2.7K 1/8W 5%	R3
1	038	100-215-4421	RN55D4421F	G	RES 4.42K 1/8W 1%	R28
1	039	101-127-10C	8417-1000	B	POT 1K .75W 10%	R29
1	040	100-215-6650	RN55D6650F	G	RES 665 OHMS 1/8W 1%	R30
1	041	100-017-512	RC05GF512J	C	RES 5.1K 1/8W 5%	R31
2	042	100-444-003	V53C1-10K-.1%	D	RES 10K .3W .1%	R32
						R33
6	043	100-215-1000	RN55D1000F	G	RES 100 OHMS 1/8W 1%	R35
						R36
						R37
						R39
						R40
						R41
2	045	100-215-4991	RN55D4991F	G	RES 4.99K 1/8W 1%	R46
						R47
2	047	101-127-501	8417-500	B	POT 500 .75W 10%	R45
						R48
1	048	100-215-1431	RN55D1431F	G	RES 1.43K 1/8W 1%	R49
1	049	100-017-822	RC05GF822J	C	RES 8.2K 1/8W 5%	R55
1	050	100-017-123	RC05GF123J	C	RES 12K 1/8W 5%	R56
1	051	100-017-132	RC05GF132J	C	RES 1.3K 1/8W 5%	R57
3	052	100-017-103	RC05GF103J	C	RES 10K 1/8W 5%	R58
						R59
						R60
2	055	139-209-002	CA3046	D	IC	U1
						U2
2	056	139-163-002	MC1458P	J	IC OP AMP 8 PIN TO-99	U3
						U5
1	057	139-174-001	ICL741CPA	J	IC OP AMP 8 PIN DIP	U4
3	058	139-232-001	NE521A	A	IC VOLT COMP 14 PIN	U6
						U7
						U8
1	061	121-202-009	SPCJ-200-01	K	TEST POINT PC WHT	TP GND
3	062	121-202-005	SPCJ-200-05	K	TEST POINT PC GRN	TP1
						TP2
						TP3
2	073	100-215-4751	RN55D4751F	G	RES 4.75K 1/8W 1%	R43
						R44
1	081	131-049-001	RC-TO18100-2A	A	PAD TRANS TO18 6PIN	
1	082	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 01197 R.M.		1-6-75	
C	REVISED PER ECO 01485	2 THRU 7	7-23-75	
D	REVISED PER ECO 01651	2,3,7	10/19/76	
E	REVISED PER ECO 03392 JSG		7-6-78	J Hinkle
F	REVISED PER ECO 03883 BAKER 1-29-79		2-13-79	
G	REVISED PER ECO #04579 JSG		11-7-79	J Hinkle
H	REVISED PER ECO 06747 RAK 21 SEP 81		10-2-81	
J	REVISED PER ECO 08484 WKH 6-7-83			

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—	—	—	—	—	—														

AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

TITLE PARTS LIST
TYPE BLD001-2
BIT LEVEL DETECTOR

CODE IDENT 20747
CONTRACT NO.

DRAWN	Karl Basie	19 MAY 1975	ENGINEER	R Wasson	6/2/75	DWG NO. PL460-1161-502	REV J
CHECKED	ES		APPROVED	O'Mant	6/2/75		
DRAFTING	E Stucki	6-2-75				SHEET 1 OF 2	

800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		460-1161-502		J	PARENT BLD001-2	
1	001	400-1345		B	BOARD P.W. MONI 1	
2	005	102-419-102	8101A100651102M	P	CAP 1000PF 100V 20%	C10
						C11
1	006	102-417-470	8121100G0G0470K	G	CAP 47PF 100V 10%	CG
2	007	104-056-115	1N756A	P	DIODE ZENER CASE 51	CR1
						CR2
1	008	104-308-006	IN821A	D	DILDE ZENER SILICON	CR3
6	010	102-419-104	CK06BX104M	P	CAP .1UF 100V 20%	C1
						C2
						C5
						C6
						C7
1	016	100-017-332	RC05GF332J	C	RES 3.3K 1/8W 5%	C12
1	029	100-017-681	RC05GF681J	C	RES 680 OHMS 1/8W 5%	R15
1	030	100-017-222	RC05GF222J	C	RES 2.2K 1/8W 5%	R12
1	031	100-017-682	RC05GF682J	C	RES 6.8 1/8W 5%	R13
1	032	100-017-470	RC05GF470J	C	RES 47 OHMS 1/8W 5%	R16
1	038	100-215-4421	RN55D4421F	G	RES 4.42K 1/8W 1%	R17
1	039	101-127-102	8417-1000	B	POT 1K .75W 10%	R28
1	040	100-215-6650	RN55D6650F		RES 665 1/8W 1%	R29
1	041	100-017-512	RC05GF512J	C	RES 5.1K 1/8W 5%	R30
2	042	100-444-003	V53C1-10K-.1%		RES 10K .3W .1%	R31
						R3?
6	043	100-215-1000	RN55D1000F	G	RES 100 OHMS 1/8W 1%	R
						R3
						R36
						R37
						R39
						R40
						R41
1	053	100-017-101	RC05GF101J	C	RES 100 OHMS 1/8W 5%	R14
5	054	100-017-102	RC05GF102J	C	RES 1K 1/8W 5%	R18
						R27
						R34
						R38
						R42
3	058	139-232-001	NE521A	A	IC VOLT COMP 14 PIN	U6
						U7
						U8
1	059	139-209-002	CA3046	D	IC	U1
1	060	139-163-002	MC1458P	J	IC OP AMP 8 PIN TO-99	U5
1	061	121-202-009	SPCJ-200-01	K	TEST POINT PC WHT	TP GND
3	062	121-202-005	SPCJ-200-05	K	TEST POINT PC GRN	TP1
						TP2
						TP3
3	063	100-017-103	RC05GF103J	C	RES 10K 1/8W 5%	R53
						R59
						R60
1	064	100-017-272	RC05GF272J	C	RES 2.7K 1/8W 5%	R100
1	065	100-017-132	RC05GF132J	C	RES 1.3K 1/8W 5%	R1
1	068	113-001-006	299/1	C	WIRE BUS 26 AWG	
1	081	131-049-001	RC-TO18100-2A	A	PAD TRANS TO18 6PIN	
1	082	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 01197 [illegible]		1-6-75	[illegible]
C	REVISED PER ECO 01485	2 THRU 7	7-28-76	[illegible]
D	REVISED PER ECO 01651	2,3,7	10/18/76	[illegible]
E	REVISED PER ECO 03392 JSG		7-6-78	F Hinkle
F	REVISED PER ECO 03883 BAKER 1-29-79		2-13-79	[illegible]
G	REVISED PER ECO #04579 JSG		11-7-79	F Hinkle
H	REVISED PER ECO 06747 RAK 21 SEP 81		10-2-81	[illegible]
J	REVISED PER ECO 08484 WKH 6-7-83		[illegible]	[illegible]
K	REVISED PER ECO 08821 R.B. 1/10/84		17 Jan 84	RS Volz
L	REVISED PER ECO 08955 R.P.K. 2-20-84		22 Feb 84	RS Volz
M	REVISED PER ECO 09126		6 Apr 84	RS Volz

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION																							

AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

TITLE PARTS LIST
TYPE BLD001-3
BIT LEVEL DETECTOR

CODE IDENT 20747
CONTRACT NO. —

DRAWN	Karl Basic	19 MAY 1975	ENGINEER	[illegible]	6/2/75	DWG NO. PL460-1161-503	REV M
CHECKED	[illegible]		APPROVED	[illegible]	6/2/75		
DRAFTING	[illegible]	6-2-75				SHEET 1 OF 3	

800-0066

*** SINGLE LEVEL BILL - BY ITEM ***

SUB.MFG.ITEM 16:13:36 30 MAR 1984 PAGE

ASSEMBLY: 460-1161-503 REV: M

QTA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		460-1161-503		M	PRINT BLD001-3	
1	001	400-1345		B	BOARD P.W. MONI 1	
1	002	108-023-040	7022-040-000001	D	CONN FING BLOC 40 POS	
9	004	102-419-104	CK06BX104M	P	CAP .1UF 100V 20%	C1
						C2
						C3
						C4
						C5
						C6
						C7
						C8
2	005	102-419-102	8101A100651102M	P	CAP 1000PF 100V 20%	C12
						C10
1	006	102-417-470	8121100GOGO470K	G	CAP 47PF 100V 10%	C11
2	007	104-056-115	1N756A	P	DIODE ZENER CASE 51	C9
						CR1
1	008	104-308-006	1N821A	D	DIODE ZENER SILICON	CR2
2	009	104-503-014	1N4531	G	DIODE SIG MINIATURE	CR3
						CR4
1	012	103-647-008	MPS351	J	TRANS DUAL PNP TO-52	CR5
1	013	103-416-006	MPS6521	B	TRANS SIL NPN TO-92	Q1
3	014	103-408-001	2N4124	C	TRANS SIL NPN TO-92	Q2
						Q3
						Q4
2	015	103-304-001	2N4126	D	TRANS SIL PNP TO-92	Q5
						Q6
2	018	100-017-750	RC05GF750J	C	RES 75 OHMS 1/8W 5%	Q7
						R1
2	019	100-017-332	RC05GF332J	C	RES 3.3K 1/8W 5%	R2
						R15
2	020	100-215-1401	RN55D1401F	G	RES 1.4K 1/8W 1%	R51
						R4
2	021	100-215-2490	RN55D2490F	G	RES 249 OHMS 1/8W 1%	R25
						R5
1	022	101-101-002	3290P-1-201	H	POT 200 1W 5%	R9
1	023	100-017-201	RC05GF201J	C	RES 200 OHMS 1/8W 5%	R6
1	024	100-215-1301	RN55D1301F	G	RES 1.3K 1/8W 1%	R7
8	025	100-017-101	RC05GF101J	C	RES 100 OHMS 1/8W 5%	R8
						R10
						R14
						R19
						R20
						R21
						R23
						R26
						R50
1	028	100-215-7680	RN55D7680F	G	RES 768 OHMS 1/8W 1%	R11
1	029	100-017-431	RC05GF431J	C	RES 430 OHMS 1/8W 5%	R12
1	030	100-017-222	RC05GF222J	C	RES 2.2K 1/8W 5%	R13
1	031	100-017-682	RC05GF682J	C	RES 6.8 1/8W 5%	R
1	032	100-017-470	RC05GF470J	C	RES 47 OHMS 1/8W 5%	R1
8	033	100-017-102	RC05GF102J	C	RES 1K 1/8W 5%	R1
						R2
						R29
						R34

ASSEMBLY: 460-1161-503 REV: M

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
8	033	100-017-102	CONTINUATION			R38 R42 R53 R54
2	036	100-215-7500	RN55D7500F	G	RES 750 OHMS 1/8W 1%	R22 R24
1	037	100-017-272	RC05GF272J	C	RES 2.7K 1/8W 5%	R3
1	038	100-215-4421	RN55D4421F	G	RES 4.42K 1/8W 1%	R28
1	039	101-127-102	8417-1000	B	POT 1K .75W 10%	R29
1	041	100-017-512	RC05GF512J	C	RES 5.1K 1/8W 5%	R31
2	042	100-444-003	V53C1-10K-.1%	D	RES 10K .3W .1%	R32 R33
7	043	100-215-1000	RN55D1000F	G	RES 100 OHMS 1/8W 1%	R30 R35 R36 R37 R39 R40 R41
2	045	100-215-4991	RN55D4991F	G	RES 4.99K 1/8W 1%	R46 R47
2	047	101-127-501	8417-500	B	POT 500 .75W 10%	R45 R48
1	048	100-215-1431	RN55D1431F	G	RES 1.43K 1/8W 1%	R49
1	049	100-017-822	RC05GF822J	C	RES 8.2K 1/8W 5%	R55
1	050	100-017-123	RC05GF123J	C	RES 12K 1/8W 5%	R56
1	051	100-017-132	RC05GF132J	C	RES 1.3K 1/8W 5%	R57
3	052	100-017-103	RC05GF103J	C	RES 10K 1/8W 5%	R58 R59 R60
2	055	139-209-002	CA3046	D	IC	U1 U2
2	056	139-163-002	MC1458P	J	IC OP AMP 8 PIN TO-99	U3 U5
1	057	139-174-001	ICL741CPA	J	IC OP AMP 8 PIN DIP	U4
3	058	139-232-001	NE521A	A	IC VOLT COMP 14 PIN	U6 U7 U8
1	061	121-202-009	SPCJ-200-01	K	TEST POINT PC WHT	TP GND
3	062	121-202-005	SPCJ-200-05	K	TEST POINT PC GRN	TP1 TP2 TP3
2	073	100-215-4751	RN55D4751F	G	RES 4.75K 1/8W 1%	R43 R44
1	081	131-049-001	RC-TO18100-2A	A	PAD TRANS TO18 6PIN	
1	082	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 01197 [illegible]		1-6-75	[illegible]
C	REVISED PER ECO 01485	2 THRU 7	7-28-76	[illegible]
D	REVISED PER ECO 01651	2,3,7	10/18/76	[illegible]
E	REVISED PER ECO 03392 JSG		7-6-78	J Hinkle
F	REVISED PER ECO 03883 BAKER 1-29-79		2-13-79	[illegible]
G	REVISED PER ECO #04579 JSG		11-7-79	J Hinkle
H	REVISED PER ECO 06747 RAK 21 SEP 81		10-2-81	[illegible]
J	REVISED PER ECO 08484 WKH 6-7-83		[illegible]	W.K. Hinkle

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—	—	—	—	—	—														

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
TYPE BLD001-4
BIT LEVEL DETECTOR

CODE IDENT 20747
CONTRACT NO.

DRAWN	Karl Basse	19 MAY 1975	ENGINEER	[illegible]	6/2/75	DWG NO. PL460-1161-504	REV J
CHECKED	[illegible]		APPROVED	[illegible]	6/2/75		
DRAFTING	[illegible]	6-2-75				SHEET 1 OF 2	

800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		460-1161-504		J	PARENT BLD001-4	
1	001	400-1345		B	BOARD P.W. MONI 1	
1	002	108-203-040	7033-040-000001	D	CONN FING BLOC 40 POS	
4	003	102-419-104	CK06BX104M	P	CAP .1UF 100V 20%	C1
						C2
						C8
2	005	102-419-102	8101A10065102M	P	CAP 1000PF 100V 20%	C12
						C10
1	006	102-417-470	8121100G0G0470K	G	CAP 47PF 100V 10%	C11
1	008	104-308-006	IN821A	D	DILDE ZENER SILICON	C9
1	017	100-017-750	RC05GF750J	C	RES 75 OHMS 1/8W 5%	CR3
1	028	100-215-7680	RN55D7680F		RES 768 1/8W 1%	R2
1	032	100-017-470	RC05GF470J	C	RES 47 OHMS 1/8W 5%	R11
1	038	100-215-4421	RN55D4421F	G	RES 4.42K 1/8W 1%	R17
1	039	101-127-102	8417-1000	B	POT 1K .75W 10%	R28
1	041	100-017-512	RC05GF512J	C	RES 5.1K 1/8W 5%	R29
2	042	100-444-003	V53C1-10K-.1%		RES 10K .3W .1%	R31
						R32
6	043	100-215-1000	RN55D1000F	G	RES 100 OHMS 1/8W 1%	R33
						R35
						R36
						R37
						R39
						R40
						R4
5	054	100-017-102	RC05GF102J	C	RES 1K 1/8W 5%	R1
						R27
						R34
						R38
						R42
3	058	139-232-001	NE521A	A	IC VOLT COMP 14 PIN	U6
						U7
						U8
1	060	139-163-002	MC1458P	J	IC OP AMP 8 PIN TO-99	U5
1	061	121-202-009	SPCJ-200-01	K	TEST POINT PC WHT	TP GND
3	062	121-202-005	SPCJ-200-05	K	TEST POINT PC GRN	TP1
						TP2
						TP3
1	068	113-001-006	299/1	C	WIRE BUS 26 AWG	
1	069	114-001-006	SIZE 26 WHITE	J	TUBING TEF 26 AWG WHT	
1	074	100-215-1240	RN55D1240F	G	RES 124 OHMS 1/8W 1%	R30
1	081	131-049-001	RC-TO18100-2A	A	PAD TRANS TO18 6PIN	
1	082	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 01197 R.V.D.		1-6-75	
C	REVISED PER ECO 01485	2 THRU 7	7-28-76	
D	REVISED PER ECO 01651	2,3,7	10/19/76	
E	REVISED PER ECO 03392 JSG		7-6-78	J Heisler
F	REVISED PER ECO 03883 BAKER 1-29-79		2-13-79	
G	REVISED PER ECO #04579 JSG		11-7-79	J Heisler
H	REVISED PER ECO 06747 RAK 21 SEP 81		10-2-81	
J	REVISED PER ECO 08484 WKH 6-7-83			

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—	—	—	—	—	—	—														

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA 19034

TITLE PARTS LIST
TYPE BLD001-5
BIT LEVEL DETECTOR

CODE IDENT 20747
CONTRACT NO.

DRAWN	Karl Basie	19 MAY 1975	ENGINEER	R Swanson	6/2/75	DWG NO. PL460-1161-505	REV J
CHECKED	ES		APPROVED	O Mount	6/2/75		
DRAFTING	E Stuckey	6-2-75				SHEET 1 OF 3	

800-0066

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
		460-1161-505		J	PARENT BLD001-5	
1	001	400-1345		B	BOARD P.W. MONI 1	
1	002	108-203-040	7022-040-000001	D	CONN FING BLOC 40 POS	
9	004	102-419-104	CK06BX104M	P	CAP .1UF 100V 20%	C1- C2 C3 C4 C5 C6 C7 C8
2	005	102-419-102	8101A10065110 2M	P	CAP 1000PF 100V 20%	C12 C10
1	006	102-417-470	8121100G0G0470K	G	CAP 47PF 100V 10%	C11 C9
1	008	104-308-006	IN821A	D	DILDE ZENER SILICON	CR3
1	017	100-017-750	RC05GF750J	C	RES 75 OHMS 1/8W 5%	R2
1	028	100-215-7680	RN55D7680F		RES 768 1/8W 1%	R11
1	032	100-017-470	RC05GF470J	C	RES 47 OHMS 1/8W 5%	R17
1	039	101-127-102	8417-1000	B	POT 1K .75W 10%	R29
1	040	100-215-6650	RN55D6650F		RES 665 1/8W 1%	R30
1	041	100-017-512	RC05GF512J	C	RES 5.1K 1/8W 5%	R31
2	042	100-444-003	V53C1-10K-.1%		RES 10K .3W .1%	R32 R33
6	043	100-215-1000	RN55D1000F	G	RES 100 OHMS 1/8W 1%	R[illegible] R. R37 R39 R40 R41
2	047	101-127-501	8417-500	B	POT 500 .75W 10%	R45 R48
1	048	100-215-1431	RN55D1431F	G	RES 1.43K 1/8W 1%	R49
3	052	100-017-103	RC05GF103J	C	RES 10K 1/8W 5%	R58 R59 R60
5	054	100-017-102	RC05GF102J	C	RES 1K 1/8W 5%	R18 R27 R34 R38 R42
1	057	139-174-001	ICL741CPA	J	IC OP AMP 8 PIN DIP	U4.
3	058	139-232-001	NE521A	A	IC VOLT COMP 14 PIN	U6 U7 U8
1	061	121-202-009	SPCJ-200-01	K	TEST POINT PC WHT	
3	062	121-202-005	SPCJ-200-05	K	TEST POINT PC GRN	TP1 TP2 TP3
1	066	100-017-101	RC05GF101J	C	RES 100 OHMS 1/8W 5%	R50
0	067	120-101-001	SN63BS	B	SOLDER 63/37 BAR	
0	068	113-001-006	299/1	C	WIRE BUS 26 AWG	
0	069	114-001-006	SIZE 26 WHITE	J	TUBING TEF 26 AWG WHT	
3	075	100-215-4751	RN55D4751F	G	RES 4.75K 1/8W 1%	[illegible] R44

QPA	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF.DES
						R4C
1	076	100-215-4991	RN55D4991F	G	RES 4.99K 1/8W 1%	R47
1	077	106-033-104	106-027-001	D	RELY SPDT 5V 40MA	K1
1	078	139-163-002	MC1458P	J	IC OP AMP 8 PIN TO-99	U5
1	081	131-049-001	RC-TO18100-2A	A	PAD TRANS TO18 8PIN	
1	082	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	

REVISIONS				
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—	—	—																				

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

TITLE PARTS LIST
TYPE BLDØØ1-6
BIT LEVEL DETECTOR

CODE IDENT 20747
CONTRACT NO. 1337-91

DRAWN	D.B.DIXON	3-29-84	ENGINEER	RSV0/2	3-29-84	DWG NO. PL A60-1161-506	REV A
CHECKED	ES		APPROVED	RSV0/2	3-29-84		
DRAFTING	E.S.Tucker					SHEET 1 OF 3	

800-0066

*** SINGLE LEVEL BILL BY [illegible]

[illegible] 28 MAR 1984

ASSEMBLY: 460-1161-506 REV: A

QTY	ITEM	MON TOR	MFG PART NBR	REV	DESCRIPTION	REF. DES
		60	[illegible] 506	A	PARENT BOARD ASSY BL D001	
1	001	420 [illegible]		B	BOARD [illegible]	
1	002	108 [illegible]	7022-040-000001	D	CONN [illegible] DLCC 40 POS	
9	004	102-419-104	CK06BX104Y	P	CAP [illegible] 100V 20%	C1 C2 C3 C4 C5 C6 C7 C8
2	005	102-419-102	8101A100651102M	P	CAP 1000PF 100V 20%	C12 C10 C11
1	006	102-417-470	8121100GDGD470K	G	CAP 47PF 100V 10%	C9
1	007	104-056-115	1N753A	P	DIODE ZENER CASE 51	CR2
1	008	104-308-206	1N821A	D	DIODE ZENER SILICON	CR3
2	009	104-503-014	1N4531	G	DIODE SIG MINIATURE	CR4 CR5
1	010	104-056-104	1N757A	P	DIODE ZENER CASE 51	CR1
1	012	103-647-008	MPS351	J	TRANS DUAL PNP TO-52	Q1
1	013	103-416-006	MPS6521	B	TRANS SIL NPN TO-92	Q2
3	014	103-408-001	2N4124	C	TRANS SIL NPN TO-92	Q3
2	015	103-304-001	2N4126	D	TRANS SIL PNP TO-92	Q6 Q7
2	018	100-017-750	RC05GF750J	C	RES 75 OHMS 1/8W 5%	R1 R2
2	019	100-017-332	RC05GF332J	C	RES 3.3K 1/8W 5%	R15 R51
1	020	100-215-1401	RN55D1401F	G	RES 1.4K 1/8W 1%	R25
2	021	100-215-2490	RN55D2490F	G	RES 249 OHMS 1/8W 1%	R5 R9
1	022	101-101-007	3280P-1-203	H	POT 20K 1W 5%	R6
1	023	100-017-121	RC05GF121J	C	RES 120 OHMS 1/8W 5%	R7
1	024	100-215-8871	RN55D8871F	G	RES 8.87K 1/8W 1%	R8
8	025	100-017-101	RC05GF101J	C	RES 100 OHMS 1/8W 5%	R10 R14 R19 R20 R21 R23 R26 R50
1	026	100-215-1402	RN55D1402F	G	RES 14K 1/8W 1%	R4
1	028	100-215-4990	RN55D4990F	G	RES 499 OHMS 1/8W 1%	R11
1	029	100-017-361	RC05GF361J	C	RES 360 OHMS 1/8W 5%	R12
1	030	100-017-222	RC05GF222J	C	RES 2.2K 1/8W 5%	R13
1	031	100-017-682	RC05GF682J	C	RES 6.8 1/8W 5%	5
1	032	100-017-470	RC05GF470J	C	RES 47 OHMS 1/8W 5%	R17
8	033	100-017-102	RC05GF102J	C	RES 1K 1/8W 5%	R34

PL 460-1161-506A SHEET 2

QTY	ITEM	VENDOR	VENDOR PART NO	REV	DESCRIPTION	REF. DES
8	233	100-017-102			COMBINATION	R38 R42 R52 R53 R54 R22 R24
3	236	100-215-7500	RN55D7500F	G	RES 750 OHMS 1/8W 1%	R3
1	237	100-017-272	RC05GF272J	C	RES 2.7K 1/8W 5%	R28
1	238	100-215-4421	RN55D4421F	G	RES 4.42K 1/8W 1%	R29
1	239	101-127-102	8417-1000	B	POT 1K .75W 10%	R30
1	240	100-215-6650	RN55D6650F	G	RES 665 OHMS 1/8W 1%	R31
1	241	100-017-512	RC05GF512J	C	RES 5.1K 1/8W 5%	R32
2	242	100-444-003	V53D1-10K-.1%	D	RES 10K .3W .1%	R33
6	243	100-215-1000	RN55D1000F	G	RES 100 OHMS 1/8W 1%	R35 R36 R37 R39 R40 R41
2	245	100-215-4991	RN55D4991F	G	RES 4.99K 1/8W 1%	R46
2	247	101-127-501	8417-500	B	POT 500 .75W 10%	R47 R45
1	248	100-215-1431	RN55D1431F	G	RES 1.43K 1/8W 1%	R48
1	249	100-017-822	RC05GF822J	C	RES 8.2K 1/8W 5%	R49
1	250	100-017-123	RC05GF123J	C	RES 12K 1/8W 5%	R55
1	251	100-017-132	RC05GF132J	C	RES 1.3K 1/8W 5%	R56
3	252	100-017-103	RC05GF103J	C	RES 10K 1/8W 5%	R57 R58 R59 R60
2	255	139-209-002	CA3046	D	IC	U1
2	256	139-163-002	MC1458P	J	IC DP AMP 8 PIN TO-99	U2 U3
1	257	139-174-001	ICL741CPA	J	IC OP AMP 8 PIN DIP	U5 U4
3	258	139-232-001	NE521A	A	IC VOLT COMP 14 PIN	U6 U7 U8
1	261	121-202-009	SPCJ-200-01	K	TEST POINT PC WHT	TP GND
3	262	121-202-005	SPCJ-200-05	K	TEST POINT PC GRN	TP1 TP2 TP3
2	273	100-215-4751	RN55D4751F	G	RES 4.75K 1/8W 1%	R43 R44
1	281	131-049-201	RC-TO18100-2A	A	PAD TRANS TO18 8PIN	
1	282	131-017-001	10383 DAP	C	PAD IC TO5 8PIN	

PL 460-1161-506A
SHEET 3

REVISIONS					
REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 01197 9/7/71.		1-6-75	[illegible]
C	REVISED PER ECO 01485	2 THRU 7	7-28-76	[illegible]
D	REVISED PER ECO 01651	2,3,7	10/18/76	[illegible]
E	REVISED PER ECO 03392 JSG		7-6-78	J Heinlein
F	REVISED PER ECO 03883 BAKER 1-29-79		2-13-79	[illegible]
G	REVISED PER ECO 04579 JSG		11-7-79	J Heinlein
H	REVISED PER ECO 06747 RAK 21 SEP 81		10-2-81	[illegible]
J	REVISED PER ECO 08484 WKH 6-7-83		8 JUNE 83	W.R. WRIGHT
K	REVISED PER ECO 08821 R.B. 1/10/84		17 JAN 84	RS Vol 2
L	REVISED PER ECO 08956 R.P.K. 2-20-84		21 Feb 84	RS Vol 2

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	—																						

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA 19034

TITLE PARTS LIST
TYPE BLD001-1
BIT LEVEL DETECTOR

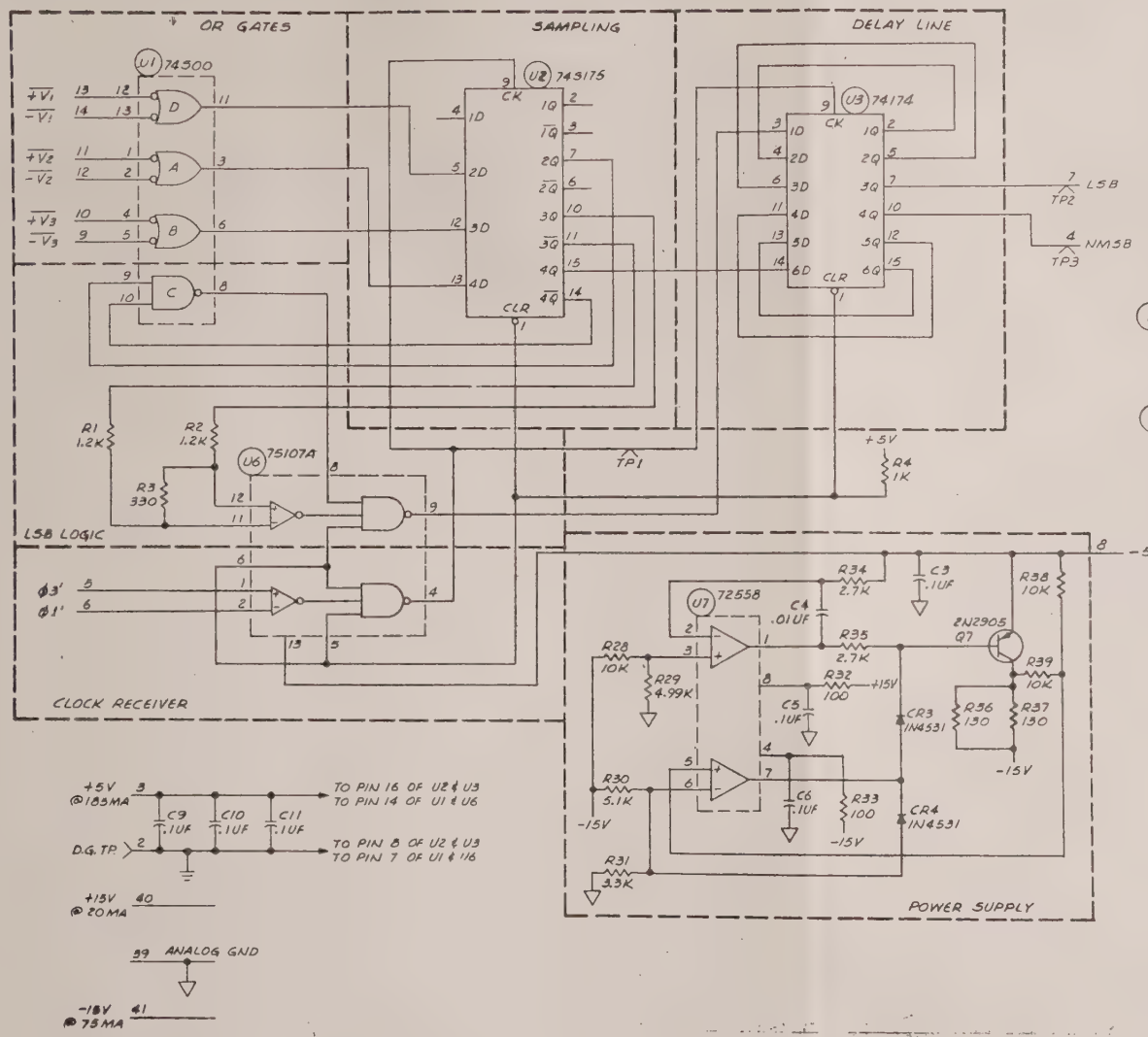
CODE IDENT 20747
CONTRACT NO.

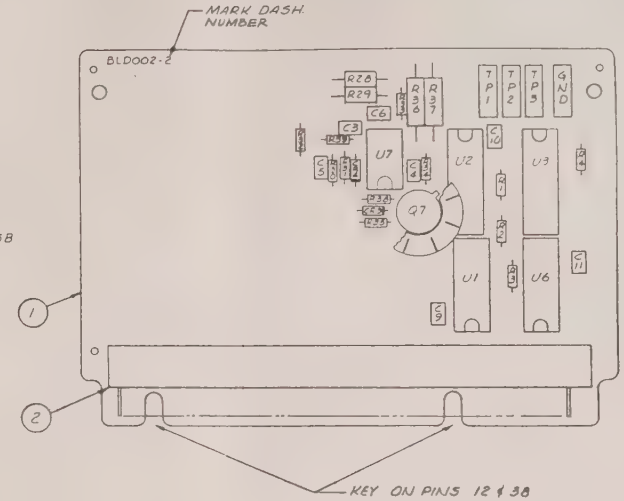
DRAWN	Karl Basie	19 MAY 1975	ENGINEER	R Watson	6/2/75	DWG NO. PL460-1161-501	REV L
CHECKED	ES		APPROVED	O'Mant	6/2/75		
DRAFTING	E Stuckey	6-2-75				SHEET 1 OF 3	

800-0066

QTY	ITEM	MONITOR #	MFG PART NBR	REV	DESCRIPTION	REF. DES
		460-1161-501		L	PARENT BLD001-1	
1	001	400-1345		B	BOARD P.W. MONI 1	
1	002	108-203-040	7022-040 000001	D	CONN FING BLOC 40 POS	
9	004	102-419-104	CK06BX104M	P	CAP .1UF 100V 20%	C1 C2 C3 C4 C5 C6 C7 C8
2	005	102-419-102	8101A10065102M	P	CAP 1000PF 100V 20%	C12 C10
1	006	102-417-470	8121100G0G0470K	G	CAP 47PF 100V 10%	C11
2	007	104-056-115	1N756A	P	DIODE ZENER CASE 51	C9 CR1
1	008	104-308-006	1N821A	D	DILDE ZENER SILICON	CR2
2	009	104-503-014	1N4531	G	DIODE SIG MINIATURE	CR3 CR4
1	012	103-647-008	MPS351	J	TRANS DUAL PNP TO-52	CR5 Q1
1	013	103-416-006	MPS6521	B	TRANS SIL NPN TO-92	Q2
3	014	103-408-001	2N4124	C	TRANS SIL NPN TO-92	Q3 Q4 Q5
2	015	103-304-001	2N4126	D	TRANS SIL PNP TO-92	Q6
2	018	100-017-750	RC05GF750J	C	RES 75 OHMS 1/8W 5%	Q7 R1
2	019	100-017-332	RC05GF332J	C	RES 3.3K 1/8W 5%	R2 R15
2	020	100-215-1401	RN55D1401F	G	RES 1.4K 1/8W 1%	R51 R4
2	021	100-215-2490	RN55D2490F	G	RES 249 OHMS 1/8W 1%	R25 R5
1	022	101-101-002	3290P-1-201	H	POT 200 1W 5%	R9
1	023	100-017-201	RC05GF201J	C	RES 200 OHMS 1/8W 5%	R6
1	024	100-215-1301	RN55D1301F	G	RES 1.3K 1/8W 1%	R7 R8
8	025	100-017-101	RC05GF101J	C	RES 100 OHMS 1/8W 5%	R10 R14 R19 R20 R21 R23 R26 R50
1	028	100-215-7680	RN55D7680F	G	RES 768 OHMS 1/8W 1%	R11
1	029	100-017-431	RC05GF431J	C	RES 430 OHMS 1/8W 5%	R12
1	030	100-017-222	RC05GF222J	C	RES 2.2K 1/8W 5%	R13
1	031	100-017-682	RC05GF682J	C	RES 6.8 1/8W 5%	R
1	032	100-017-470	RC05GF470J	C	RES 47 OHMS 1/8W 5%	R17
8	033	100-017-102	RC05GF102J	C	RES 1K 1/8W 5%	R R34 R38

PL460-1161-501L SHT. 2





NOTES:

1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES, SEE DWG. Nº A) 401-0010.
2. THE MAXIMUM COMPONENT PROFILE IS .437 (.600 CARD LIBRARY).
3. DO NOT CRIMP LEADS.

FOR PARTS LIST SEE PL460-1164-D

DRAWN J. GOODOLF 5-29-81	AYDIN MONITOR
CHECKED ES	CARD ASSEMBLY BIT LEVEL DIGITIZER BLD002-2
DRAFTING 5-29-81	
ENGINEER R. VOLZ	
APPROVED 5-29-81 R. J. MARSCHAFF	SIZE D · CODE IDENT NO. 20747 · 460-1164-502 · REV D

REVISIONS

REV	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO 01189 W.T.M.		1-5-76	
C	REVISED PER ECO 01650	23,4	10-13-76	
D	REVISED PER ECO 06473		5-29-8	

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
REVISION	D	D	D	D																			

AYDIN MONITOR SYSTEMS
FORT WASHINGTON PENNA 19034

TITLE CARD ASSEMBLY
TYPE BLD002-1,2
BIT LEVEL DIGITIZER

CODE IDENT 20747
CONTRACT NO.

DRAWN	Karl Basic	27 MAY 1975	ENGINEER	6/13/75		DWG NO. PL460-1164-501 502	REV D
CHECKED	ES		APPROVED	6/13/75			
DRAFTING	E Stickles	6/13/75				SHEET 1 OF 4	

800-0066

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	1	C	400-1348	——	20747	BD, PRINTED WIRING	
		1	1	2	A	108-203-040	7022-040-000-001	91662	CONN, FINGER BLOCK	
				3						
		—	10	4	A	102-422-104	CY20C104M	71590	CAP, .1 UF, 50V, 20%	(NOTE 3) C1-C3, C5-C11
		1	1	5	A	102-418-103	CW20A103K	71590	CAP, .01 UF, 100V, 10%	C4 (NOTE 3)
		6	-	6	A	102-422-104	CY20C104M	71590	CAP, .1 UF, 50V, 20%	C3, C5, C6, C9, C10, C11
		-	4	7	A	104-503-014	1N4531	03508	DIODE, SILICON	CR1-CR4
		2	-	8	A	104-503-014	1N4531	03508	DIODE, SILICON	CR3, CR4
				9						
		-	2	10	A	103-439-002	KE4392	27014	TRANS, SILICON, N-FET	Q1, Q5
		-	4	11	A	103-308-001	2N3906	04713	TRANS, SILICON, PNP	Q2, Q3, Q4, Q6
				12						
		1	1	13	A	103-314-202	2N2905	04713	TRANS, SILICON, PNP	Q7
				14						
		1	-	15	A	100-017-332	RC05GF3325	81349	RES, 3.3K 1/8W, 5%	R31
		2	2	16	A	100-017-122	RC05GF122J	81349	RES, 1.2K, 1/8W, 5%	R1, R2
		1	1	17	A	100-017-331	RC05GF331J	81349	RES, 330Ω, 1/8W, 5%	R3
		—	3	18	A	100-017-102	RC05GF102J	81349	RES, 1K, 1/8W, 5%	R4, R15, R17
		-	4	19	A	100-017-103	RC05GF103J	81349	RES, 10K, 1/8W, 5%	R5, R6, R38, R39
		—	5	20	A	100-215-4991	RN55C4991F	81349	RES, 4.99K, 1/10W, 1%	R7, R8, R11, R12, R29
				21						
		—	4	22	A	100-215-1002	RN55C1002F	81349	RES, 10K, 1/10W, 1%	R9, R10, R24, R28

DRAWN	CHECKED	TITLE	CODE IDENT NO.	DWG NO.	REV
K. Bucci		CARD ASSEMBLY TYPE BLD002-□ BIT LEVEL DIGITIZER	20747	460-1164-□	
DATE 5 JUN. 1975	DATE			SHEET 2 OF	

800-0477

AYDIN MONITOR SYSTEMS

QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	SIZE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		-	2	23	A	100-215-1003	RN55C1003F	81349	RES, 100K, 1/10W, 1%	R13, R19
		-	2	24	A	100-215-1473	RN55C1473F	81349	RES, 147K, 1/10W, 1%	R14, R18
		-	1	25	A	100-017-154	RC05GF154J	81349	RES, 150K, 1/8W, 5%	R16
		-	1	26	A	100-017-202	RC05GF202J	81349	RES, 2K, 1/8W, 5%	R20
		-	1	27	A	100-017-123	RC05GF123J	81349	RES, 12K, 1/8W, 5%	R21
		-	1	28	A	100-017-153	RC05GF153J	81349	RES, 15K, 1/8W, 5%	R22
		-	1	29	A	100-017-152	RC05GF152J	81349	RES, 1.5K, 1/8W, 5%	R23
		-	1	30	A	100-215-4871	RN55C4871F	81349	RES, 4.87K, 1/10W, 1%	R25
		-	1	31	A	100-017-223	RC05GF223J	81349	RES, 22K, 1/8W, 5%	R26
		-	4	32	A	100-017-101	RC05GF101J	81349	RES, 100Ω, 1/8W, 5%	R27, R32, R33, R43
		1	1	33	A	100-017-512	RC05GF512J	81349	RES, 5.1K, 1/8W, 5%	R30
		-	1	34	A	100-017-682	RC05GF682J	81349	RES, 6.8K, 1/8W, 5%	R31
		2	2	35	A	100-017-272	RC05GF272J	81349	RES, 2.7K, 1/8W, 5%	R34, R35
		2	2	36	A	100-005-131	RC20GF131J	81349	RES, 130Ω, 1/2W, 5%	R36, R37
		-	1	37	A	100-017-470	RC05GF470J	81349	RES, 47Ω, 1/8W, 5%	R40
		-	1	38	A	100-017-562	RC05GF562J	81349	RES, 5.6K, 1/8W, 5%	R41
		-	1	39	A	100-017-472	RC05GF472J	81349	RES, 4.7K, 1/8W, 5%	R42
		1	-	40	A	100-017-102	RC05GF102J	81349	RES, 1K, 1/8W, 5%	R4
		2	-	41	A	100-017-103	RC05GF103J	81349	RES, 10K, 1/8W, 5%	R38, R39
		1	-	42	A	100-215-4991	RN55C4991F	81349	RES, 4.99K, 1/10W, 1%	R29
		1	1	43	A	139-152-400	SN74S00N-10	01295	IC, QUAD NAND GATE	U1
		1	1	44	A	139-152-175	SN74S175N-10	01295	IC, QUAD D-TYPE FLIPFLOP	U2

DRAWN M. Basic DATE 5 JUN. 1975	CHECKED DATE	TITLE CARD ASSEMBLY TYPE BLD002-□ BIT LEVEL DIGITIZER	CODE IDENT NO. 20747	DWG NO. 460-1164-□ SHEET 3 OF	REV D

800-0438A

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QTY 504	QTY 503	QTY 502	QTY 501	ITEM NO.	TYPE	MONITOR PART NUMBER	VENDOR PART NUMBER	VENDOR CODE IDENT NO.	DESCRIPTION	NOTES
		1	1	45	A	139-046-174	SN74174N-10	01295	IC, HEX D-TYPE FLIP FLOP	U3
		-	5	46	A	139-163-002	SN72558P-10	01295	IC, OP AMP	U4,U5,U7,U10,U11
		1	-	47	A	139-163-002	SN72558P-10	01295	IC, OP AMP	U7
		1	1	48	A	139-085-107	SN75107AN-10	01295	IC, DUAL LINE RECEIVER	U6
		-	1	49	A	139-046-432	SN7432N-10	01295	IC, QUAD OR GATE	U8
		-	1	50	A	139-046-440	SN7440N-10	01295	IC, DUAL NAND BUFFER	U9
		1	-	51	A	100-215-1002	RN55C1002F	81349	RES, 10K, 1/10W, 1%	R28
		2	-	52	A	100-017-101	RC05GF101J	81349	RES, 100Ω, 1/8W, 5%	R32, R33
		1	1	53	A	121-202-010	8041-1G6	91506	TEST JACK, (BLK)	DIG GND
		3	3	54	A	121-202-005	8041-1G7	91506	TEST JACK, (GRN)	TP1-TP3
		1	1	55	A	116-002-003	TXBF-032-025B	98978	HEAT SINK, TRANS	INSTALL ON Q7
		1	1	56	A	131-008-001	10001	07047	PAD, TRANS, (TO-5)	INSTALL ON Q7
		AR	AR	57	A	120-101-001	—	81348	SOLDER, SN63BS	QQ-S-571
				58						
		-	REF	59	M	460-1164-501	—	20747	CARD ASSY & SCHI MATIC	
		REF	-	60	D	460-1164-502	—	20747	CARD ASSY SCHEMATIC	

DRAWN K. Basic DATE 5 JUN. 1975	CHECKED DATE	TITLE CARD ASSEMBLY TYPE BLD002-□ BIT LEVEL DIGITIZER	CODE IDENT NO. 20747	DWG NO. 460-1164-□ SHEET 1 OF 1	REV D

800-04[illegible]A

REVISIONS				
REV.	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED

GENERAL NOTES

1. For additional information see Assembly Drawing 355-0002-501
2. Unless otherwise indicated, all wire is MIL-W-16878, type B, #26 AWG white.
3. Chains must be run in order shown.

NOTE. TO GENERATE MODEL 352-0557-504/356-0002-503
Delete wires shown on Sh, 2
Add wires shown on Sh, 3

SHEET	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	
REVISION																				
SHEET	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
REVISION																				
SHEET	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REVISION																				
SHEET	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
REVISION																				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REVISION																				

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FORT WASHINGTON, PENNSYLVANIA

TITLE MODEL 335 MOD. FOR SOFT DECISION

CODE IDENT 20747
CONTRACT NO.

DRAWN	F Hinkle		ENGINEER	Jim Mather	10/15/80	DWG NO. 730-2012	REV H
CHECKED			APPROVED	[illegible]	16 Oct 80		
DRAFTING			MFG	T Melgrave		SIZE A	SHEET 1 OF 3

FORM NO. 800-0126B

APPENDIX D

Model 1126B Interface & Soft Bit Decision
Options 11, 21, Model Number 356-0002-504

GENERAL

For information on the Model 335 PCM Bit Synchronizer, model number 356-0002-504, refer to the following appendices: Appendix B (Model 1126B interface) and Appendix C (soft bit decision). The BNC rear panel outputs for this model are the same as those for soft bit decision (table C2-1). The following drawing, included in this appendix, contains the wiring changes made to the standard unit for these options:

Model 335 Mod. for Soft Decision/1126B, No. 730-2013

REVISIONS				
REV.	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED
B	REVISED PER ECO #06063 J.S.G.		4M4281	RSVol 2

GENERAL NOTES

1. For additional information see Assembly Drawing 355-0002-501
2. Unless otherwise indicated, all wire is MIL-W-16878, type B, #26 AWG white.
3. Chains must be run in order shown.

NOTE - TO GENERATE MODEL 352-0557-508/356-0002-504
Delete wires shown on Sh 2
Add wires shown on Sh 3-5

SHEET	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	
REVISION																				
SHEET	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
REVISION																				
SHEET	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REVISION																				
SHEET	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
REVISION																				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REVISION	B	B	A	B	A															

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TITLE MODEL 335 MOD. FOR SOFT DECISION / 1126B

CODE IDENT 20747
CONTRACT NO.

DRAWN	F Hinkle	7-1-80	ENGINEER	[illegible]	10/15/80	DWG NO. 730-2013	REV B
CHECKED			APPROVED	RSVol 2	16 Oct 80		
DRAFTING			MPG	[illegible]		SIZE A	SHEET 1 OF 5

FORM NO. 800-0126B

LINE	FUNCTION NAME/CODE	REMOVE WIRE RUN					REMARKS (SEE NOTE)
		FROM	TO	TO	TO	TO	
1	READ	J17-X	A4A7-11	A4A8-11			GRN/W
2	WRITE	J17-Y	A3A5-7				BRN/W
3	ACK	J17-V	A4A7-4				RED/W
4		J17-AA	A4A8-40				BLK
5		J17-BB	A4A8-36				RED
6		J17-CC	A4A8-33				WHT
7		J17-DD	A4A8-30				GRN
8		J17-EE	A4A8-28				ORN
9		J17-FF	A4A8-23		BUNDLE TOGETHER & PUT SLEEVING OVER ENDS		BLU
10		J17-HH	A4A8-20				BRN
11		J17-JJ	A4A8-17				YEL
12		J17-KK	A1A9-27		PUT SLEEVING OVER END		VIO.
13							
14	90°	A4A9-10	A4A9-23				
15	0°	A4A9-20	A4A9-26				
16	$\overline{\text{HF-NRZ}}$	A1A4-5	A1A5-29				
17	HF-NRZ	A1A4-6	A1A5-28				
18							
19							
20							

NOTE - J17 WIRES WILL BE REPOSITIONED, DO NOT REMOVE WIRES FROM J17.

REMOVE THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST # 760-0219 AND CABLE WIRE LIST # 730-1702 TO GENERATE MODEL 352-0557-508/356-0002-504

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800-0118

DRAWN	TITLE MODEL 335 - MOD FOR SOFT DECISION / 1126B	CODE IDENT NO. 20747	DWG NO. 730-2013	REV B
DATE			SHEET 2 OF 5	

800-0118

LINE	FUNCTION NAME/CODE	ADD. WIRE RUN					REMARKS (SEE NOTE)
		FROM	TO	TO	TO	TO	
1	2°	J17-AA	A4A5-38				BLK.
2	2¹	J17-BB	A4A5-35				RED
3	SYNC STATUS	J17-CC	A4A5-31				WHT
4	$\overline{\text{LOSS}}$	J17-DD	A4A5-34				GRN
5	LOCAL/REMOTE	J17-EE	A4A5-10				ORN.
6	$\overline{\text{R/W ACK}}$	J17-V	A4A8-4				RED/W
7	$\overline{\text{R/W}}$	J17-X	A3A5-7	A4A7-27			GRN/W
8	LOCAL/REMOTE	A3A1-39	A4A5-11	A4A5-12			
9		A4A7-18	A4A7-11	A4A8-11			
10		A4A7-12	A4A8-27				
11	VERIFY STROBE	A4A8-18	A4A5-15				
12	TRANS. STROBE	A3A5-4	A4A5-14				
13	R/W ACK	A4A5-13	A4A8-10				
14		A4A8-13	A4A8-5				
15	1B1	A2A4-26	A4A5-7	A4A5-8			
16	1B2	A2A4-27	A4A5-4	A4A5-5			
17	LOSS	A1A9-25	A4A5-32	A4A5-33			
18	$\overline{\text{SYNC}}$	A1A11-7	A4A5-29	A4A5-30			
19	$\overline{\text{1B1}}$	A4A5-9	A4A5-39	A4A5-40			
20	$\overline{\text{1B2}}$	A4A5-6	A4A5-36	A4A5-37			

ADD THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST # 760-0219, AND CABLE WIRE LIST # 730-1702 TO GENERATE MODEL 352-0557-508/356-0002-504

MONITOR SYSTEMS INC.

DRAWN	TITLE MODEL 335 MOD. FOR SOFT DECISION/1126B	CODE IDENT NO. 20747	DWG NO. 730-2013	REV A
DATE			SHEET 3 OF 5	

800-0118

800-0118

LINE	FUNCTION NAME/CODE	ADD WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
21	CB0/VR0	A4A8-40	A3A5-20				
22	CB1/VR1	A4A8-36	A3A5-23				
23	CB2/VR2	A4A8-33	A3A5-25				
24	CB3/VR3	A4A8-30	A3A5-14				
25	CB4/VR4	A4A8-28	A3A5-17				
26	CB5/VR5	A4A8-23	A3A5-19				
27	CB6/VR6	A4A8-20	A3A5-5				
28	CB7/VR7	A4A8-17	A3A5-9				
29	+5V P/U	A4A5-24	A4A5-25	A4A5-26	A4A5-28		
30							
31							
32	$\overline{\text{LF-NRZ}}$	A1A2-7	A4A3-33				TWST PR. & BLK GRN
33	LF-NRZ	A1A2-8	A4A3-32				
34	$\overline{\text{HF-NRZ}}$	A1A4-5	A4A3-25				TWST PR. & BLK GRN
35	HF-NRZ	A1A4-6	A4A3-26				
36	HF-NRZ*	A1A5-28	A4A3-37				TWST PR. & BLK GRN
37	$\overline{\text{HF-NRZ}}$*	A1A5-29	A4A3-38				
38	ϕ3	A1A10-22	A4A4-6				TWST PR. & BLK GRN
39	ϕ1	A1A10-21	A4A4-5				
40	DEC 4	A4A1-5	A4A3-34				WHT #26

ADD THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST # 760-0219 TO GENERATE MODEL 352-0557-508 / 356-0002-504

MONITOR SYSTEMS INC.

DRAWN	TITLE MODEL 335 MOD. FOR SOFT DECISION / 1126 B	CODE IDENT NO. 20747	DWG NO. 730-2013	REV B
DATE			SHEET 4 OF 5	

800-0118

800-0118

LINE	FUNCTION NAME/CODE	ADD WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
41	-5V	A4A3-3	A4A4-8				1uH #26
42	$+\overline{V_1}$	A4A3-5	A4A4-13				
43	$-\overline{V_1}$	A4A3-4	A4A4-14				
44	$+\overline{V_2}$	A4A3-11	A4A4-11				
45	$-\overline{V_2}$	A4A3-10	A4A4-12				
46	$+\overline{V_3}$	A4A3-16	A4A4-10				
47	$-\overline{V_3}$	A4A3-15	A4A4-9				
48	LSB	A4A4-7	A4A9-26				
49	NMSB	A4A4-4	A4A9-23				
50							

ADD THE ABOVE WIRES TO MODEL 335 LIBRARY
WIRE LIST # 760-0219 TO GENERATE
MODEL 352-0557-508/356-0002-504

MONITOR SYSTEMS INC.

DRAWN	TITLE MODEL 335 MOD. FOR SOFT DECISION/1126 B	CODE IDENT NO. 20747	DWG NO. 760-2013	REV A
DATE			SHEET 5 OF 5	

800-0118

800-011

APPENDIX E

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This appendix contains the information necessary to operate and maintain the Model 335 PCM Bit Synchronizer, model number 356-0002-505, supplied with data quality (option 22). The data quality output option is very similiar in theory and operation to the soft bit decision option, which is explained in Appendix C. To avoid repetition, only the differences between the two are explained here.

1.2 PHYSICAL DESCRIPTION

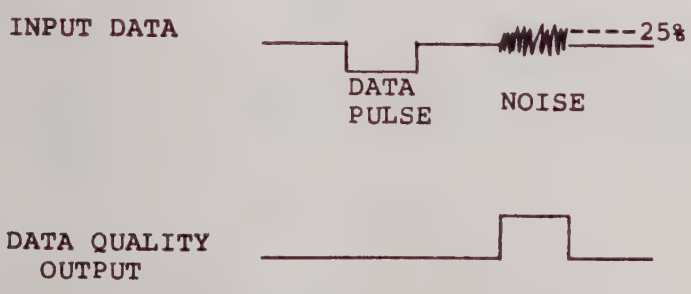
The front and rear views of the standard bit synchronizer are not changed with the addition of data quality output. See figure C1-1 in Appendix C for the top view.

Modifications to the bit synchronizer are made with the addition of two circuit cards in library file A4.

A4A3 - BLD001-3, Bit Level Detector
A4A4 - BLD002-2, Bit Level Digitizer

1.3 OVERALL FUNCTIONAL DESCRIPTION

A simplified block diagram of a bit synchronizer with data quality is shown in figure E1-1. The data quality bit (corresponding to the NMSB in soft decision) is attained by sampling the amount of noise on the signal. The output is a logic one whenever the amount of signal noise crosses a threshold level, which is preadjustable from 15% to 35%. The data quality signal is passed to the line drivers, and output to the rear panel. The drawing below illustrates the correlation between input data and data quality output.



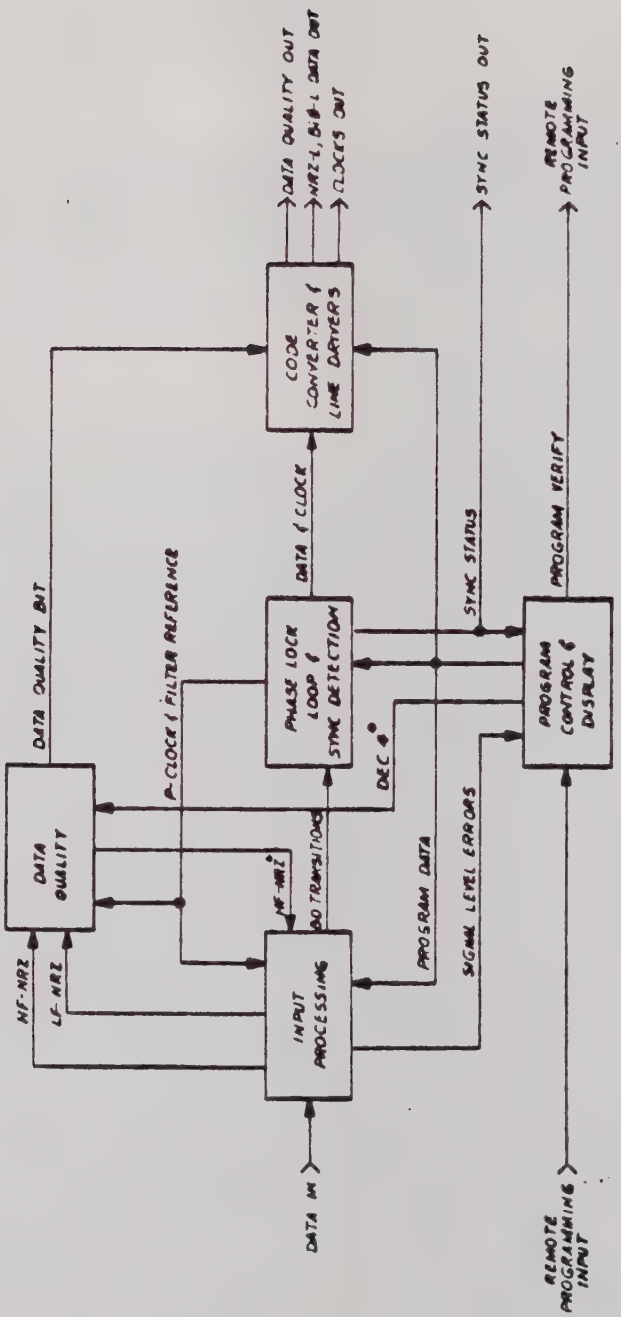


Figure E1-1. Model 335 Bit Synchronizer with Data Quality Output, Simplified Block Diagram

SECTION II

INSTALLATION

2.1 GENERAL

The two printed circuit cards associated with the -505 unit are factory-installed,

2.2 REAR PANEL INPUT/OUTPUT CONNECTIONS

The function of each BNC connector is given in table E2-1. J2 and J7 are identical outputs. The sync status output is a corollary modification with this option. A logic one indicates sync and a zero indicates lack of sync.

Table E2-1. BNC Rear Panel Connectors

DESIGNATION	FUNCTION
J1	+3v 0° Clock Output
J2	Data Quality
J3	+3v NRZ-L Output
J4	+3v 180° Clock Output
J5	+3v 90° Clock Output
J6	Sync Status
J7	Data Quality
J8	+3v 270° Clock Output
J9	Tape Recorder NRZ-L Output
J10	Tape Recorder BiØ-L Output
J11	Data Input 4
J12	Data Input 3
J13	Data Input 2
J14	Data Input 1
J15	External Clock Input

Output logic levels:

J1 through J8 are 0v ±0.5v to 3.5v ±0.5v
J9 and J10 are adjustable from 2.0v p-p to 6.0v p-p
All outputs should be terminated into 50 ohms.

SECTION III

The operation procedures of the bit synchronizer are not affected by the addition of data quality.

SECTION IV

THEORY OF OPERATION

The theory of operation of the data quality option is identical to that of soft bit decision (explained in Appendix C). The data quality output bit corresponds to the NMSB in soft decision; the LSB and MSB are don't cares.

SECTION V

MAINTENANCE

5.1 GENERAL

Maintenance procedures presented in the manual are unchanged by the addition of data quality output.

5.2 ADJUSTMENT PROCEDURES

Of the two additional cards, only BLD001-3 requires adjustment. These are four potentiometers located on this card; to properly adjust them, use the following procedure.

a. Set bit rate to 100 Kbps, NRZ-L code, unit in sync.

b. With an oscilloscope observe TP1, matched filter signal. Note signal amplitude (approx. 2 volts p-p).

c. Adjust pot R6 as required so that the signal present at TP1 is balanced about ground.

d. Set bit rate to 1 Kbps, NRZ-L, unit in sync.

e. With an oscilloscope monitoring TP1, adjust pot R45 so that signal present at TP1 is balanced about ground.

f. Continue to monitor TP1 and adjust R48 so that the signal amplitude is the same at 1 Kbps as it is at 100 Kbps.

g. Continue to monitor TP1 and with a second oscilloscope probe monitor TP3. Adjust R29 as required to select threshold levels, normally 25% of the peak signal level at TP1.

SECTION VI

DRAWINGS AND PARTS LISTS

See Appendix C for the assembly, logic and schematic drawings and parts lists for the data quality pc boards: BLD001-3 (drawing no.

460-1161-503) and BLD002-2 (drawing no. 460-1164-502). The following drawing, included in this appendix, lists the wiring changes that are made to the standard unit for this option:

Model 335 Mod. for Data Quality, no. 730-2219.

REVISIONS				
REV.	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED

GENERAL NOTES

1. For additional information see Assembly Drawing 355-0002-501
2. Unless otherwise indicated, all wire is MIL-W-16878, type B, #26 AWG white.
3. Chains must be run in order shown.

NOTE - TO GENERATE MODEL 356-0002-505
DELETE WIRES SHOWN ON SH. 2.
ADD WIRES SHOWN ON SH. 3+4.

SHEET	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	
REVISION																				
SHEET	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
REVISION																				
SHEET	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REVISION																				
SHEET	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
REVISION																				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REVISION	A	A	A	A																

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TITLE MODEL 335 MOD.
FOR DATA Q

CODE IDENT 20747
CONTRACT NO.

DRAWN			ENGINEER	RS Volz	2MAY83	DWG NO. 730-2219	REV A
CHECKED			APPROVED	RS Volz	2MAY83		
DRAFTING				M. Mann	5/12/83	SIZE A SHEET 1 OF 4	

FORM NO. 800-L 8

LINE	FUNCTION NAME/CODE	REMOVE WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
1	0°	A1A10-15	A4A9-2[illegible]	A4A9-26			
2	90°	A4[illegible]	[illegible]				
3	180°	A1A10-16	A4[illegible]				
4	270°	A1A10-13	A4A9-[illegible]				
5							
6	DATA	A1A10-9	A4A[illegible]	[illegible]			
7							
8	HF-NRZ	A1A4-5	A1A5-[illegible]				
9	—	A1A4-6	A1A[illegible]				BLK GRN
10							

REMOVE THE ABOVE WIRES TO MODEL [illegible] LIBRARY WIRE [illegible] #760-0219 TO GENERATE MODEL 356-0002-505

MONITOR SYSTEMS

800-0118

DRAWN	TITLE MODEL 335 MOD FOR DATA Q	CODE IDENT NO. 20747	DWG NO. 730-2219	REV A
DATE			SHEET 2 OF 4	

LINE	FUNCTION NAME/CODE	ADD WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
1	$\overline{LF-NRZ}$	A1A2-7	A4A3-33				BLK/GRN
2	—	A1A2-8	A4A3-32				
3							
4	$\overline{HF-NRZ}$	A1A4-5	A4A3-25				BLK/GRN
5	—	A1A4-6	A4A3-26				
6							
7	HF-NRZ	A1A5-28	A4A3-37				GRN/BLK
8	—	A1A5-29	A4A3-38				
9							
10	$\phi 1$	A1A10-21	A4A4-5				GRN/BLK
11	$\phi 3$	A1A10-22	A4A4-6				
12							
13	DEC 4	A4A1-5	A4A3-34				WHT #26
14							
15	SYNC/LOCK	A1A9-27	A4A9-14				
16							
17	-5 V	A4A3-8	A4A4-8				
18							
19	+ $\overline{V_1}$	A4A3-5	A4A4-13				
20	- $\overline{V_1}$	A4A3-4	A4A4-14				

ADD THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST #760-0219 TO GENERATE MODEL 356-0002-505

MONITOR SYSTEMS

800-0118

DRAWN	TITLE MODEL 335 MOD FOR DATA Q	CODE IDENT NO. 20747	DWG NO. 730-2219	REV A
DATE			SHEET 3 OF 4	

LINE	FUNCTION NAME/CODE	ADD WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
21	$+\overline{V_2}$	A4A3-11	A4A4-11				WHT #26
22	$-\overline{V_2}$	A4A3-10	A4A4-12				
23							
24	$+\overline{V_3}$	A4A3-16	A4A4-10				
25	$-\overline{V_3}$	A4A3-15	A4A4-9				
26							
27	NMSB	A4A4-4	A4A9-7	A4A9-23			
28							
29	0° CLOCK	A1A10-15	A4A9-26				
30	180°	A1A10-16	A4A9-20				
31	270°	A1A10-13	A4A9-4				
32							
33	DATA	A1A10-9	A4A9-16				
34							
35							
36							
37							
38							
39							
40							

ADD THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST #760-0219 TO GENERATE MODEL 356-0002-505

MONITOR SYSTEMS

800-0118

DRAWN	TITLE MODEL 335 MOD. FOR DATA Q	CODE IDENT NO. 20747	DWG NO. 730-2219	REV. A
DATE			SHEET 4 OF 4	

APPENDIX F

Model 1126E Interface & Data Quality Output
Options 11, 22, Model Number 356-0002-506

GENERAL

For information on the Model 335 PCM Bit Synchronizer, model number 356-0002-506, refer to the following appendices: Appendix B (model 1126B interface) and Appendix E (data quality output). The BNC rear panel outputs for this model are the same as those for the -505 model (table E2-1). The following drawing, included in this appendix, lists the wiring changes that are made to the standard unit for this option:

Model 335 Mod. for Data Quality/1126B, No. 730-2015

REVISIONS				
REV.	DESCRIPTION	EFFECTIVE ON S/N	DATE	APPROVED

GENERAL NOTES

1. For additional information see Assembly Drawing [redacted] 355-0002-501
2. Unless otherwise indicated, all wire is MIL-W-16878, type B, #26 AWG white.
3. Chains must be run in order shown.

NOTE - TO GENERATE MODEL 356-0002-506
DELETE WIRES SHOWN ON SH. 2
ADD WIRES SHOWN ON SH. 3, 4, 5

SHEET	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	
REVISION																				
SHEET	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
REVISION																				
SHEET	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REVISION																				
SHEET	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
REVISION																				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REVISION	A	A	A	A	A															

MONITOR
an AYDIN company
FORT WASHINGTON, PENNSYLVANIA

TITLE MODEL 335 MOD.
FOR DATA QUALITY/1126B

CODE IDENT 20747
CONTRACT NO.

DRAWN			ENGINEER	F. HINKLE		DWG NO. 730-2015	REV A
CHECKED	J Hinkle	7-27-81	MFG APPROVED	[illegible]	7/30/81		
DRAFTING			APPR.	RJW	7/27/81	SIZE A	SHEET 1 OF 5

FORM NO. 800-0126B

LINE	FUNCTION NAME/CODE	REMOVE WIRE RUN					REMARKS (SEE NOTE)
		FROM	TO	TO	TO	TO	
1	90°	A4A9-10	A4A9-23				
2	270°	A1A10-13	A4A9-7				
3	180°	A1A10-16	A4A9-14				
4							
5							
6	$\overline{\text{HF-NRZ}}$	A1A4-5	A1A5-29				BLK
7	HF-NRZ	A1A4-6	A1A5-28				BRN 8
8	READ	J17-X	A4A7-11	A4A8-11			BRN/W
9	WRITE	J17-Y	A3A5-7				BRN/W
10	ACK.	J17-V	A4A7-4				RED/W
11		J17-AA	A4A8-40				BLK
12		J17-BB	A4A8-36				RED
13		J17-CC	A4A8-33				WHT
14		J17-DD	A4A8-30				BRN
15		J17-EE	A4A8-28				ORG
16		J17-FF	A4A8-23		BUNDLE TOGETHER AND PUT SLEEVING OVER ENDS		GRN
17		J17-HH	A4A8-20				BRN
18		J17-JJ	A4A8-17				YEL
19		J17-KK	A1A9-27		PUT SLEEVING OVER END.		VIO

MONITOR SYSTEMS

REMOVE THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST #760-0219 AND CABLE WIRE LIST #730-1702 TO GENERATE MODEL 356-0002-506.

NOTE: J17 WIRES WILL BE REPOSITIONED, DO NOT REMOVE WIRES FROM J17.

800-0118

DRAWN / DATE	TITLE	CODE IDENT NO.	DWG NO.	REV
		20747	730-2015 SHEET 2 OF 5	A

LINE	FUNCTION NAME/CODE	ADD WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
1	$\overline{LF\text{-}NRZ}$	A1A2-7	A4A3-33				TWST PR 8 BLK GRN
2	LF-NRZ	A1A2-8	A4A3-32				
3	$\overline{HF\text{-}NRZ}$	A1H4-5	A4A3-25				TWST PR 8 BLK GRN
4	HF-NRZ	A1H4-6	A4A3-26				
5	HF-NRZ	A1H5-28	A4A3-37				TWST PR. 8 GRN BLK
6	$\overline{HF\text{-}NRZ}$	A1A5-29	A4A3-38				
7	$\phi 3$	A1A10-22	A4A4-6				TWST PR. 8 BLK GRN
8	$\phi 1$	A1A10-21	A4A4-5				
9	DEC 4	A4A1-5	A4A3-34				WHT #26
10	SYNC/LOCK	A1A9-27	A4A9-14				
11	-5V	A4A3-8	A4A4-8				
12	$+\overline{V1}$	A4A3-5	A4A4-13				
13	$-\overline{V1}$	A4A3-4	A4A4-14				
14	$\overline{+V2}$	A4A3-11	A4A4-11				
15	$\overline{-V2}$	A4A3-10	A4A4-12				
16	$\overline{+V3}$	A4A3-16	A4A4-10				
17	$\overline{-V3}$	A4A3-15	A4A4-9				
18	NMSB	A4A4-4	A4A9-7	A4A9-23			
19	$\overline{R/W}$	J17-X	A3A5-7	A4A7-27			
20	LOCAL/REMOTE	J17-EE	A4A5-10				

ADD THE ABOVE WIRES TO MODEL 335 LIBRARY WIRE LIST # 760-0219 AND CABLE WIRE LIST # 730-1702 TO GENERATE MODEL 356-0002-506.

MONITOR SYSTEMS

800-0118

DRAWN	TITLE	CODE IDENT NO.	DWG NO.	REV
DATE		20747	730-2015 SHEET 3 OF 5	A

LINE	FUNCTION NAME/CODE	ADD WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
21	$\overline{R/W\ ACK}$	J17-V	A4A8-4				
22		A4A7-18	A4A7-11	A4A8-11			
23	LOCAL/REMOTE	A3A1-39	A4A5-11	A4A5-12			
24		A4A7-12	A4A8-27				
25	VERIFY STROBE	A4A8-18	A4A5-15				
26	TRANS. STROBE	A3A5-4	A4A5-14				
27	R/WACK	A4A5-13	A4A8-10				
28		A4A8-13	A4A8-5				
29	1B1	A2A4-26	A4A5-7	A4A5-8			
30	1B2	A2A4-27	A4A5-4	A4A5-5			
31	LOSS	A1A9-25	A4A5-32	A4A5-33			
32	$\overline{SYNC}$	A1A11-7	A4A5-29	A4A5-30			
33	$\overline{1B1}$	A4A5-9	A4A5-39	A4A5-40			
34	$\overline{1B2}$	A4A5-6	A4A5-36	A4A5-37			
35	2°	J17-AA	A4A5-38				BLK
36	2′	J17-BB	A4A5-35				RED
37	SYNC STATUS	J17-CC	A4A5-31				WHT.
38	$\overline{LOSS}$	J17-DD	A4A5-34				GRN.
39	CB0/VR0	A4A8-40	A3A5-20				
40	CB1/VR1	A4A8-36	A3A5-23				

MONITOR SYSTEMS

800-0118

DRAWN	TITLE	CODE IDENT NO.	DWG NO.	REV
DATE		20747	730-2015	A
			SHEET 4 OF 5	

LINE	FUNCTION NAME/CODE	ADD WIRE RUN FROM	TO	TO	TO	TO	REMARKS (SEE NOTE)
41	CB2/VR2	A4A8-33	A3A5-25				
42	CB3/VR3	A4A8-30	A3A5-14				
43	CB4/VR4	A4A8-28	A3A5-17				
44	CB5/VR5	A4A8-23	A3A5-19				
45	CB6/VR6	A4A8-20	A3A5-5				
46	CB7/VR7	A4A8-17	A3A5-9				
47	+5V P/U	A4A5-24	A4A5-25	A4A5-26	A4A5-28		

MONITOR SYSTEMS

800-0118

DRAWN	TITLE	CODE IDENT NO.	DWG NO.	REV
DATE		20747	730-2015	A
			SHEET 5 OF 5	